A Through-Wafer Interconnect in Silicon for RFICs

Joyce H. Wu, Jörg Scholvin, and Jesús A. del Alamo

***Abstract*—In order to minimize ground inductance in RFICs, we have developed a high-aspect ratio, through-wafer interconnect (or substrate via) in silicon that features a silicon nitride barrier liner and completely filled Cu core. We have fabricated vias with a nominal aspect ratio of 30 and verified the integrity of the insulating liner in vias with an aspect ratio of eight. The inductance of vias with nominal aspect ratios between three and 30 approach the theoretically expected values. This interconnect technology was exploited in a novel Faraday cage structure for substrate crosstalk suppression in system-on-chip applications. The isolation structure consists of a ring of grounded vias that surrounds sensitive or noisy portions of a chip. This Faraday cage structure has shown noise suppression of 30 dB at 10 GHz and 16 dB at 50 GHz at a distance of 100 μm when compared to the reference structure.**

***Index Terms*—Ground inductance, Si RF technology, substrate noise, substrate via, system-on-chip (SOC), three-dimensional interconnects, through-wafer interconnect.**

I. Introduction

IN MILLIMETER-WAVE and RF applications, the high-frequency performance of silicon-based technology has been approaching that of III-V semiconductor devices in recent years. Consequently, silicon is replacing GaAs in low-end, high-volume RF applications because of its lower manufacturing costs and its integration capabilities [1]. To improve the high-frequency operation of silicon RFICs, it is crucial to reduce extrinsic parasitics. In particular, the source impedance of MOSFETs and the emitter impedance of BJTs degrade the gain, noise figure, and efficiency of RF amplifiers [2]–[4]. Through-wafer interconnects, or substrate vias, are widely used in GaAs microwave and millimeter-wave ICs to provide a low-impedance ground to reduce the source impedance [3], [4]. Extending this idea to silicon, we have developed a through-wafer via technology for silicon, which allows for the implementation of high-aspect ratio, low-impedance ground connections.

Through-wafer vias in silicon have initially been demonstrated using KOH etching [5], [6]. However, this approach results in a poor aspect ratio with a large footprint at the wafer surface. Borrowed from microelectromechanical systems (MEMS) technology, we have used deep reactive-ion etching (DRIE), which can achieve aspect ratios of up to 20 and has become a common method to etch through-wafer vias in silicon. Recently, electrochemical etching has been used to form porous Si that can produce vias of aspect ratios of 100 [7], [8]. Previous DRIE-via technologies use a thin coating of metal to line the inside surface of the via [9], [10], whereas others fill the via with highly doped polysilicon to achieve a low-impedance interconnect [11]. These different via technologies have found applications in three-dimensional (3-D) chip stacks [5], as a substrate coil inductor [9], microstrip substrate interconnect [10], and in MEMS [7], [11]. The novelty of our via technology is that it features an insulator liner and a solid metal core. Consequently, the vias exhibit very low impedance over a broad frequency range, which is essential for use in mixed-signal RF systems. They can also be used to distribute power and ground in logic circuits and MEMS. In order to characterize this technology, we have fabricated test structures that measure the impedance of a single via in the microwave regime.

In exploring other practical applications, we have exploited this via technology to construct an innovative isolation scheme to reduce substrate crosstalk in mixed-signal circuits for system-on-a-chip (SOC) applications [12]. Early results of this technology characterized up to 6 GHz were published in [13]. This paper discusses the details of the fabrication process of the substrate vias and gives more extensive results of isolated vias and Faraday cages up to 50 GHz.

II. Fabrication Technology

This paper exploits MEMS technology to develop a through-wafer via technology for applications in thin substrates and fabrication at the back-end. There are three critical process steps: 1) DRIE of Si to form vias; 2) conformal deposition of silicon nitride to line the vias; and 3) Cu electroplating and CMP to fill the vias and prepare them for metal contacts. An illustration of the via concept is depicted in Fig. 1. In order to fabricate substrate vias on thin substrates without using such fragile starting material, we developed a test vehicle on thick-film, bonded silicon-on-insulator (SOI) wafers. The SOI device layer, 75- to 100-μm thick, was intended as the substrate for via fabrication, whereas the handle wafer strengthened wafer integrity. Holes were etched in the handle wafer from the backside using KOH, and the buried oxide was etched using BOE. These holes gave access to the underside of the device layer while still maintaining wafer integrity. The backside holes and SOI handle wafer were intended only for handling purposes and are not part of the substrate-via structure.

Both trenches and vias were etched in order to facilitate the characterization of the fabrication process. Substrates had a resistivity of 10–20 $\Omega \cdot$ cm. In the following paragraphs, we give details about each of the key process steps in our technology. The process flow is depicted in Fig. 2.

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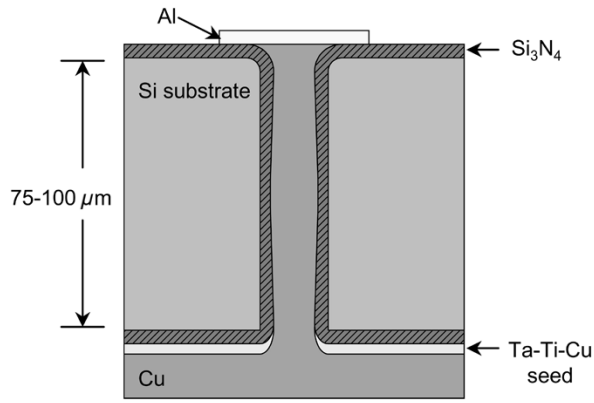

Fig. 1. Conceptual drawing of a substrate via.

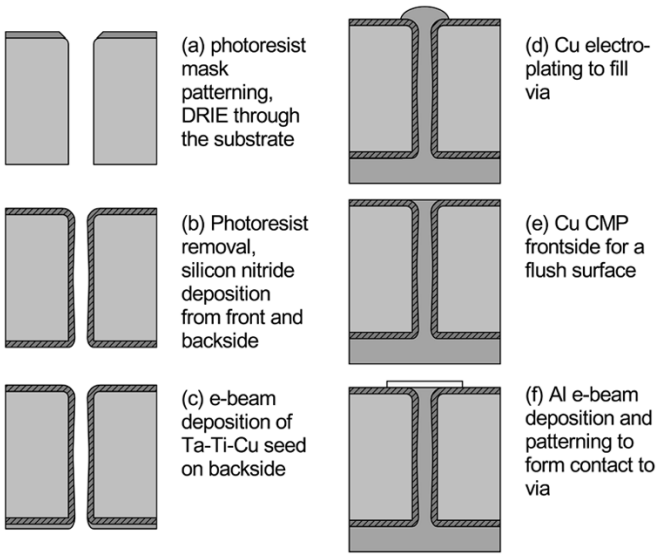

Fig. 2. Sketch of the process flow to fabricate through-wafer vias.

A. Silicon DRIE

The vias were etched through the substrate (SOI device layer) from the frontside using an STS anisotropic deep reactive-ion etcher (DRIE) with an inductively coupled plasma. The DRIE uses a Bosch etch of alternating etch and passivation cycles to achieve near-vertical sidewalls to create high-aspect ratio structures [14]. A 3-μm-thick OCG825 photoresist was used as the mask. The etch rate was about 2 $\mu\mathrm{m}/\mathrm{min}$, and trench aspect ratios as high as 49 were achieved. As in [14], we found that the etch rate decreased with increasing aspect ratio. Our results, depicted in Fig. 3, show that the dependence was noticeable but small, and that for aspect ratios as high as 20, the decrease in etch rate was less than 15%. This dependence is due to reactive-ion etch lag (RIE-lag) common in fluorinated plasmas [14].

Another consequence of DRIE is that the via opening widens as the etch proceeds due to the slant in the photoresist profile. We found that the via diameter increases by about 1 μm for every 100 μm etched in depth. This produces a small difference between the nominal diameter on the mask and the actual physical diameter of the via, and consequently, discrepancies in the nominal and actual aspect ratio. In this paper, actual aspect ratios will be quoted unless noted otherwise.

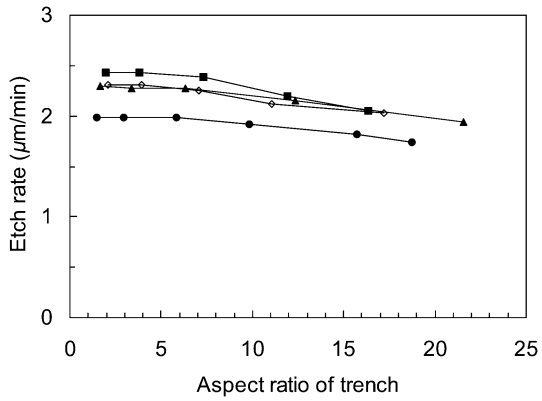

Fig. 3. DRIE etch rate versus aspect ratio for trenches on different wafers (each line). For aspect ratios as high as 20, the decrease in the etch rate is less than 15%.

B. Silicon Nitride Insulating Barrier Liner

Our goals in introducing a via liner were twofold. First, the liner must be a barrier to the Cu that fills the via because migrating Cu ions degrade device performance by inducing leakage currents [15]. Second, in order to route power and ground on the same chip, the substrate vias must be electrically insulated from the Si substrate. Amorphous dielectric films like Si_3N_4 and SiO_xN_y meet both criteria [16]. Since our process is designed so that the substrate-via fabrication is part of the backend, we deposited Si_3N_4 by plasma-enhanced chemical vapor deposition (PECVD) at 400 °C using a Novellus Concept-1. This tool combines the stable discharge and substrate coupling of high frequency plasma and the low-energy ion bombardment of low frequency for better sidewall density and step coverage [17].

To take advantage of the insulating and barrier properties of silicon nitride, the liner had to be conformal to the sidewalls of the via. To improve conformality, we deposited nitride on the frontside and backside. We characterized the conformality of PECVD silicon nitride by examining cross sections of silicon nitride deposited in through-wafer trenches. Fig. 4 plots the nitride sidewall thickness normalized to the surface thickness against the aspect ratio of through-wafer trenches. Thickness measurements were taken using the SEM at the top sidewall 1 μm from the surface and at the mid-sidewall. Fig. 4 shows that the nitride thickness at the top of the sidewall remains relatively constant, independent of aspect ratio (top line in Fig. 4). However, the thickness at the mid-sidewall decreases drastically, thinning with aspect ratio (bottom line). For aspect ratios greater than 15, the nitride was too thin or nonexistent in the middle of the trench. The highest aspect ratio trench fully lined with conformal nitride was 10. For vias, it was eight [Fig. 5(a)]. In this process, silicon nitride conformality has emerged as the limiting factor for achieving fully lined vias with higher aspect ratios. However, other deposition methods may provide better conformality.

C. Cu Electroplating

The low resistivity of Cu allows for higher current density, and Cu has proven to have increased scalability and better electromigration reliability than Al(Cu) interconnects [18]. Some

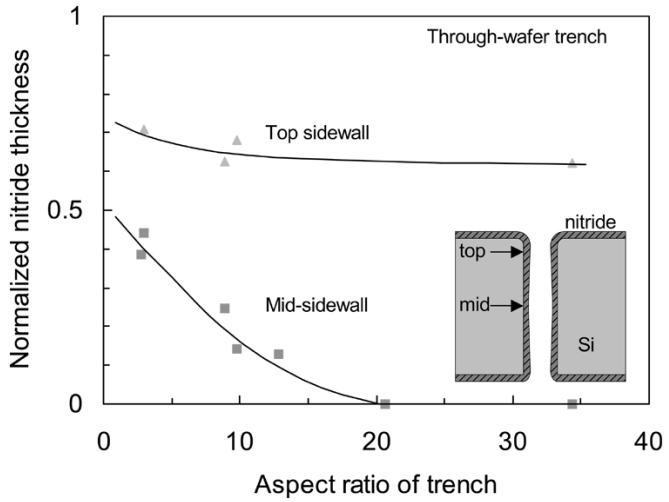

Fig. 4. Normalized PECVD silicon nitride liner thickness versus aspect ratio of a through-wafer trench. The liner thickness is normalized to the surface thickness. Mid-sidewall measurements were taken halfway down the trench and top sidewall measurements 1 μm down from the surface.

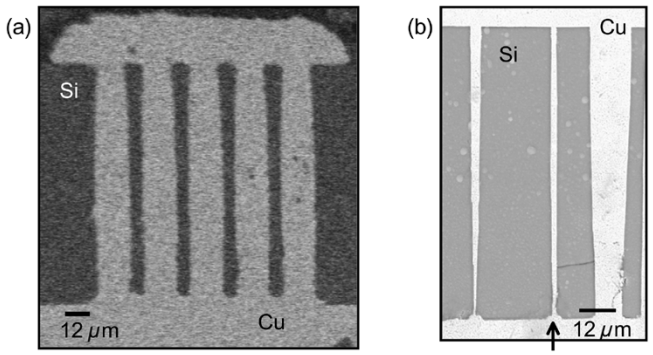

Fig. 5. (a) SEM cross section of substrate vias with an aspect ratio of 8, 12-μm-wide via in a 100-μm-thick substrate. These vias are conformally lined with silicon nitride and overfilled with Cu (SEM taken prior to the CMP step). (b) Best DRIE and Cu electroplating result (arrow): a trench of aspect ratio 49, 2-μm wide by 97-μm deep, filled with Cu without seams or voids. The "footing" at the bottom of these trenches is from a previous process in which the buried oxide was used as an etchstop for the DRIE.

disadvantages of Cu are its poor adhesion to dielectrics and the need for barrier and/or adhesion layers [18]. However, Cu has the critical advantage of being able to fill high-aspect ratio holes by electroplating.

We used a commercial Cu-sulfate solution from Enthone-OMI that is used for semiconductor applications and particularly for high-aspect ratio plating. We used a Dynatronix DuPR 10-1-3 power supply with a pulse-reverse current, which enhances electrodeposition into high-aspect ratio structures. The dissolution of Cu during the negative pulse provides a better concentration gradient of cupric ions in the via than dc, so that during the subsequent positive pulse, deposition is more uniform and void size is reduced [19]. We used a positive peak pulse of 16 mA/cm^2 for 5 ms and a negative peak pulse of -13 mA/cm^2 for 1 ms, which equates to an average current density of 11 mA/cm^2.

For our electroplating seed, we e-beam evaporated a stack of 250 Å Ta, 250 Å Ti, and 2000 Å of Cu onto the wafer backside. Due to the anisotropy of e-beam deposition and the high-aspect ratio of the vias, the seed did not significantly coat the via sidewalls, and as a result, the seed was perforated. During copper electroplating, Cu deposited onto the seed at the bottom of the via increased in thickness isotropically until the opening closed (Fig. 6). Once the via bottom was sealed, the inside of the via filled from bottom to top. This process resulted in a solid Cu core without seams and voids, as similarly reported in [19].

The rate of filling of the via had a slight inverse dependence on the opening width. This is due to initial time taken to seal the bottom of the via. Larger diameter vias will take longer to seal, and therefore will fill slower. Additionally, the Cu deposition rate varied across the wafer. By overfilling the vias and using chemical–mechanical polishing (CMP) to remove excess Cu, we were able to obtain a Cu filling that was flush with the surface for all via dimensions across the wafer and eliminated the dependence on a uniform Cu deposition rate. Contact to the via at the top was made through a patterned Al layer. The highest aspect ratio trench filled with Cu was 49 [Fig. 5(b)], and 14 for vias, although it is possible to achieve even higher aspect ratios.

III. Application I: Through-Wafer via Interconnect

A. Test Structure and Measurement Setup

To measure the impedance of a single via, we designed a one-port, 50-Ω, ground-signal-ground coplanar test structure with the via under test at the end of the signal line (Fig. 9 inset). The ground pads are shorted by 30 substrate vias to the backside Cu ground plane in order to reduce the impedance of the ground pads. Characterized vias ranged from 3 to 25 μm in nominal diameter on a 77-μm-thick substrate. S-parameters of the substrate vias were measured from 50 MHz to 50 GHz and converted to Z_{11}. The series resistance and inductance of the test structure pads were not de-embedded, so the actual impedance of a via is lower than that measured. The test structure parasitics are estimated to contribute less than 4 pH to the inductance values.

B. Results and Discussion

For all vias, the real part of Z_{11} was found to be largely independent of frequency (below about 5 GHz), whereas the imaginary part was positive and increased linearly with frequency (Fig. 7). These results suggest a simple, equivalent circuit model for a via that consists of a resistor and an inductor in series, from which the inductance was extracted. The rise in the real part at frequencies greater than 5 GHz represents an increase in resistance due to the skin effect. The skin effect is also responsible for the decline in inductance as seen in Fig. 8. This is because the effective area enclosed by the current loop is reduced due to surface current crowding. As seen in the Fig. 8, larger diameter vias are affected by the skin effect at lower frequencies.

Fig. 9 shows the averaged measured inductances of substrate vias at 10 GHz against the nominal aspect ratio along with the inductance predicted by [20]. The measured inductance values are tightly clustered and approach the theoretical curve. This suggests that it is possible to predict inductance values for a particular aspect ratio via for computer-aided circuit design tools.

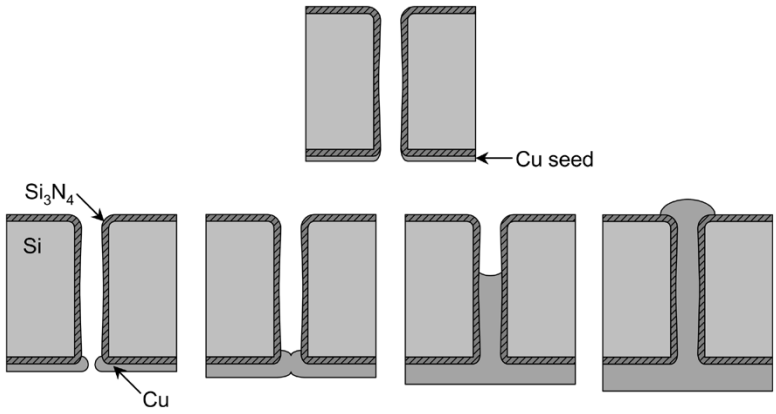

Fig. 6. Sketch of the evolution of the electrodeposition of Cu with perforated seed. Starting from the seed evaporated on the backside in Fig. 2(c), the electroplated Cu deposits isotropically on the seed. The Cu deposit grows horizontally until the Cu on the two sides of the via meet, sealing the via opening at the bottom. Then, the Cu deposits inside the via filling it and on the backside.

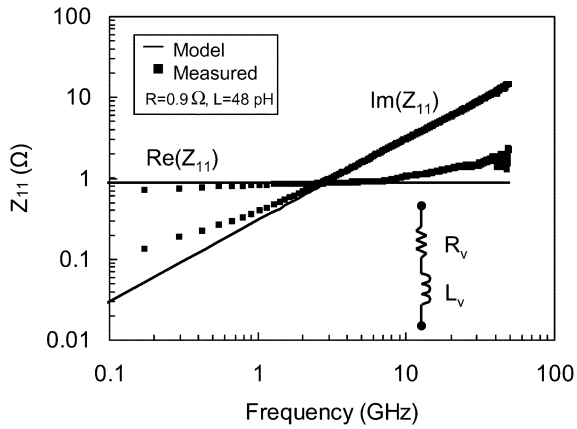

Fig. 7. Z_{11} versus frequency of a 4-μm diameter and 77-μm-deep via. The solid line plots simulation results of a series *RL* equivalent circuit model from which the indicated values of resistance and inductance are extracted. The slight rise in resistance with frequency is due to the skin effect.

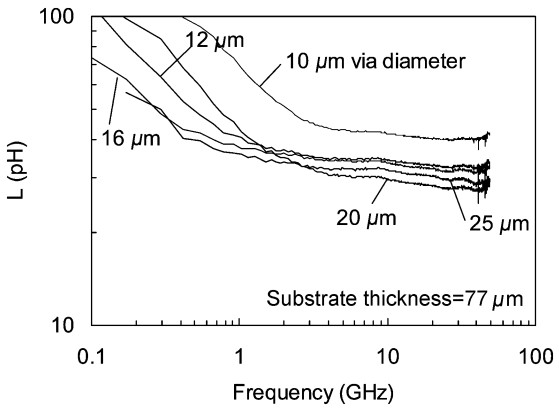

Fig. 8. Inductance extracted from the imaginary part of Z_{11} versus frequency. The inductance decreases with frequency due to the skin effect.

The residual discrepancy of the inductance with [20] may be due to parasitic inductance of the test structure or the assumptions made in the development of the model.

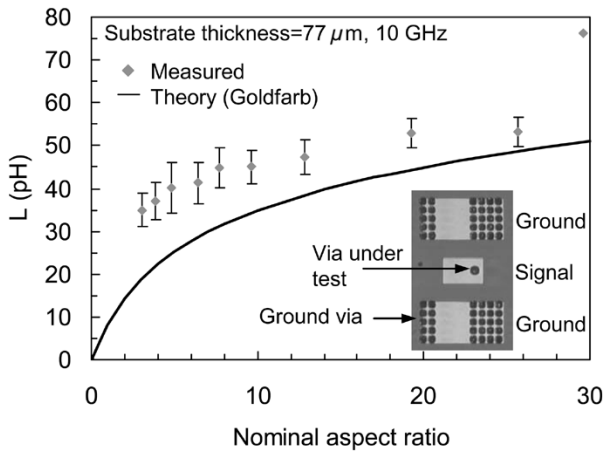

Fig. 9. Extracted inductance at 10 GHz versus nominal aspect ratio of vias on a substrate thickness of 77 μm. Each point represents the average inductance with error bars of one standard deviation in each direction. Plotted in a solid line is the inductance model of Goldfarb *et al.* [20]. *Inset*: picture of fabricated test structure to measure inductance of a single via. The multiple grounding vias reduce the impedance of the ground pads.

IV. Application II: Faraday Cage for Substrate Crosstalk Suppression

A. Motivation

One of the possible applications of high-aspect ratio substrate vias is subsystem isolation in mixed-signal circuits. Substrate crosstalk between sensitive RF circuits, analog circuits, and noisy digital blocks is a significant barrier to enabling one-chip systems. Future systems will require densely packed circuits operating at high frequency. This has motivated substantial work in the development of substrate crosstalk isolation schemes [6], [8], [21]–[25].

Traditional approaches to reduce substrate crosstalk include guard rings [21], [22], SOI and high-resistivity substrates [22]–[24], and junction-isolated wells [22]. However, unconventional techniques have achieved better crosstalk suppression, such as porous silicon [7], [8], metal-filled trenches [6], and SOI on metal with Faraday cage [25]. A comparison between different crosstalk isolation schemes is difficult due to different

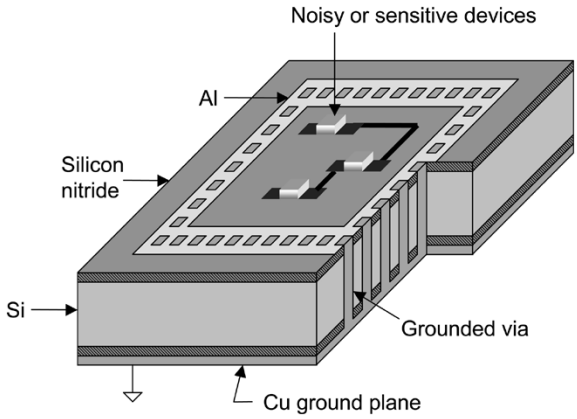

Fig. 10 Faraday cage as a novel isolation scheme for substrate crosstalk. The ring of grounded vias surrounds a noisy or a sensitive circuit.

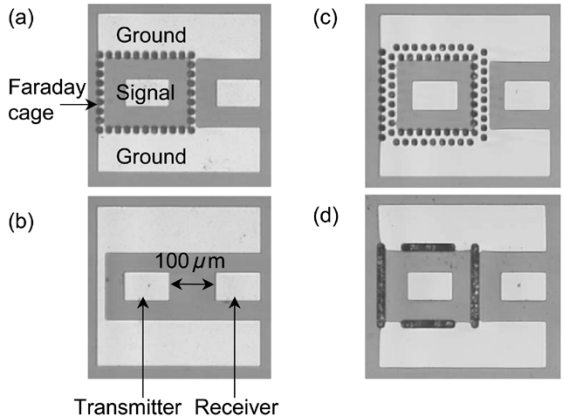

Fig. 11. Top view of (a) a Faraday cage test structure; (b) a reference test structure; (c) a double Faraday cage; and (d) a trench Faraday cage at a transmitter-receiver separation or transmission distance of 100 μm. Each via of the cage is 10 μm wide and separated by 10 μm. For the double Faraday cage, the ring of cages is separated by 10 μm.

references structures and test structure design. A key consideration when evaluating crosstalk isolation schemes is the footprint of the isolation structure and nonstandard fabrication processes. For example, in [6] the metal trench is 60-μm wide and in [8] 100-μm wide, and [25] uses a buried metal ground.

We have exploited the high-aspect ratio of our substrate vias to demonstrate a novel Faraday cage isolation scheme to suppress substrate crosstalk [12]. The Faraday cage consists of a ring of substrate vias connected to the grounded backplane on the backside of the substrate and shorted together by a ring of metal on the frontside (Fig. 10). This approach combines exceptional crosstalk suppression with a small footprint.

B. Test Structure and Measurement Setup

To determine the isolation effectiveness of the Faraday cage, we measured S_{21} up to 50 GHz using a two-port test structure in a coplanar, 50-Ω ground-signal-ground configuration (Fig. 11). The distance between the pads varied from 100 to 800 μm, and the transmitter pad was surrounded by the Faraday cage. The transmitter and receiver pads were each 62 $\times$ 100 μm in area. An identical structure was fabricated without the Faraday cage, but with the same grounded backplane, to serve as the reference [Fig. 11(b)]. Additional Faraday cage variations were examined: a double Faraday cage [Fig. 11(c)] and a discontinuous trench [Fig. 11(d)]. The double Faraday cage had one cage encircling the other, with each ring separated by 10 μm. The trench Faraday cage was 10 μm wide and was discontinuous in order to maintain the integrity of the substrate. In this implementation, we used a 77-μm-thick substrate and 10-μm-diameter vias with an aspect ratio close to 8. We also varied via spacing between 10 and 70 μm on test structures with a transmission distance of 200 μm. We had to reduce the air crosstalk between the microwave probes in order to accurately determine the crosstalk suppression of the Faraday cage. For this, we introduced a grounded metallic screen between the two probes that reduced crosstalk through the air by about 30 dB. The noise floor of our setup was reduced to around -90 dB at 1 GHz and -47 dB at 50 GHz at a probe separation distance of 100 μm.

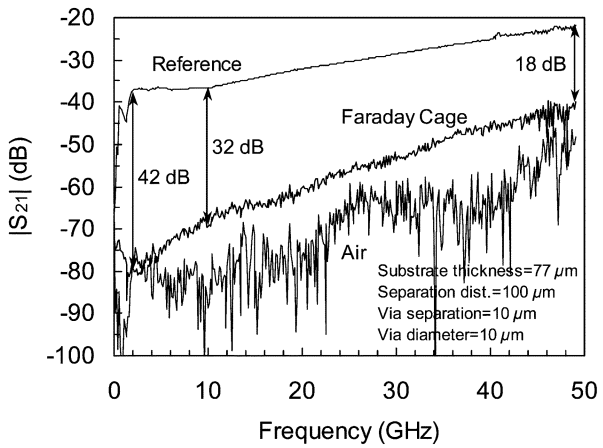

Fig. 12. $|S_{21}|$ versus frequency for a Faraday cage and reference structure at a transmission distance of 100 μm. This Faraday cage provides 32 dB of isolation at 10 GHz and 18 dB at 49 GHz. Also plotted is $|S_{21}|$ of the probes in the air.

C. Results and Discussion

Fig. 12 graphs $|S_{21}|$ against frequency for a Faraday cage at a transmission distance of 100 μm. Also shown are measurements from the reference structure and with the probes lifted in the air to show that the measurements are not limited by air crosstalk. Compared to the reference structure, on average, the Faraday cage improved isolation by 30 dB at 10 GHz and 16 dB at 50 GHz. Comparing the reference structure to one with a 20-μm wide metal Al strip between the transmitter and receiver produced only about 2 dB in isolation. Fig. 13 shows the impact of transmitter-receiver separation on crosstalk isolation at 10 GHz. On average, the Faraday cage improved isolation by 30 dB at 100 μm and 42 dB at 800 μm when compared to the reference. The reference structure shows an expected decrease in crosstalk with distance, and the Faraday cage shows an improvement in crosstalk suppression of about 12 dB as the distance is increased from 100 to 800 μm.

We have also examined the impact of via separation on isolation effectiveness. For a transmission distance of 200 μm, we fabricated Faraday cages with via spacings between 10 and

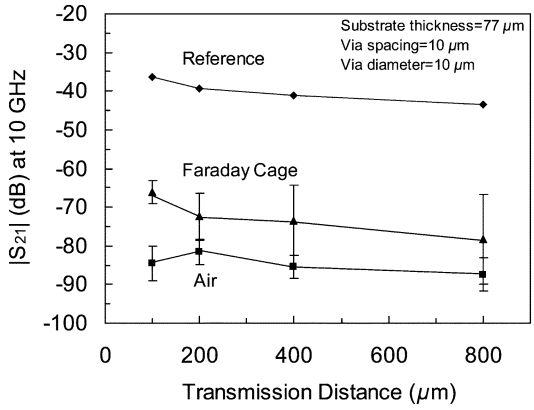

Fig. 13. Average $|S_{21}|$ at 10 GHz versus the transmitter-receiver distance for Faraday cage and reference structures. The error bars indicate one standard deviation away from the mean. Substrate crosstalk decreases with transmission distance. The effectiveness of the Faraday cage improves slightly with increasing transmission distance.

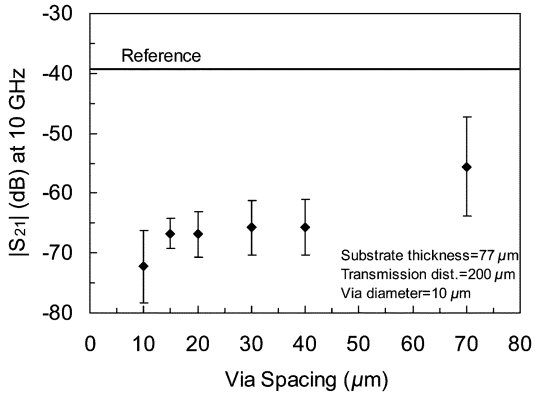

Fig. 14. Average $|S_{21}|$ versus via spacing of the Faraday cage at 10 GHz. No crosstalk dependence is apparent up to a 40-μm separation.

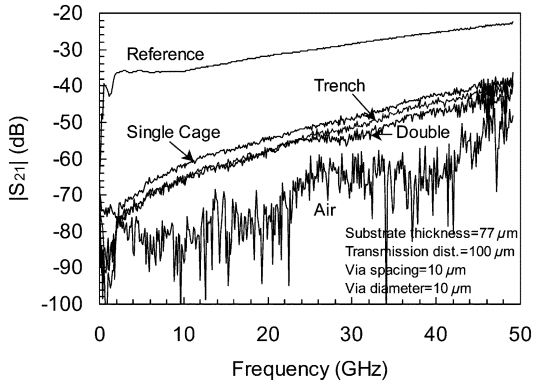

Fig. 15. $|S_{21}|$ versus frequency for a single, double, and trench Faraday cage and reference structure at a transmission distance of 100 μm. Crosstalk suppression is within 3 dB for all three types of Faraday cages across the entire spectrum.

70 μm. Fig. 14 plots the average crosstalk suppression for these via spacings at 10 GHz. We found that there is no discernible dependence of isolation effectiveness on via density for via spacings up to 40 μm. At 70-μm via spacing, the degradation in crosstalk suppression is about 10 dB. This is an important result because sparse Faraday cages can be used in order to maintain the mechanical integrity of the substrate without compromising crosstalk suppression.

To determine if other types of Faraday cage structures would improve its performance, we fabricated a double Faraday cage, and a Faraday cage constructed by a discontinuous trench as seen in Fig. 11. The results of the crosstalk measurements are plotted in Fig. 15. The single and double cage and trench perform within about 3 dB overall. This result, together with the via spacing results suggest that a simple cage of sparse substrate vias can significantly reduce crosstalk through the substrate. Further insight into the noise suppression of the Faraday cage can be obtained by deriving a lumped-element equivalent circuit model, which has been presented in [26].

V. Conclusion

We have successfully developed a high-aspect ratio, insulated substrate-via technology in silicon and have used these vias to demonstrate a new Faraday cage isolation scheme for SOC applications. We have demonstrated fully lined and completely filled substrate vias with aspect ratios of 8. Measured inductance of individual vias approaches theoretically expected values. We have used this substrate-via technology to demonstrate a Faraday cage isolation scheme for SOC applications. The Faraday cage improves isolation by 30 dB at 10 GHz and 16 dB at 50 GHz at a distance of 100 μm. The small footprint of the isolation structure and its high isolation effectiveness at short distances allows close packing of mixed-signal circuits.

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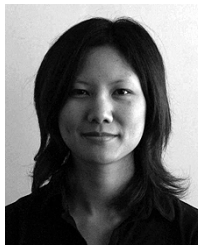

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