An Equivalent Circuit Model
for a Faraday Cage Substrate Crosstalk Isolation Structure

Joyce H. Wu and Jesús A. del Alamo

Massachusetts Institute of Technology, Cambridge, MA 02139, USA

Abstract – **We have developed a physics-based equivalent circuit model for a novel Faraday cage substrate crosstalk isolation structure. This compact isolation approach relies on high-aspect ratio, solid copper substrate vias that are shorted to ground. A cage constructed with these vias can be used to enclose sensitive or noisy portions of a chip and has been proven effective up to 50 GHz. The Faraday cage equivalent-circuit model is based on a well-established substrate crosstalk model with the substrate node shunted to ground through a series inductor-resistor branch that represents the substrate vias. This straightforward approach provides good agreement with the measured data into the millimeter-wave regime for different layouts of the Faraday cage.**
Index Terms – **modeling, substrate noise, crosstalk, isolation**

I. INTRODUCTION

Substrate crosstalk between digital, analog, and RF blocks is a major problem when designing mixed-signal circuits for System-on-Chip (SoC) applications. Suppression of substrate noise is critical to enable single-chip systems that integrate noisy logic or RF power amplifiers with sensitive analog or low-noise RF circuits. Future systems will require densely packed circuits operating at frequencies extending to the millimeter-wave regime where substrate isolation is problematic. Numerous isolation schemes to reduce substrate noise coupling have been proposed and implemented with varying results [1, 2]. In general, traditional schemes based on guard rings or SOI have either a large footprint or become ineffective at high frequencies [1, 3].

A particularly promising approach that is both economic in space and is effective up to mmw frequencies is a Faraday cage embedded in the substrate that surrounds a noisy or sensitive circuit (Fig. 1) [4]. This Faraday cage uses high-aspect ratio, through-wafer vias with a silicon nitride liner and a solid copper core that is shorted at the top and to the ground plane at the back of the wafer [5]. Faraday cages have shown an isolation improvement of 41 dB at 1 GHz, 30 dB at 10 GHz, and 16 dB at 50 GHz for a separation distance of 100 μm when compared to a reference structure [4].

In order to better understand the exceptional performance of this Faraday cage and to provide a tool for system designers to explore its impact on SoC
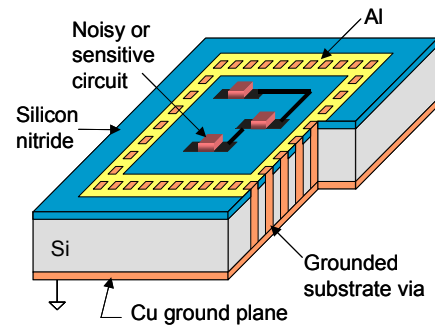

Fig. 1. Schematic diagram of Faraday cage constructed using through-wafer vias. The vias are shorted together to a ground plane at the bottom of the wafer.

applications, we have developed a compact physics-based equivalent circuit model for this structure. The model reveals the origin of the high crosstalk suppression of this structure.

II. EXPERIMENT

The experimental work has been described in detail in [4] and [5]. Substrate isolation was measured between a pad located inside the cage (transmitter) and another outside (receiver) at distances between 100 and 200 μm in a ground-signal-ground configuration (Fig. 2). The transmitter and receiver pads were each 62 μm × 100 μm in area. The substrate was 77-μm thick with a resistivity of 10–20 Ω·cm. The Faraday cage was composed of 10-μm diameter vias with an aspect ratio close to 8. Via spacing in the cage varied from 10 to 70 μm. The variable via spacing of the Faraday cage was evaluated on test structures of a transmission distance of 200 μm. To serve as reference, an identical structure was fabricated without the Faraday cage, but with the same grounded backplane.

Substrate crosstalk isolation was evaluated by measuring S_{21} using an HP8510C network analyzer from 500 MHz to 50 GHz. The lumped-element circuit model for the crosstalk isolation structures was simulated using Agilent Technologies Advanced Design System (ADS) software.
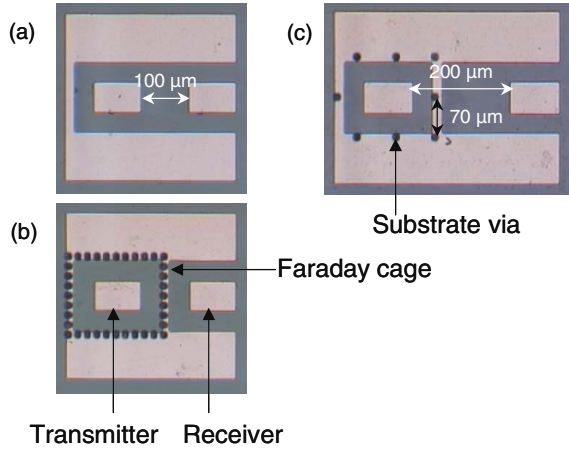
Fig. 2. Die pictures of test structures: (a) reference structure and (b) Faraday cage with 10-µm via spacing at transmitter-receiver separation of 100 µm. (c) Faraday cage structure with 70-µm via spacing and 200-µm pad separation.

Fig. 3. (a) Equivalent circuit model of the reference structure. (b) Equivalent circuit model of the Faraday cage.

III. FARADAY CAGE CIRCUIT MODEL AND RESULTS

The equivalent circuit model of the Faraday cage isolation structure was constructed by first examining the reference test structure. At frequencies below that corresponding to its dielectric relaxation time constant, the silicon substrate behaves as a simple resistor. At higher frequencies, the substrate begins to act as a lossy dielectric, requiring a parallel resistor-capacitor combination [3, 6-8]. A suitable model for the reference structure is therefore one that is similar to the SOI model in [3] and the high-resistivity substrate model in [6] (Fig. 3a). R_r and C_r represent the substrate between the transmitter and receiver. R_3 and C_3 are lumped to represent the substrate from the surface to the backside of the wafer. C_{pad} is the pad capacitance. The model fits better to the measurements if a series resistor, R_2, is added. This perhaps represents the spreading resistance between the pad and the substrate. At a pad separation distance of 100 µm, the S_{21} measured and simulation data for the reference structure match fairly well (Fig. 4).

The Faraday cage model extends from the reference model by adding the ground shunt that is provided by the vias. First, the center R_r–C_r pair is split into identical parallel R_1 and C_1 pairs in series (Fig. 3b). If the split is such that $R_1=R_r/2$ and $C_1=2C_r$, where R_r and C_r are the original reference resistance and capacitance, the simulation results remain unchanged. This split exposes a node in the circuit that represents the substrate in the middle of the transmitter-receiver gap. The effect of the Faraday cage is to shunt this node to ground through the
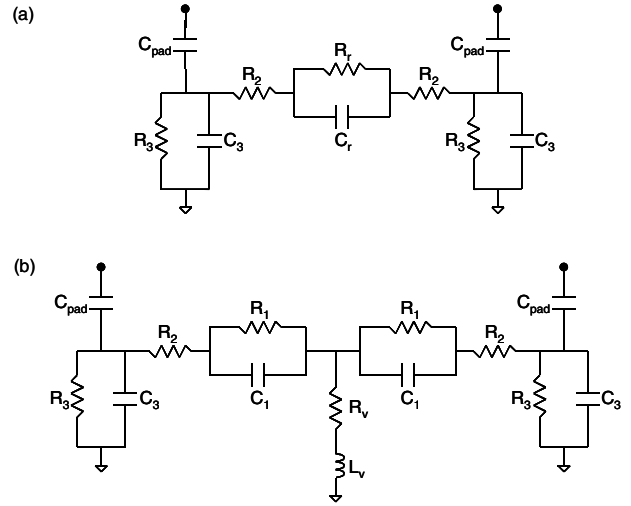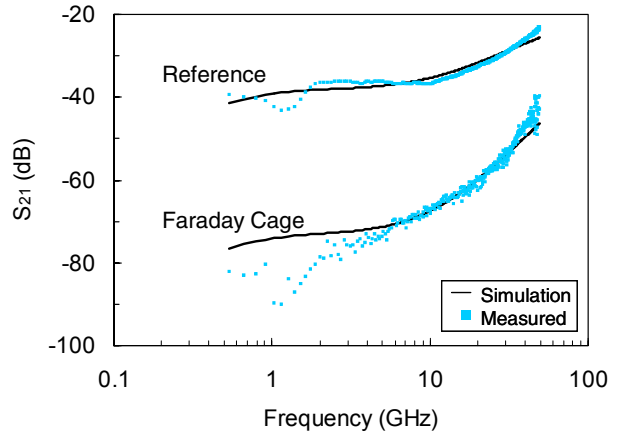

Fig. 4. S_{21} of the reference and Faraday cage at 100-µm pad separation distance.

substrate via. A simple resistor-inductor series branch is a good description of a substrate via up to 50 GHz (Fig. 5). In our proposed Faraday cage model, the entire effect of the Faraday cage is captured by lumped elements R_v and L_v. The smaller R_v and L_v are, the more effective the ground shunting of the substrate between the transmitter and receiver, resulting in a reduction in crosstalk (Fig. 6).

This simple model matches the measured data very well with a set of parameters that remains relatively unchanged from the reference structure (Fig. 4). The lumped-element values used in simulations are listed in Table 1. The range of values that are needed for R_v and L_v are consistent with the measured values extracted in [5] for a single via. The
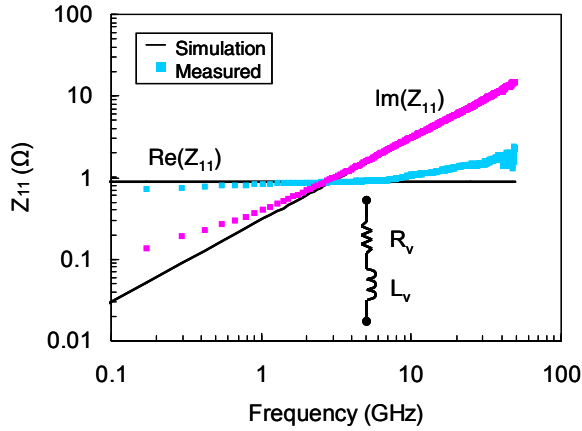
Fig. 5. Real and imaginary parts of Z_{11} for a 4-µm diameter and 77-µm deep substrate via. The solid line plots simulation results of a series R-L equivalent circuit model that matches the measured data well.

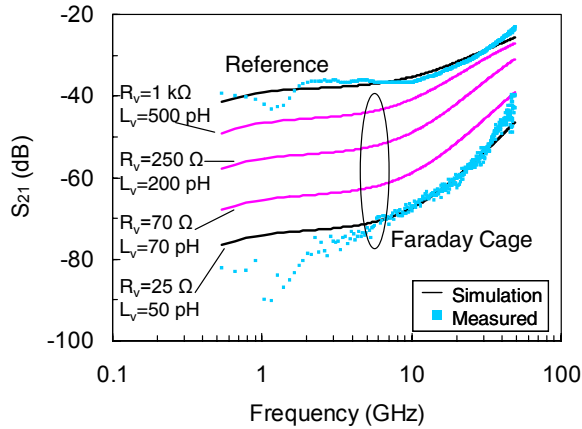Fig. 7. Polar plot of S_{21} of a Faraday cage structure with 100-µm pad separation.

Fig. 6. Simulation of lumped-element model evolving from the reference to the Faraday cage structure at 100-µm pad separation. Only the resistance (R_v) and inductance (L_v) of the cage vias have been changed.

Table 1. Summary of lumped-element values.

	Ref.	Cage	Ref.	Cage	Cage
Tx-Rx separation	100 µm	100 µm	200 µm	200 µm	200 µm
Via spacing	10 µm	10 µm	10 µm	10 µm	70 µm
C_r	3 fF	–	2 fF	–	–
R_r	5 k	–	6.4 k	–	–
C_1	–	6 fF	–	5 fF	5 fF
R_1	–	2.5 k	–	6 k	6 k
R_2	200	200	250	250	250
C_3	17 fF	17 fF	17 fF	17 fF	17 fF
R_3	260	260	260	260	260
R_v	–	25-50	–	20	45-85
L_v	–	10-130 pH	–	30-50 pH	from 30 pH
C_{pad}	1.4 pF	1.4 pF	1.4 pF	1.4 pF	1.4 pF

spread in isolation effectiveness that we observe from sample to sample can be easily accommodated by just varying R_v and L_v in a manner consistent with the spread measured in [5]. This variation in the via inductance and resistance can be attributed to fabrication issues in contacting the via at the surface. The model not only matches the magnitude of S_{21} fairly well but also its real and imaginary components individually (Fig. 7).
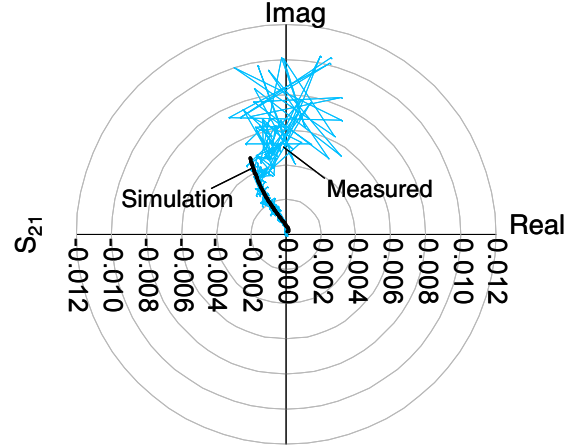
IV. DISCUSSION

Increasing the separation distance between the pads reduces substrate crosstalk. In the reference structure, this can be effectively modeled by increasing R_r and decreasing C_r. Fig. 8 shows the effect of increasing the pad separation to 200 µm. At 200-µm separation, the Faraday cage model also fits the data very well.

Another factor that we have studied is the effect of via spacing of the Faraday cage. The simulation and measured
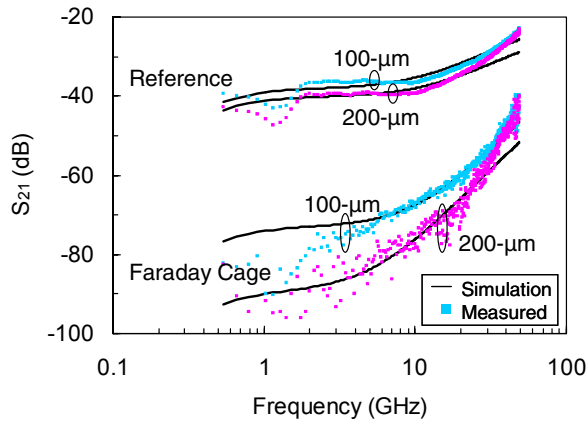
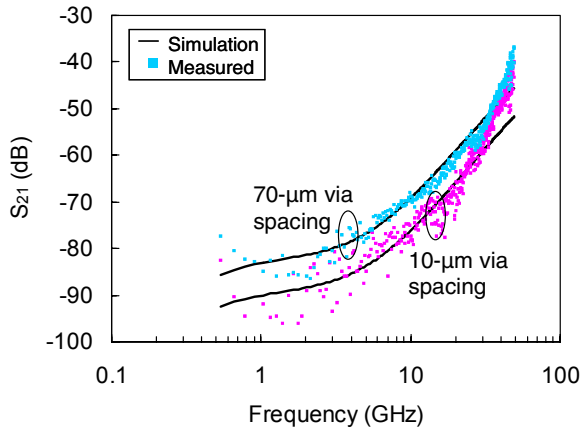Fig. 8. S_{21} of the reference and Faraday cage structures at 100-μm and 200-μm pad separation distance.

Fig. 9. S_{21} of the Faraday cage with 10-μm and 70-μm via spacing at 200-μm pad distance.

data of the Faraday cage at 200-μm pad separation with 10-μm and 70-μm via spacing is shown in Fig. 9. Experimentally, we found that as the spacing between the vias of the cage increases, substrate noise more easily escapes the Faraday cage. The model can explain this result if the effectiveness of the shunt is reduced. This is reasonable since fewer vias are used to shunt the substrate between transmitter and receiver to ground (Fig. 2c). However, even at the greatest via spacing of 70 μm, the loss in noise suppression compared to a 10-μm via spacing is not large, 17 dB at 10 GHz and only 7 dB at 50 GHz (Fig. 9).

V. CONCLUSION

A simple, lumped-element equivalent circuit model for a Faraday cage substrate crosstalk isolation structure has been developed. The model is physically meaningful and matches the experimental data well into the mmw regime. This model will be a useful tool to evaluate the effectiveness of this innovative substrate isolation scheme in actual circuits.

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