RF Power Potential of 90 nm CMOS:
Device Options, Performance, and Reliability

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Abstract

This paper presents the first detailed comparative study of the RF power potential of the various device options offered in a state-of-the-art 90 nm CMOS foundry technology. We show that at a constant voltage of 1 V, the nominal 90 nm thin gate-oxide logic devices offer the best performance, at $V_{dd} = 1$ V and 2.2 GHz showing over 20 dBm of output power and 59% PAE, as well as a power density of 34 mW/mm and 59% PAE at 8 GHz. If the operating voltage can be selected, 250 nm long thick gate-oxide I/O devices offer the highest power and efficiency at 2.5 V. However, when reliability considerations are included, the 90 nm digital devices outperform the 250 nm I/O devices. Overall, we find that the RF power performance of 90 nm CMOS exceeds the requirements for power amplifiers in a large variety of wireless high volume applications.

Introduction

The roadmap for integration of the RF and digital functions on a chip inevitably goes through the 90 nm node, which offers clear advantages for digital CMOS. However, implementing the RF function, particularly RF power amplification, brings unique concerns about performance and reliability. In a modern foundry process, in addition to the nominal digital devices, it is common to offer devices with thicker gate oxides and longer gate lengths for analog and I/O functions. This comes at the cost of increased process complexity. When considering the RF power potential of a deeply scaled CMOS technology generation, it is essential to evaluate the suitability of the entire set of devices from a performance as well as reliability point of view. This is the goal of this work.

There is only one other study of the RF power suitability of 90 nm CMOS that we know of [1]. In that work, a single narrow standard digital device was studied under a limited set of conditions. Our work, in contrast, investigates wider devices and a variety of device types with gate lengths and oxide thicknesses that are commonly available in a foundry process.

Technology

The technology that has been studied in this work is a foundry 90 nm CMOS technology manufactured at IBM. Table 1 shows the available device options. In addition to the standard 90 nm NFET with a nominal gate oxide thickness of 14 Å ($V_{dd} = 1.0$ V), there is an intermediate oxide I/O FET ($t_{ox} = 22$ Å) equivalent to the 130 nm node ($V_{dd} = 1.2$ V), and a thick oxide I/O FET ($t_{ox} = 51$ Å) equivalent to the 250 nm node ($V_{dd} = 2.5$ V). Additional combinations of these gate oxide thicknesses and gate lengths are available. Depending on the process details, the additional mask count required to offer these device options is between 1 and 3. In this paper, L_g will always refer to the node's gate length (rather than the poly-silicon or printed gate length).

	Oxide Thickness		
	thin (nominal) (14 Å)	medium (22 Å)	thick (51 Å)
Nominal V_{dd}	1.0 V	1.2 V	2.5 V
Addl. Mask	0	1 to 3	1 to 3
$L_g = 90$ nm	48 x 16 µm	n/a	n/a
$L_g = 130$ nm	34 x 16 µm	34 x 16 µm	n/a
$L_g = 250$ nm	30 x 20 µm	30 x 20 µm	30 x 20 µm

Table 1: Measured devices and their sizes (number of fingers x unit finger width). Sizes have been chosen to give identical drive current for the 90 nm thin-, 130 nm medium-, and 250 nm thick-oxide devices.

Results: RF Power Performance of 90 nm Logic Device

RF power characterization was carried out at 2.2 GHz on an ATN load-pull system and at 8 GHz on a Maury system. Input and output impedance matching conditions were selected to yield optimum power-added efficiency (PAE). We chose 8 GHz for the bulk of our work in order to avoid device oscillations and to explore the high-frequency potential of deeply scaled CMOS technologies. Additionally, S-parameter measurements were performed up to 80 GHz.
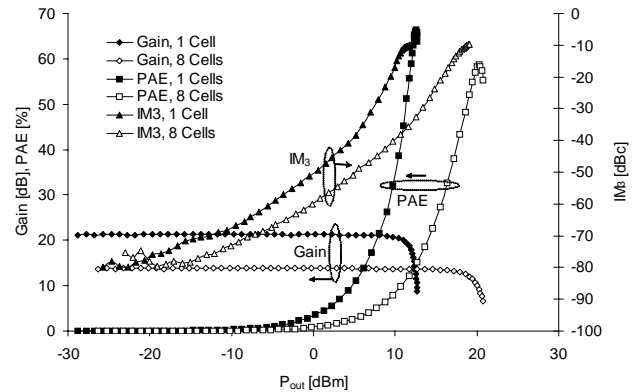

Fig. 1: Power performance at 2.2 GHz of a thin-oxide 90 nm device (48x16 µm) and a device array (8 cells of 48x16 µm each), both biased at $V_{dd} = 1$ V, $I_d = 32.6$ mA/mm. Impedances were optimized for the best linearity-efficiency tradeoff.

The 2.2 GHz power performance of standard digital 90 nm devices of two different total gate widths is shown in Fig. 1, and summarized in Table 2. For a 48x16 µm cell, a peak PAE in class AB operation of about 66% is obtained at an output power of 12.7 dBm. When connecting 8 device cells in parallel, we have achieved a peak PAE of 59% at an

output power of 20.2 dBm, indicating a good scaling of P_{out} with cell count. The PAE at a linearity (in terms of IM_3) of -35 dBc is 14% and 12% for the 48x16 µm device and the 8x48x16 µm device, respectively.

To put these results in context, a WCDMA PA driver requires about 14 dBm of 1 dB compression power, with an OIP_3 of 24 dBm [2]. From Table 2 we see that the 8x48x16 µm device exceeds these requirements by a safe margin. The results of Table 2 suggest that 90 nm CMOS is quite suitable for a wide range of integrated PA applications, such as WLANs, bluetooth and cellular PA drivers, giving acceptable efficiency at linear operation.

Measurements at 8 GHz for the standard 90 nm thin-oxide device at $V_{dd} = 1$ V are shown in Fig. 2. The device achieves a peak PAE of 56.8% at 13.4 dBm output power with an associated gain of 14.6 dB. Across-wafer measurement uniformity for the 90 nm devices, including probing uncertainty, is shown in Table 3. Excellent uniformity is seen across the entire 8" wafer.
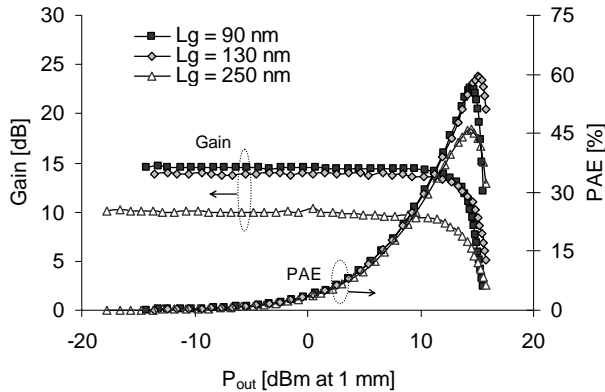

Fig. 2: Power sweep for thin oxide devices with different values of L_g at $V_{dd} = 1$ V. For very short devices, increasing L_g results in a softer compression that pushes the peak PAE point out.

Device	48x16 µm	8 cells of 48x16 µm
Bias	$V_{dd} = 1$ V $I_d = 25$ mA	$V_{dd} = 1$ V $I_d = 200$ mA
Frequency	2.2 GHz	2.2 GHz
Peak PAE	66 %	59 %
P_{out} at peak PAE	12.5 dBm	20.2 dBm
Small signal gain	21.2 dB	14 dB
OIP_3	25 dBm	30 dBm
PAE at IM_3=-35dBc	14 %	12 %
P_{out} at IM_3=-35dBc	6 dBm	12 dBm
P_{out} at 1 dB compression	11 dBm	18 dBm

Table 2: Performance comparison of the standard 90 nm device and a parallel combination of 8 standard devices. Impedances were optimized for the best linearity-efficiency tradeoff.

	Peak PAE	Peak P_{out}	Small Signal Gain
Average	59.3 %	14.2 dBm	16.3 dB
Std. Dev.	0.6 %	0.1 dB	0.3 dB

Table 3: Statistics on power data for 18 sites across an entire 8" wafer. Measurement done with constant impedances, input power and bias point ($V_{dd} = 1$V, $I_d = 26$ mA/mm) at 8 GHz. Data include both the probe contact uncertainty as well as the device variation across the wafer. Device geometry used was 96x8 µm.

Results: RF Power Performance of Other Device Options

The performance of thin-oxide devices with longer gates is also shown in Fig. 2. In comparison to the 90 nm device, the 130 nm device offers a slightly higher PAE of 59.5% at an output power of 12.4 dBm, but the associated gain drops to 13.9 dB. The 250 nm device is clearly inferior.

Figs. 3 and 4 compare in detail the peak PAE power performance of the thin oxide devices for the three different gate lengths, as a function of V_{dd} ($I_d = 26$ mA/mm). Fig. 3 shows the small signal gain, the peak PAE and the corresponding output power density as a function of V_{dd}. Fig. 4 looks at these results by showing the peak PAE as a function of the output power density at peak PAE, with V_{dd} as parameter. As seen in Figs. 3 and 4, there is not much difference between the 90 nm and the 130 nm devices, while the 250 nm device gives much lower performance.

Figs. 5 and 6 show the impact of gate oxide thickness, keeping L_g constant at 250 nm. Decreasing the oxide thickness results in lower gain and efficiency. However, the power density for a given V_{dd} is increasing slightly.

Finally, Figs. 7 and 8 show the performance when we both scale oxide thickness and L_g. Both the 250 nm I/O devices and the 90 nm digital devices reach comparable levels of peak PAE and gain. However, the use of a thicker oxide allows higher power levels for the 250 nm device. The performance obtained in the 250 nm I/O device is better than reports available in the literature [3].

In order to understand the physical origin of the results shown in Figs. 2-8, we have measured f_{max} for all these devices at nominal V_{dd} and at $I_d = 26$ mA/mm. This is graphed in Fig. 9. The f_{max} of the large power 90 nm and 130 nm thin oxide devices is identical, in good agreement with the RF power data of Figs. 3 and 4. Interestingly, the f_{max} of the 250-nm thick-oxide device is comparable to the 90 nm and 130 nm devices with thin oxides. This is also consistent with the power data of Figs. 3-8. The values here are relatively low because the bias point is not optimal for f_{max}, and because additional parasitics such as R_g and back-end C_{gd} penalize very wide devices. For comparison, the f_{max} of typical small analog devices is also shown. These are characteristic of state-of-the-art 90 nm technology.

The optimum device choice for RF power applications depends on the system design constraints. If an optimum voltage can be used, Fig. 8 suggests that the thick oxide 250 nm device operating at higher voltages delivers a higher output power density than any of the thin-oxide devices, while operating with an identical peak efficiency. However, if the application is to use a single bias point for all its subsystems, the $V_{dd} = 1$ V that is dictated by the digital circuitry implies that the 90 or 130 nm thin oxide devices are preferable. This can be seen in Figs. 3, 5, and 7. For low voltage operation, the thin oxide devices are preferable because their lower knee voltage leads to a higher peak PAE.
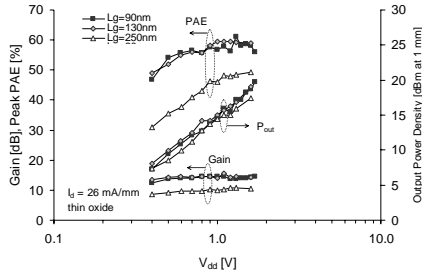
Fig. 3: Gain, PAE and output power density at peak PAE point as a function of V_{dd} for thin oxide devices of three different gate lengths. Impedances and input power drive were re-optimized at each V_{dd} for each device.
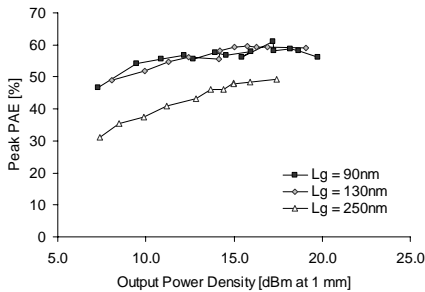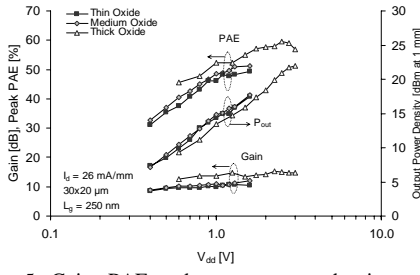

Fig. 5: Gain, PAE and output power density at peak PAE as a function of V_{dd} for 250 nm devices with three different gate oxide thicknesses. Impedances and input power drive were re-optimized at each V_{dd} for each device.
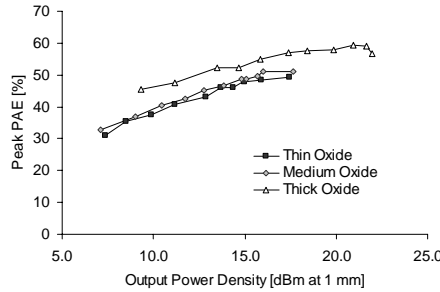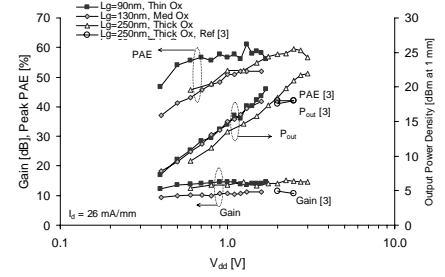

Fig. 7: Gain, PAE and output power density at peak PAE point as a function of V_{dd} when scaling both L_g and gate oxide thickness. Impedances and input power drive were re-optimized at each V_{dd} for each device.
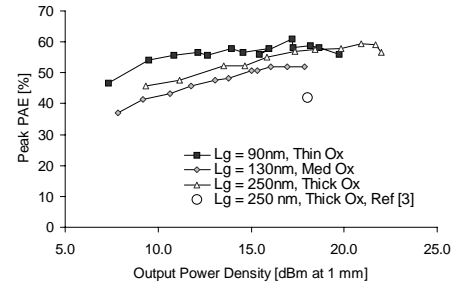

Fig. 4: PAE as a function of output power density at peak PAE for thin-oxide devices of three different gate lengths. The different data points correspond to different values of V_{dd}.

Fig. 6: PAE as a function of output power density for peak PAE point for 250 nm devices with three different gate oxide thicknesses.

Fig. 8: PAE as a function of output power density at peak PAE point when scaling both L_g and gate oxide thickness.

Results: Reliability

Reliability is as important as performance in evaluating a technology for power applications. In a design environment in which one can select an optimum voltage for the PA, it is fair to ask if the improved RF power performance of the 90 nm devices can make up for the expected reduced reliability.

As the bias voltage is increased, large voltage excursions under high output RF power conditions may yield to problems with gate oxide integrity and hot electrons. Under significant power compression, the drain voltage can reach 2 to 3 times V_{dd} and it can approach or exceed the off-state breakdown voltage of the device. Fig. 10 compares the measured BV_{off} for all available devices. This was measured with the device biased at $V_{gs} = V_t$ (defined as 1 mA/mm at $V_{nominal}$), and sweeping V_{ds} until avalanche in I_d destroyed the device. Interestingly, BV_{off} exceeds $V_{nominal} = 1$ V in the thin-oxide devices by more than a factor of three. In contrast, BV_{off} is only about a factor of two higher than $V_{nominal} = 2.5$ V in the thick-oxide device. This is consistent with data in the literature [3].

The relationship between BV_{off} and $V_{nominal}$ in the various devices suggests that biased at $V_{nominal}$ and under strong power compression, the 90 nm device might actually be more reliable than the 250 nm device. This indeed is observed in reliability measurements shown in Fig. 11. This graph plots the mean-time-to-failure defined as the time for the gain to drop by 0.2 dB in devices powered at the peak PAE point for

extended periods of time for different values of V_{dd}. This decrease in gain is equivalent to reducing the PAE to 95% of its initial value, and is a rather conservative limit.

As Fig. 11 shows, at a fixed voltage, the reliability of the 250 nm technology is clearly superior to that of the 90 nm technology, as expected. However, if we now compare the expected reliability of these two technologies at $V_{nominal}$, the 90 nm devices have a reliability that is improved by 2 to 3 orders of magnitude (depending on how one extrapolates from the limited data set). A straight line extrapolation leads to 200 hours for 90 nm at $V_{nominal}$, compared to less than 0.1 hours for the 250 nm thick oxide device.

An alternative way to consider this issue is by comparing device performance at identical levels of reliability. For an identical mean-time-to-failure of 4.0 hours, the 90 nm device operates at $V_{dd} = 1.3$ V and has a peak PAE of 58% at a $P_{out} = 16.8$ dBm (for 1 mm of width). In contrast, the 250 nm device must operate at $V_{dd} = 1.6$ V and yields an inferior performance with a peak PAE of 55.8% at a P_{out} of 15.6 dBm (for 1 mm of width). Since the two lines in Fig. 11 tend to converge as V_{dd} is reduced, for an equivalent level of reliability, the performance of the 90 nm device is superior to that of the 250 nm device.

The fact that the two lines in Fig. 11 are not parallel may suggest two different degradation mechanisms, gate oxide and hot electron damage. Evidence that this might be taking place comes from the observation of an increasing gate leakage current with stressing time in the 90 nm devices,

while no measurable gate leakage current was ever seen in the 250 nm devices.

It is important to realize that the mean-time-to-failure of Fig. 11 is rather short because we have selected very harsh conditions. Under more realistic conditions, the reliability improves substantially. In linear applications, backing off from the peak PAE improves reliability very quickly, as shown in Fig. 12. Here, the mean-time-to-failure is shown as a function of gain compression. As gain compression is backed off, the reliability improves rapidly but the PAE drops, as is well known.

Conclusions

We have studied the RF power suitability of the device options offered in a typical 90 nm digital CMOS foundry process. We have demonstrated excellent performance at 2.2 and 8 GHz. We have found that, reliability considerations aside, at a constant voltage of 1 V, 90 nm nominal devices offer the best performance, but 130 nm thin-oxide devices
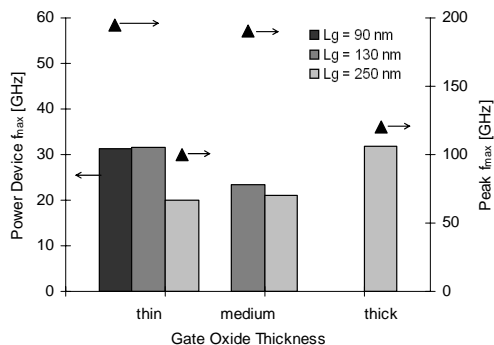
closely match it. If one allows for optimum voltage selection, the 250 nm thick-oxide devices offer the highest output power and efficiency at the highest voltages. On the other hand, when consideration is given to device reliability, the 90 nm thin-oxide digital devices outperform thick-oxide 250 nm I/O devices.

Acknowledgements

References
[1] M. Ferndahl, et al., Microwave and Wireless Components Letters, IEEE, Volume: 13, Issue: 12, Dec. 2003, pp. 523 – 525
[2] RF2681, preliminary product data sheet, RF Micro Devices, Rev A8 040512, pp. 529 – 536
[3] E. Chen, et al., IEEE RAWCON, 2000, pp. 163 – 166

Fig. 9: Comparison of f_{max} for the devices in Table 1 operating at $V_{nominal}$. The technology (right axis) offers a peak f_{max} of 100 to 200 GHz. The f_{max} of the power devices (left axis) used in this paper is much lower due to the low class AB bias (I_d = 26 mA/mm) and the parasitics associated with the large number of fingers and their width (e.g. R_g and C_{gd}). The f_{max} for power devices is not de-embedded, unlike the peak f_{max} data, and includes the back-end and pads.
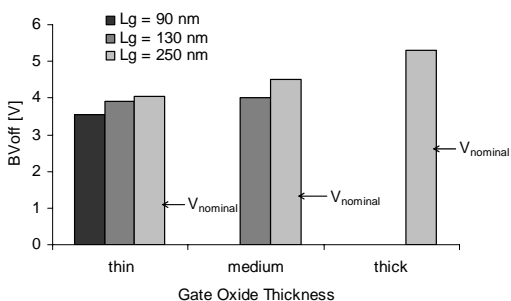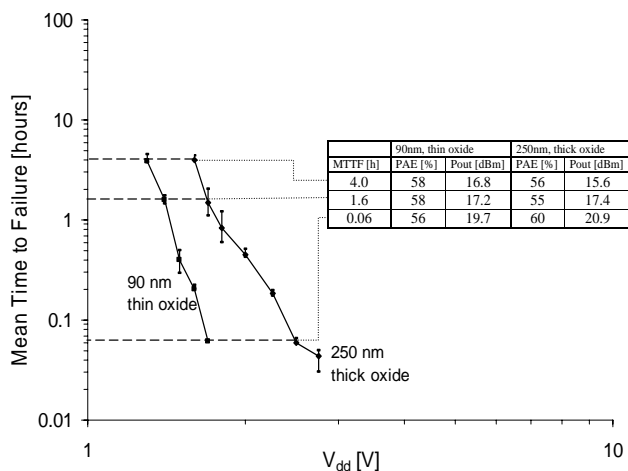

Fig. 11: Mean-time-to-failure (defined as time for the gain to drop by 0.2 dB) as a function of V_{dd} for 90 nm and 250 nm devices. Upper and lower bounds of the time extraction are shown by the vertical bars. The table shows performance figures (PAE and P_{out}) for three different levels of constant MTTF. At higher values of MTTF, the 90 nm device outperforms the 250 nm device.
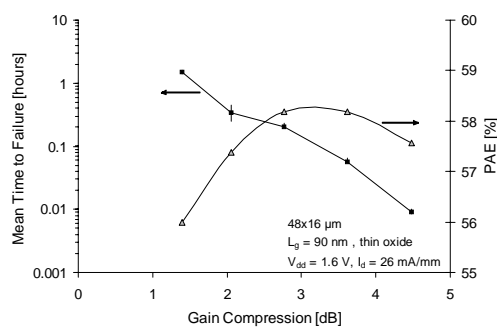

Fig. 10: Breakdown voltage (at I_d = 1 mA/mm) due to impact ionization for the various device designs. Also indicated is the nominal voltage for each gate oxide.

Fig 12: Mean-time-to-failure of the 90 nm thin oxide device as a function of gain compression (power) at V_{dd} = 1.6 V. Also shown is the PAE. Upper and lower bounds of the time extraction are shown by the vertical bars. The relatively short value of MTTF is explained by the aggressive choice of V_{dd}.