Hydrogen-Induced Changes in the Breakdown Voltage of InP HEMTs

Roxann R. Blanchard, Jesús A. del Alamo, and Albert Cornet Calveras

***Abstract*—In this work, electrical measurements show that the breakdown voltage, $\mathrm{BV_{DG}}$, of InP HEMTs increases following exposure to H_2. This $\mathrm{BV_{DG}}$ shift is nonrecoverable. The increase in $\mathrm{BV_{DG}}$ is found to be due to a decrease in the carrier concentration in the extrinsic portion of the device. We provide evidence that H_2 reacts with the exposed InAlAs surface in the extrinsic region next to the gate, changing the underlying carrier concentration. Hall measurements of capped and uncapped HEMT samples show that the decrease in sheet carrier concentration can be attributed to a modification of the exposed InAlAs surface. Consistent with this, XPS experiments on uncapped heterostructures give evidence of As loss from the InAlAs surface upon exposure to hydrogen.**

***Index Terms*—Electric breakdown, hydrogen, indium compounds, MODFETs, surfaces, X-ray spectroscopy.**

I. Introduction

HYDROGEN degradation of III-V FETs is a serious and well-documented reliability concern [1]–[6]. Exposure occurs when hydrogen out-gasses from packaging material and gets trapped inside hermetically sealed packages. Over time, hydrogen causes changes in device characteristics that can ultimately lead to parametric module failures. Compared with more extensive studies of H_2 degradation of GaAs MESFETs and PHEMTs [3]–[6], only limited data on the H_2 sensitivity of InP HEMTs is available [1], [2], [5]. To our knowledge, a device-level solution to this problem has not been reported for either InP or GaAs technologies.

Previous work on the effects of H_2 exposure has focused primarily on the changes in the device threshold voltage, V_T, and transconductance, g_m [2]–[6]. These device parameters are governed mainly by the physics in the intrinsic region of the device, which is the area directly beneath the gate. In this work, we report that in addition to this, hydrogen also affects the extrinsic region, the area outside of the gate, and in a manner that is very different from the intrinsic region. We show that the interaction of H_2 with exposed InAlAs in the gate recess region leads to a decrease in the extrinsic sheet carrier concentration, $n_{s,\mathrm{ext}}$, causing an increase in the device gate-to-drain breakdown voltage, $\mathrm{BV_{DG}}$. Unlike V_T and g_m, the change in $\mathrm{BV_{DG}}$ is nonrecoverable. These results are consistent with similar experiments reported in AlGaAs/GaAs HEMTs [7].

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II. Experimental

The InP HEMTs used for this study were fabricated at MIT. The device heterostructure consists of: semi-insulating InP substrate, 2500 Å InAlAs, bottom δ-doping, 50 Å InAlAs spacer, 200 Å InGaAs channel, 20 Å InAlAs spacer, top δ-doping, 270 Å InAlAs pseudo-insulator, and a 70 Å undoped InGaAs cap. The fabrication process features a selective cap recess, sidewall recess isolation, dielectric-assisted lift-off, Ni/AuGe/Ni alloyed ohmic contacts, ECR-enhanced, low-temperature Si_3N_4 passivation and Ti/Pt/Au gate metallization. The devices used in this study have gate lengths from 0.6 μm to 10 μm, and gate orientations along the [011], [010], and [01$\bar{1}$] directions on a (100) substrate.

Hydrogen exposure and characterization measurements were made in a temperature-controlled wafer probe station equipped with a sealed chamber allowing the introduction of N_2 or forming-gas (5% H_2 in N_2). All devices underwent a thermal burn-in at 230 °C in N_2 until no further changes in threshold voltage, ΔV_T, were observed. The devices were then annealed unbiased at 200 °C for 3 hours in forming-gas. For reference, selected burned-in devices were also annealed in N_2. A detailed room-temperature characterization was performed pre-anneal and post-anneal. To monitor degradation in the extrinsic portion of the device, $\mathrm{BV_{DG}}$ was measured using the drain-current-injection technique [8]. The breakdown voltage was defined at $I_G = 1$ mA/mm.

Following H_2 degradation exposure, some devices underwent a subsequent recovery anneal in pure N_2 at 200 °C for up to 24 hours. This recovery anneal is designed to see if H_2 degradation can be annealed out with further thermal processing in pure N_2. Recovery behavior has been frequently reported following H_2 degradation [1], [4], [5]. $\mathrm{BV_{DG}}$ was also measured at room temperature following the N_2 recovery anneal.

The behavior of V_T in these devices as a result of similar hydrogen exposure and follow-on recovery anneals has been described in [2].

III. Results

Before annealing, the breakdown voltage of these devices was approximately 6.7 V. After annealing in forming-gas at 200 °C for 3 hours, $\mathrm{BV_{DG}}$ increased on average 0.9 V for all devices, as shown in Fig. 1. $\Delta\mathrm{BV_{DG}}$ showed no L_G or orientation dependence, in contrast to the ΔV_T behavior observed on the same devices [2]. The control devices annealed in N_2 showed no $\mathrm{BV_{DG}}$

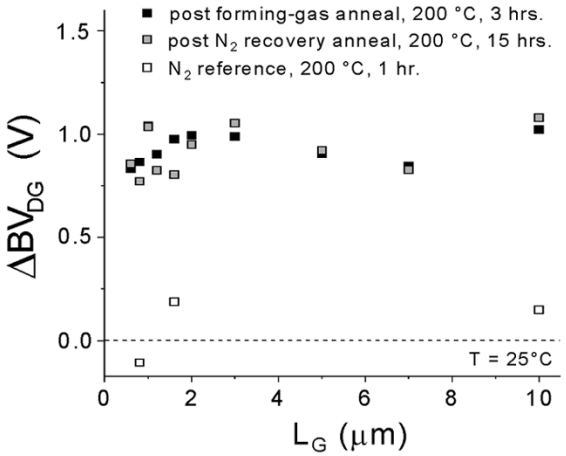

Fig. 1. Black squares show change in $\mathrm{BV_{DG}}$ after exposure to forming-gas (5% $\mathrm{H_2}$ in $\mathrm{N_2}$). There is no L_G dependence, nor was there any orientation dependence in $\Delta\mathrm{BV_{DG}}$. Data in the gray squares show that the increase in $\mathrm{BV_{DG}}$ does not recover with further annealing in $\mathrm{N_2}$ following the forming-gas degradation anneal. All measurements at room temperature.

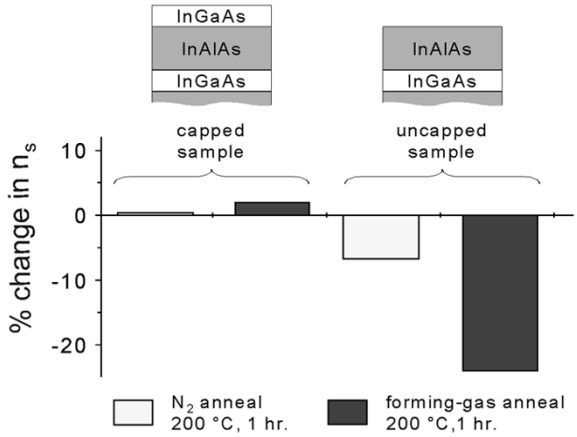

Fig. 2. Hall measurements showing the change in n_s on capped and uncapped HEMT heterostructures. There is no change in n_s for the capped samples after annealing in either $\mathrm{N_2}$ or forming-gas. In contrast, the uncapped samples in which the InAlAs layer is exposed show an n_s decrease of $>20\%$ after annealing in forming-gas, compared to $<10\%$ for the $\mathrm{N_2}$ annealed samples. This rules out donor passivation as the cause of the reduction in n_s due to $\mathrm{H_2}$ exposure.

increase. The total change in $\mathrm{BV_{DG}}$ for samples that additionally underwent a subsequent recovery anneal in $\mathrm{N_2}$ for 15 hours at 200 °C is also shown in Fig. 1. As seen in Fig. 1, $\mathrm{BV_{DG}}$ does not recover with further $\mathrm{N_2}$ annealing. All these results are consistent with similar experiments reported in AlGaAs/GaAs HEMTs [7]. Devices without $\mathrm{Si_3N_4}$ passivation were also fabricated and underwent identical experiments. They were found to behave in a similar way.

The increase in $\mathrm{BV_{DG}}$ could be explained with either an increase in the gate Schottky barrier height, ϕ_B, or a decrease in $n_{s,\mathrm{ext}}$ [9]. To produce a 0.9 V increase in $\mathrm{BV_{DG}}$, ϕ_B must increase by nearly 15 meV [9]. This is inconsistent with the *negative* threshold voltage shift observed on the same devices following $\mathrm{H_2}$ exposure [2]. It is also inconsistent with the fact that ΔV_T was found to recover with further $\mathrm{N_2}$ annealing while $\Delta\mathrm{BV_{DG}}$ did not. Therefore, the increase in $\mathrm{BV_{DG}}$ is a result of a reduction in $n_{s,\mathrm{ext}}$.

The reduction of $n_{s,\mathrm{ext}}$ required to realize the increase in $\mathrm{BV_{DG}}$ could occur through donor passivation [3], through changes in the surface in the extrinsic region [10], [11], or through stress-induced piezoelectric charges in the extrinsic region [1], [2]. Previous work has shown that exposure to $\mathrm{H_2}$ leads to compressive stress in Ti/Pt/Au gates due to the formation of $\mathrm{TiH_x}$ [1], [2] and the creation of a piezoelectric volume charge distribution in the device. Piezoelectric charge is ruled out here as the main cause of the $n_{s,\mathrm{ext}}$ decrease because there is no orientation dependence to $\Delta\mathrm{BV_{DG}}$.

To determine if the decrease in $n_{s,\mathrm{ext}}$ is due to donor passivation or due to changes in the surface stoichiometry, we have directly measured n_s on Hall measurement samples prepared from the same wafer used to fabricate the transistors. One set of samples retained the InGaAs capping layer. In a second set of samples, the InGaAs capping layer was selectively etched off, exposing the InAlAs insulating layer. An etching process identical to the one used in device fabrication was followed. Hall measurements were performed at room temperature before and after annealing the samples in either $\mathrm{N_2}$ or forming-gas at 200 °C for 1 hour.

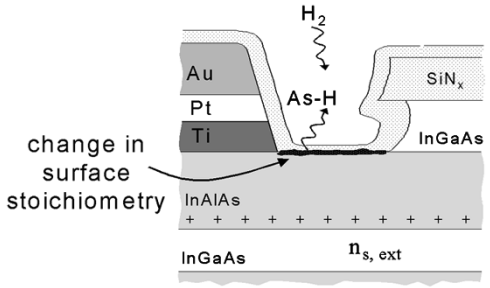

Fig. 3. Cross section of a typical InP HEMT, focusing on the gate region at the drain end of the device. This diagram depicts the proposed mechanism for explaining the reduction of $n_{s,\mathrm{ext}}$ after exposure to $\mathrm{H_2}$. $\mathrm{H_2}$ reacts with the exposed InAlAs surface and modifies its stoichiometry. This changes the Fermi pinning position at the surface or creates trap states that become subsequently occupied. The end result is a reduction in the sheet carrier concentration in the InGaAs layer underneath.

The results of this experiment are shown in Fig. 2. There was no change in the n_s for the capped samples under either annealing condition. For the uncapped samples, there was a $>20\%$ decrease in n_s following the forming-gas anneal. The uncapped samples annealed in $\mathrm{N_2}$ showed a decrease in n_s of less than 10%. Since it is unlikely that the InGaAs cap is a significant barrier to hydrogen diffusion, this experiment allows us to rule out donor passivation as the source of the n_s reduction in the extrinsic region.

We therefore postulate that changes in the surface potential of the InAlAs layer are responsible for the reduction in $n_{s,\mathrm{ext}}$. Some InAlAs is inevitably exposed when part of the InGaAs cap layer is removed so that the gate may directly contact the InAlAs. This is known as the gate-recess region and is illustrated in Fig. 3. A change in the surface potential of the exposed InAlAs could come about through As desorption, leaving behind a cation rich surface [10]. This mechanism can reduce $n_{s,\mathrm{ext}}$ by changing the Fermi level pinning position at the surface [11] or by creating trap states that become subsequently occupied [7].

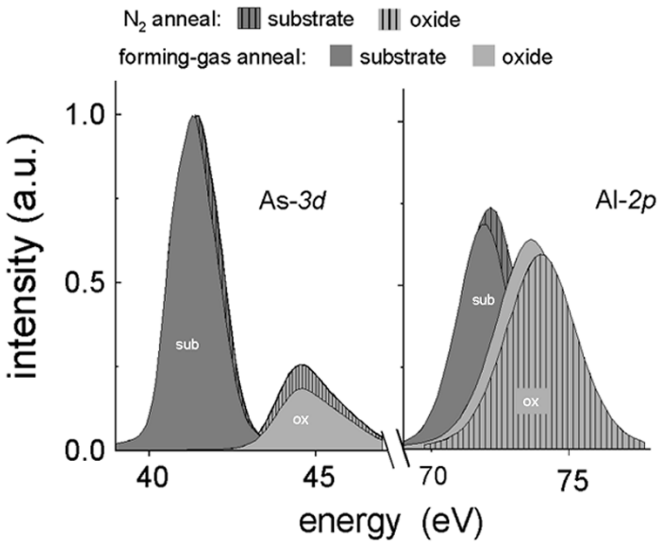

Fig. 4. XPS results comparing uncapped HEMT samples annealed in either N_2 or forming-gas. The As-3d data are presented on the left, and show that the As(oxide)/As(substrate) ratio decreases after the forming-gas anneal, relative to the N_2 control sample. In contrast, the Al-2p core level spectra on the right show that the Al(oxide)/Al(substrate) peak ratio increases after the forming-gas anneal, relative to the N_2 control sample. These results are evidence showing that exposure to H_2 causes As loss from the InAlAs native oxide. Composite peaks have been deconvolved into their respective oxide and substrate components. All values have been normalized to the peak composite value.

In order to verify this hypothesis, we have performed XPS measurements on uncapped heterostructures nearly identical to those used in the transistor and Hall measurements. The samples were annealed for 1 hour in either N_2 or forming-gas at 200 °C. Selected samples also underwent a subsequent N_2 recovery anneal following the H_2 degradation anneal. The Al-2p and As-3d core level spectra were examined (the results examining In$-3d$ spectra were inconclusive since the In_2O_3 and InAs bonding energies are too close to be distinguished). The composite peaks were deconvolved into their respective substrate and native-oxide components. All values were then normalized to the peak composite value. The results are shown in Fig. 4.

Examining the As-3d spectra on the left in Fig. 4, we see that the sample annealed in forming-gas showed a 28% decrease in the As(oxide)/As(substrate) total integrated area ratio compared to the N_2 control sample. This indicates that the relative amount of As_2O_3 at the surface *decreased* for the sample annealed in forming-gas, compared to the sample annealed in N_2. In contrast, the Al(oxide)/Al(substrate) area ratio for the sample annealed in forming-gas increased by 13% compared to the N_2 control sample, as shown on the right in Fig. 4. This indicates that relative amount of Al_2O_3 at the surface *increased* for the sample annealed in forming-gas, compared to the sample annealed in N_2.

Fig. 5 is a bar graph comparing the changes in the Al(oxide)/Al(substrate) and As(oxide)/As(substrate) area ratios of samples annealed in forming-gas and a sample that underwent a subsequent N_2 recovery anneal. Both are relative to their respective N_2 control samples. These results show that the InAlAs surface degradation does not recover after further

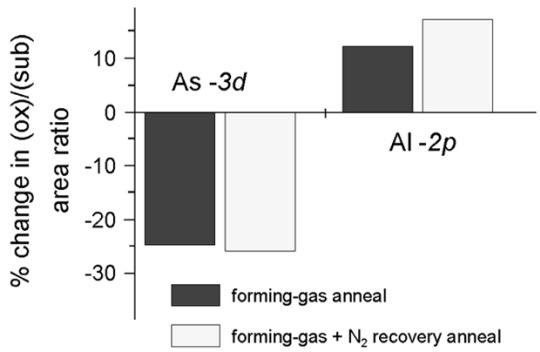

Fig. 5. Bar graph summarizing the results of XPS measurements of the InAlAs surface after the forming-gas anneal, and after a subsequent recovery anneal in pure N_2 at 200 °C for 15 hours. All numbers are relative to the N_2 control sample. The loss of As from the InAlAs surface does not recover following further annealing in N_2, consistent with the $\mathrm{BV_{DG}}$ measurements.

annealing in N_2, consistent with our electrical measurements of $\mathrm{BV_{DG}}$.

The decrease in the As(oxide)/As(substrate) ratio observed in XPS is evidence of As loss from the native oxide of InAlAs after exposure to H_2. Similar results have been observed on AlGaAs surfaces [10]. As postulated in [10], the adsorption of H onto the oxidized semiconductor can lead to the formation of volatile AsH_3 with H_2O as a byproduct [10], [12]. The volatile AsH_3 desorbs, leaving H_2O on the surface [11].

Physisorbed H_2O on InGaAs substrates has been shown to lead to additional cation oxidation and further AsH_3 desorption [10], [12]. In the case of InAlAs surfaces, physisorbed H_2O could result in the formation of additional Al_2O_3 or In_2O_3. However, the heat of formation of Al_2O_3 is -400 kcal/mol, making it significantly more stable that either In_2O_3 (-222 kcal/mol) or As_2O_3 (-156 kcal/mol) [13]. It therefore seems reasonable that Al oxidizes preferentially, which is consistent with our XPS observation of an increase in the Al(oxide)/Al(substrate) peak ratio.

A possible consequence of the removal of As from the InAlAs surface is a modification in the surface stoichiometry. This could change the surface Fermi-pinning position or result in trap states that can subsequently become occupied by electrons. Both would be consistent with a reduction in n_s [7], [11]. Moreover, this phenomenon is logically not recoverable, consistent with both the XPS and electrical experiments.

IV. Conclusion

Electrical measurements show the breakdown voltage of InP HEMTs increases following exposure to H_2. The increase in $\mathrm{BV_{DG}}$ is due to a decrease in the carrier concentration in the extrinsic portion of the device. We provide evidence that H_2 reacts with the exposed InAlAs surface in the extrinsic region of the HEMTs right next to the gate, affecting the underlying carrier concentration. Hall measurements of capped and uncapped HEMT samples show that the decrease in $n_{\mathrm{s,ext}}$ can be attributed to changes in the exposed InAlAs surface. XPS experiments on uncapped heterostructures provide evidence of unrecoverable As loss from the exposed InAlAs surface upon hydrogen exposure.

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