Excess OFF-State Current in InGaAs FinFETs: Physics of the Parasitic Bipolar Effect

Xin Zhao, *Member, IEEE*, Alon Vardi, *Member, IEEE*, and Jesús A. del Alamo, *Fellow, IEEE*

***Abstract*— InGaAs FinFETs are challenged by relatively high leakage current in the OFF state. This originates from band-to-band tunneling (BTBT) at the drain end of the channel that is amplified by a parasitic bipolar effect (PBE) as a result of its floating body. In this paper, we present a simple model of the PBE in InGaAs FinFETs, which captures the key gate length and fin width dependences. Our model accounts for surface recombination at the sidewalls of the fin as well as bulk recombination at the heavily doped source. When compared with experimental results, our model suggests that fin sidewall recombination dominates in long gate length transistors and leads to an exponential gate length dependence of the current gain on the parasitic bipolar junction transistor (BJT). The model enables the extraction of the carrier diffusion length which exhibits the predicted fin width dependence. For short gate length transistors, source recombination is shown to dominate and the parasitic bipolar gain scales with the inverse of the gate length.**

***Index Terms*— FinFETs, GIDL, III–V, parasitic bipolar effect (PBE), self-aligned, tunneling.**

I. Introduction

InGaAs is a promising channel material candidate for CMOS technologies beyond the 7 nm node [1], [2]. In these dimensions, only high aspect-ratio 3-D transistors with a fin or nanowire configiuration can deliver the necessary performance while suppressing short-channel effects. Recently, impressive InGaAs FinFET [3]–[11] prototypes have been demonstrated.

A pressing concern with this device technology is the excessive OFF-state current that is often observed [12]–[18] and that is believed to be a consequence of the narrow bandgap of the channel [12]. Its origin has been attributed to band-to-band tunneling (BTBT) at the drain-end of the channel that is amplified by a parasitic bipolar junction transistor (BJT) formed by the source, drain, and floating body of the MOSFET.

Both BTBT and the parasitic bipolar effect (PBE) have been extensively studied in Si MOS transistors [19]–[21]. The physical origin of BTBT is a direct tunneling process at the drain edge of the channel [19], [20]. With the gate voltage below the threshold and a high drain voltage, a high electric-field appears at the drain-end of the channel that results in valence electrons in the channel tunneling to the conduction band in the drain. In floating-body SOI MOSFETs [19]–[21], PBE was identified as a mechanism that amplifies BTBT or an impact ionization current generated by the high gate-to-drain electric field.

An n-type MOSFET contains a parasitic n-p-n BJT where the body acts as the base, the drain as the collector, and the source as an emitter. With a floating body, the base of the BJT is left open and holes generated at the drain end of the channel pile up in the body and eventually turn on the base–emitter (body-source) junction of the BJT. This results in electron injection from the source (emitter) into the channel (base) and collection by the drain (collector). In this manner, the hole generation current is multiplied by the current gain of the parasitic bipolar transistor, resulting in a large drain (collector) current [22]. Similar bipolar effects have been observed in other transistors such as planar FETs and FinFETs based on SiGe and Ge [23], [24].

These phenomena have also been identified in planar InGaAs MOSFETs [12]–[15] and more recently in InGaAs FinFETs [25]. Detailed experimental studies [25] confirmed the roles of BTBT and PBE in both types of devices. A bipolar gain exceeding 10^4 [26] and 10^2 [25] was observed for planar and FinFET devices, posing a significant challenge for InGaAs transistor to meet the demanding leakage requirement of advanced logic applications. Its suppression requires a detailed physical understanding, which is the subject of this paper.

This paper presents a first-order scalable model of PBE for InGaAs FinFETs, which captures the key gate length and fin width dependences observed experimentally. Unique to the FinFET is the constrained channel geometry and the presence of fin sidewalls where carrier recombination is expected to take place. Compared with [25], this paper presents a detailed analytical model for PBE and a more complete comparison with experiments emphasizing fin-length and fin-width scaling issues. Our model predicts that the current gain scales with fin width and the inverse of gate length when source recombination dominates in short L_g devices. In addition, in long gate-length devices, a diffusion length proportional to the square root of the fin width is predicted. All these predictions are borne out in experiments.

The paper is organized as follows. The device structure and fabrication process of FinFETs used in our detailed study are presented in Section II. An equivalent circuit model accounting for the various current components is introduced in Section III.

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The authors are with the Department of Electrical Engineering and Computer Science, Massachusetts Institute of Technology, Cambridge, MA 02142 USA (e-mail: xinzhao@mit.edu).

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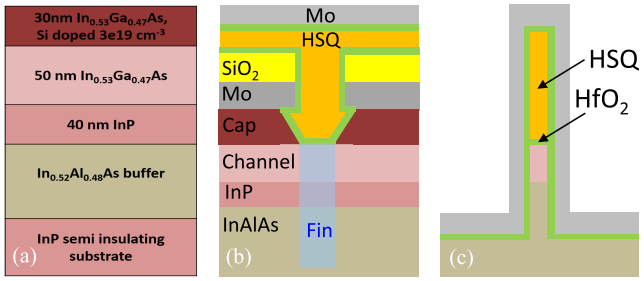


Fig. 1. (a) Starting heterostructure, (b) cross-sectional schematic along with the fin length, and (c) across the fin width in a finished device. In (b), the blue region indicates the location of the fin.

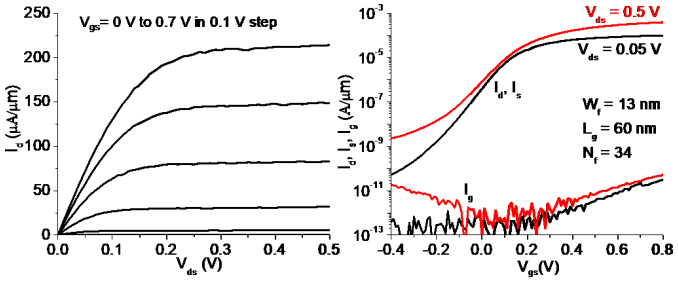


Fig. 2. Output and subthreshold characteristics of an InGaAs FinFET with $W_f = 13$ nm, $L_g = 60$ nm, and $N_f = 34$.

Section IV derives the bipolar gain assuming negligible carrier recombination in the fin, followed by a discussion on the carrier recombination in the fin in Section V. Comparison with experiments is discussed in detail in Section VI.

II. Devices Under Study

Fig. 1(a) shows the starting heterostructure of the InGaAs FinFETs studied here. It includes a 50-nm-thick undoped InGaAs layer as the channel and a 30-nm-thick heavily doped InGaAs cap. Beneath the channel, a buffer layer consisting of 40-nm undoped InP and 400-nm undoped InAlAs was grown. All layers are lattice matched to the InP substrate.

Device fabrication follows a contact-first, gate-last process [9] and features self-aligned ohmic contacts. A combination of dry etch [27] and digital etch (DE) [28] was used to define high aspect ratio fins with smooth and vertical sidewalls. A dry cap recess process based on Cl_2/BCl_3 reactive ion etching and DE resulted in 5 nm separation between the edge of the cap and the fin [Fig. 1(b)]. This is critical to obtaining low access resistance and high performance; 3 nm HfO_2 as gate dielectric was deposited via atomic layer deposition, corresponding to roughly 0.8 nm equivalent oxide thickness. The hydrogen silsesquioxane mask that is used to define the fins is left in place making these double-gate FinFETs. In this process, no intentional contact was made to the body which is left floating.

FinFETs under investigation have fin width $W_f = 13$–25 nm and gate length $L_g = 60$ nm–16 μm. The electrical characteristics of a typical fin array device with $N_f = 34$ fins, $W_f = 13$ nm, and $L_g = 60$ nm are shown in Fig. 2. The output characteristics exhibit excellent current saturation. All metrics are normalized by the conducting gate periphery which is twice the channel thickness or 100 nm.

The InGaAs channel sits on top of a thick undoped barrier layer and a semi-insulating substrate. The devices have three

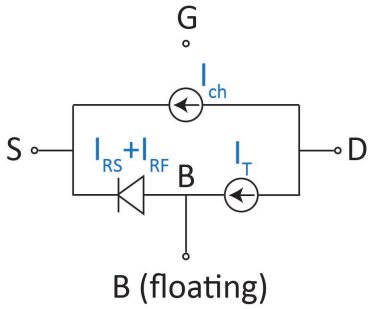


Fig. 3. Equivalent circuit diagram for off-state current.

electrical contacts and the substrate was kept floating during the measurements. The overlapping source and drain currents shown in Fig. 2 confirm that the measured leakage current is not due to drain junction leakage current or substrate leakage.

For the device shown in Fig. 2, a peak transconductance ($g_{m,pk}$) of 770 μS/μm is obtained at $V_{ds} = 0.5$ V. A minimum subthreshold swing at $V_{ds} = 0.05$ V (S_{lin}) of 78 mV/dec is also obtained. In the bias range of interest, the gate current is at least 1.5 orders of magnitude lower than the drain–source current. For $V_{ds} = 0.5$ V, the significant OFF-state current is observed. This is caused by a combination of BTBT and PBE. Developing a model for this current is the goal of this paper.

III. Equivalent Circuit Model

A steady-state equivalent-circuit model for the InGaAs FinFET in the OFFstate that includes the parasitic floating-base bipolar transistor is shown in Fig. 3.

The origin of the excess drain current in the OFFstate is BTBT induced by the high electric field that appears at the drain-end of the channel under large gate-to-drain bias [12]–[20], [25]. This is represented in Fig. 3 by the I_T current generator. Electrons generated by BTBT flow directly into the drain while the generated holes accumulate in the floating body (middle node, labeled B). Hole accumulation self-biases the body and turns on the base–emitter (body-source) junction of the BJT. A consequence of this is hole injection into the source and subsequent recombination in the heavily doped cap region or at the cap-contact interface. This is captured in Fig. 3 by the diode component I_{RS}.

A second consequence of the reduction in the source-body energy barrier associated with the forward-biasing of this junction is electron injection from the source into the fin. Most of these electrons diffuse through the channel and are collected by the drain. This is represented in Fig. 3 by the current generator I_{ch}. This current adds to the BTBT current and results in the excess drain current that is observed.

A few of the electrons injected into the channel recombine with the holes that have piled up there. This recombination can take place in the body of the fin or at the sidewall surfaces. Carrier recombination in the fin results in an additional source-body current component captured by the second diode term I_{RF}.

Under steady-state conditions, the tunneling current is equal to the total recombination current. We then have

$$I_T = I_{RS} + I_{RF}. \quad (1)$$

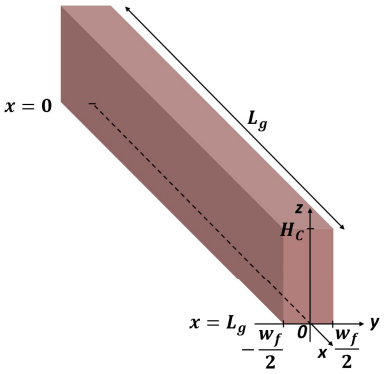


Fig. 4. Schematic showing the fin geometry.

The current gain of the parasitic bipolar transistor is the ratio of the collected current from the channel divided by the total recombination current. Hence

$$\beta = \frac{I_{\rm ch}}{I_{\rm T}} = \frac{I_{\rm ch}}{I_{\rm RS} + I_{\rm RF}}. \tag{2}$$

The total drain current is then given by

$$I_{\rm D} = I_{\rm T} + I_{\rm ch} = I_{\rm T}\,(1+\beta)\,. \tag{3}$$

In the following sections, we build a model for β. We first assume negligible recombination in the fin, that is, $I_{\rm RF} = 0$. This will be shown to describe well the characteristics of short channel transistors. We then develop a model for $I_{\rm RF}$ by accounting for recombination in the fin and show its relevance in long-channel transistors.

IV. Negligible Carrier Recombination in the Fin

Fig. 4 shows the geometry of the fin. x is the direction along the fin length with electron injection at $x = 0$ (source side) and extraction at $x = L_{\rm g}$ (drain side), y is the direction transversal to the fin, and z is the direction normal to the wafer surface.

In sufficiently short gate length transistors with well-passivated sidewalls, total recombination in the fin may well be negligible in comparison to recombination in the source. The situation is then similar to a standard BJT biased in the forward-active regime [22] where the base current consists entirely of carrier recombination in the emitter with base recombination being negligible. This is the case we study first.

The channel current consists of electron injection from the source into the fin, diffusion along the fin, and collection by the drain. This is a classic minority-carrier situation as in the base of a standard BJT. Diffusion is the prevailing transport mechanisms because the MOSFET is biased in the subthreshold regime and there is no lateral field along the fin length. We assume low-level injection conditions in the fin, that is, $n \ll p$. This assumption is borne out by the good agreement between our model predictions and experimental data, as shown below.

As in a standard BJT, in the absence of significant base recombination, the excess electron distribution in the base (fin) has a linear relationship along the fin direction, as sketched with the blue line in Fig. 5. Also, the excess electron concentration at the fin end is 0 due to the high field region that

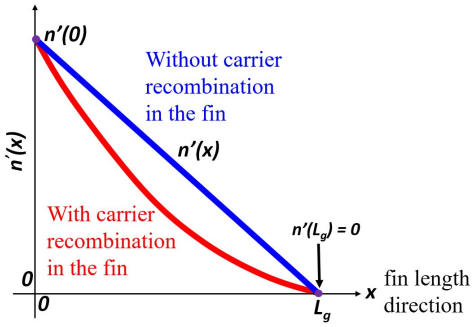


Fig. 5. Excess electron density along the fin in the absence of carrier recombination in the fin.

extracts the electrons into the drain. Analytically, then

$$n'(x) = n'(0)\left(1 - \frac{x}{L_{\rm g}}\right). \tag{4}$$

Note that in the absence of fin recombination, there is no dependence of the electron concentration with the fin across the width direction.

From the excess carrier distribution in (4), we can obtain the channel current $I_{\rm ch}$ (note sign definition in Fig. 3) as

$$I_{\rm ch} = -q\,D_{\rm e}H_{\rm c}W_{\rm f}\frac{dn'}{dx}\bigg|_{L_{\rm g}} = \frac{q\,D_{\rm e}H_{\rm c}W_{\rm f}n'(0)}{L_{\rm g}} \tag{5}$$

where $D_{\rm e}$ is the electron diffusivity in the fin and $H_{\rm c}$ is the fin height.

According to the ideal BJT model, the hole recombination current in the source (emitter), $I_{\rm RS}$, is approximately [20]

$$I_{\rm RS} = q\,D_{\rm h}H_{\rm c}W_{\rm S}\frac{p'(0)}{L_{\rm E}} \tag{6}$$

where $D_{\rm h}$ is the hole diffusivity in the source, $L_{\rm E}$ is the characteristic length relevant for emitter recombination, $p'(0)$ is the excess hole concentration at the source side of the junction, and $W_{\rm S}$ is the width of the source. The magnitude of $L_{\rm E}$ depends on the dominant recombination mechanism, whether bulk recombination in the heavily doped cap or at the ohmic contact interface. As we note below, the details of recombination at the source are of secondary significance in this paper.

Under the assumption of negligible carrier recombination in the fin, the bipolar gain (denoted as β_0) can be written as

$$\beta_0 = \frac{I_{\rm ch}}{I_{\rm T}} = \frac{I_{\rm ch}}{I_{\rm RS}} = \frac{{\rm D_e}n'(0)L_{\rm E}W_{\rm f}}{D_{\rm h}p'(0)L_{\rm g}W_{\rm S}}. \tag{7}$$

The important result here is that in the absence of significant carrier recombination in the fin, the bipolar gain is inversely proportional to the gate length and scales linearly with fin width. These dependencies will be verified below.

V. Carrier Recombination in the Fin

In medium and long-channel devices, carrier recombination in the base (fin) can become significant. In the Appendix, a model for carrier recombination in the fin is developed by reducing the inherently 3-D problem to two quasi-1-D problems with the carrier distribution along the fin decoupled from that across the fin. In our model, we assume that nothing changes along the z-direction (vertical to the wafer surface)

since the channel is vertically confined by two high-quality heterojunctions.

Along the x dimension, the problem is governed by the electron diffusion length, L_d. This is the mean distance that electrons diffuse along the length of the fin before recombining. Recombination in the fin is assumed to be dominated by surface recombination and is governed by transport along the y-direction which is modeled in the Appendix. From (27) in the Appendix, we have

$$L_d \approx \sqrt{\frac{D_e W_f}{2S}} \tag{8}$$

where S is the surface recombination velocity at the fin surface.

Along the fin length [see Fig. 5 (red line)], we have a classic minority carrier problem [20] with

$$n'(x) = A \exp\left(-\frac{x}{L_d}\right) + B \exp\left(\frac{x}{L_d}\right) \tag{9}$$

where A and B are constants to be determined. With the boundary conditions given in Fig. 5, we have

$$n'(x) = n'(0) \frac{\exp\left(\frac{x}{L_d}\right) - \exp\left(\frac{2L_g - x}{L_d}\right)}{1 - \exp\left(\frac{2L_g}{L_d}\right)}. \tag{10}$$

According to (5), we can obtain the collector current I_{ch}

$$I_{ch} = q D_e H_c W_f \frac{2n'(0)}{L_d} \frac{\exp\left(\frac{L_g}{L_d}\right)}{\exp\left(\frac{2L_g}{L_d}\right) - 1}. \tag{11}$$

We now turn our attention to calculate the two components of the hole current in (1). The hole recombination current in the source (emitter), I_{RS}, is unchanged from (6) derived in the previous section. The hole current induced by base (fin) recombination, I_{RF}, can be obtained from

$$I_{RF} = q H_c W_f \int_0^{L_g} U dx = \frac{q H_c W_f}{\tau_e} \int_0^{L_g} n'(x) dx \tag{12}$$

where τ_e is the carrier lifetime in the fin. This is not the bulk carrier lifetime but the mean recombination time at the surface and is set by W_f and S [see (25) in the Appendix].

Plugging (10) into (12), we obtain

$$I_{RF} = q H_c W_f \frac{n'(0) L_d}{\tau_e} \frac{\exp\left(\frac{L_g}{L_d}\right) - 1}{\exp\left(\frac{L_g}{L_d}\right) + 1}. \tag{13}$$

We now study two limiting cases depending on which base current component, I_{RF} or I_{RS}, dominates. In the case where base (fin) recombination dominates, we have

$$\beta_F = \frac{I_{ch}}{I_{RF}} = \frac{2 \exp\left(\frac{L_g}{L_d}\right)}{\left[\exp\left(\frac{L_g}{L_d}\right) - 1\right]^2}. \tag{14}$$

When emitter (source) recombination dominates, we get

$$\beta_S = \frac{I_{ch}}{I_{RS}} = 2\beta_0 \frac{L_g}{L_d} \frac{\exp\left(\frac{L_g}{L_d}\right)}{\exp\left(\frac{2L_g}{L_d}\right) - 1}. \tag{15}$$

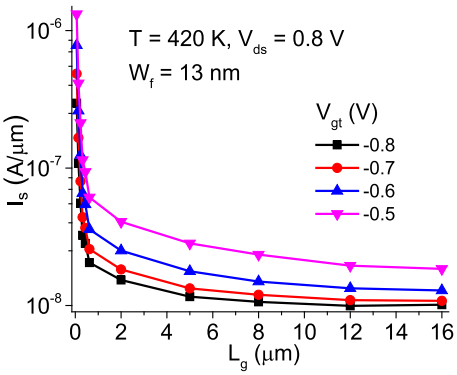


Fig. 6. Source current of $W_f = 13$ nm, $N_f = 34$ FinFETs with various L_g, showing saturating OFF-state current for $L_g > 8$ μm. This is the pure BTBT current.

We can now examine the L_g limits for β_F and β_S. At short L_g, we can assume $L_g \ll L_d$ and the gain in both cases becomes

$$\beta_F|_{\text{short}L_g} \approx 2\left(\frac{L_d}{L_g}\right)^2 \left(1 + \frac{L_g}{L_d}\right) \approx 2\left(\frac{L_d}{L_g}\right)^2 \tag{16}$$

and

$$\beta_S|_{\text{short}L_g} \approx \beta_0 \left(1 + \frac{L_g}{L_d}\right) \approx \beta_0. \tag{17}$$

This second result is straightforward as when source recombination dominates, in the limit of short gate length devices, the case studied here reverts to the one discussed in Section IV.

For long gate length transistors $L_g \gg L_d$, the current gain in the two cases studied here becomes

$$\beta_F|_{\text{long}L_g} \approx 2 \exp\left(-\frac{L_g}{L_d}\right) \tag{18}$$

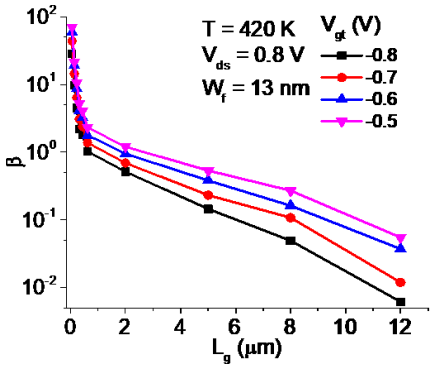
$$\beta_S|_{\text{long}L_g} \approx 2\beta_0 \frac{L_g}{L_g} \exp\left(-\frac{L_g}{L_d}\right). \tag{19}$$

To summarize, we find that for long gate lengths, the parasitic bipolar transistor gain decays exponentially with L_g. For short L_g, the current gain goes as $1/L_g$ if emitter recombination dominates and as L_g^{-2} if fin recombination is dominant.

VI. Experimental Verification

The source current of $W_f = 13$ nm devices with different L_g from 60 nm to 16 μm at $T = 420$ K, $V_{ds} = 0.8$ V and various V_{gt} are shown in Fig. 6. Here, an elevated temperature is used to mitigate contamination from gate current. The temperature dependence of the drain–source current leakage follows that of the BTBT process, as discussed in [25]. The gate current shows a weaker temperature dependence. As a result, the source/drain current increases relatively to the gate current as the temperature rises, enabling a cleaner study of the OFF-state leakage current at higher temperatures. In our analysis, I_S is used instead of I_D to minimize the impact of gate current, especially at high drain bias. $V_{gt} = V_{gs} - V_t$ is used to correct V_t roll-off with L_g. V_t is extracted at constant $|I_s| \times L_g$ (10^{-6} A/μm $\times$ 1 μm).

We observe in Fig. 6 that the OFF-state current is rather insensitive to L_g for $L_g \geq 8$ μm, suggesting negligible current gain. This current floor is then I_T in (3). This realization



V_{gt} (V)	L_d (μm)
-0.5	3.2
-0.6	3.0
-0.7	2.5
-0.8	2.3

Fig. 7. Bipolar gain as a function of L_g for the device in Fig. 6 in the semilog scale (left). Extracted electron diffusion length (L_d) in the channel (right table).

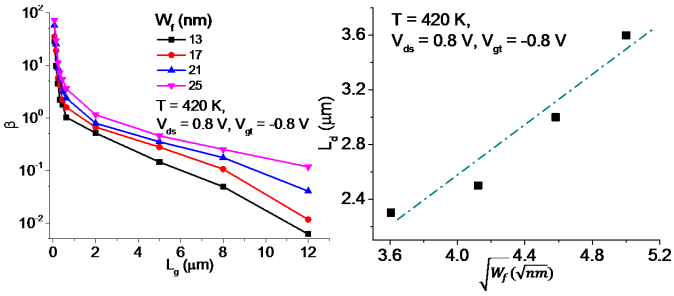


Fig. 8. Left: β as a function of L_g for different W_f. Right: extracted L_d versus $\sqrt{W_f}$ revealing a linear dependence.

allows us to experimentally extract the current gain at all $L_g < 16\ \mu$m. Using (3), then, β can be obtained from [25]

$$\beta = \left(\frac{I_S}{I_S|_{\text{long}L_g}} - 1 \right). \tag{20}$$

Fig. 7 plots the extracted β versus L_g in a semilog scale. An exponential L_g dependence is observed for $L_g > 2\ \mu$m, as predicted by our model equations (18) and (19). From the slope of the β decay, we can estimate L_d (see the table in Fig. 7) and values of around 2–3 μm are extracted. We find that L_d is reduced at lower V_{gt}, likely due to an increasing hole density in the base which enhances electron recombination.

Fig. 8 shows the extracted β as a function of L_g in semilog scale for devices with different W_f (left), as well as the extracted L_d as a function of $\sqrt{W_f}$ (right). As predicted by (8), we observe a linear dependence of L_d on $\sqrt{W_f}$, verifying the dominance of fin sidewall recombination in long channel devices.

The gate length dependence at short L_g can be studied by plotting experimental β versus L_g in a log-log scale, as shown in Fig. 9. A linear relationship with a slope of -1 is observed for $L_g < 2\ \mu$m, suggesting that source recombination is dominant, as in (17) and (7). This value of L_g ($\sim 2\ \mu$m) that separates the short- and long-L_g regimes is consistent with the above-estimated L_d values.

Further confirmation that source recombination is dominant in short L_g devices is obtained by studying the β dependence on W_f in this regime. The source recombination should not depend on W_f according to (6). We therefore expect a linear W_f dependence for the gain in (7) that stems from the linear dependence of the channel current that scales with W_f in (5).

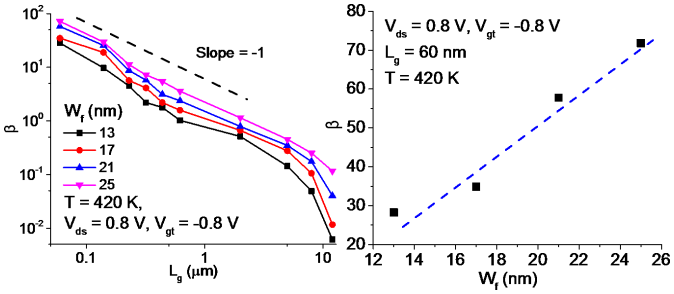


Fig. 9. Left: β (log-log scale) versus L_g for devices with different W_f. Right: Current gain as a function of W_f for $L_g = 60$ nm.

We experimentally confirm this by observing in Fig. 9 a linear dependence of β versus W_f in short-channel devices.

VII. Conclusion

In a III–V FinFET biased in the OFFstate at high drain bias, the PBE associated with its floating body multiplies the BTBT current. This makes it challenging to meet the stringent leakage requirement of logic applications. We have developed a simple model of PBE for InGaAs FinFETs that accounts for carrier recombination in the fins. The model predicts the exponential L_g dependence of the gain on the parasitic BJT for long L_g transistors, enabling extraction of the diffusion length and verification of its fin width dependence. At short L_g, source recombination is shown to dominate and the current gain scales with the inverse of L_g.

Appendix

To model the carrier recombination in the fins, we first assume that carrier confinement limits all carrier action to the InGaAs channel bound by large energy sidewalls at its top and bottom. We also assume perfect passivation at the top and bottom surfaces. This removes the z-direction from the problem.

We then deal with the y-direction, transversal to the fin. In a narrow fin made of a long carrier lifetime material, carrier recombination is most likely dominated by surface recombination [29] and bulk recombination can be assumed negligible. This is a classic minority carrier problem with a straightforward solution. We can start from, for example, [23, eq. (5.156)], and assume negligible bulk recombination. By changing the notation for the present problem, the excess electron concentration across the fin can be written as

$$n'(x, y) \approx n'(x, 0) \left[1 - \frac{SW_f}{D_e} \left(\frac{y}{W_f} \right)^2 \right]. \tag{21}$$

The net surface recombination rate taking place at cross section x along the fin is twice the recombination at each surface, or

$$U_s(x) = 2Sn' \left(x, \frac{W_f}{2} \right) = 2Sn'(x, 0) \left(1 - \frac{SW_f}{4D_e} \right). \tag{22}$$

In the limit of reasonably well-passivated fin sidewall surface and thin fins, we can approximate this by

$$U_s(x) \approx 2Sn'(x, 0). \tag{23}$$

An alternative way to express this result is to derive an expression for the mean time between recombination events

for excess electrons at cross section x along the fin length. We can denote this as an effective carrier lifetime. To derive an expression for this, we first turn the total surface recombination rate into equivalent volume recombination. This is done by dividing by W_f. Then we equate this to the excess electron concentration divided by the effective carrier lifetime τ_e. Altogether, we have

$$U(x) = \frac{U_s(x)}{W_f} \approx \frac{2S}{W_f} n'(x,0) = \frac{n'(x,0)}{\tau_e}. \tag{24}$$

Solving for τ_e, we obtain

$$\tau_e \approx \frac{W_f}{2S}. \tag{25}$$

This is expected since (25) expresses the average that it takes for an electron to reach the surface and recombine [22].

Finally, we focus on the x-direction along the fin length. With a constant effective carrier lifetime irrespective of x location as in (25), we expect an excess electron profile along the fin length direction that is characterized by a diffusion length, L_d, that represents the mean distance that an electron travels by diffusion before recombining. L_d is then given by

$$L_d = \sqrt{D_e \tau_e}. \tag{26}$$

Here, τ_e is the effective carrier lifetime that is determined by surface recombination, as obtained in (25). We then have

$$L_d \approx \sqrt{\frac{D_e W_f}{2S}}. \tag{27}$$

We find that the characteristic length for minority carrier recombination increases with fin width and decreases with surface recombination velocity. Both trends reflect the dominant role of surface recombination in this problem.

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