Temperature-Accelerated Degradation of GaN HEMTs under High-Power Stress: Activation Energy of Drain-Current Degradation

Yufei Wu, Chia-Yu Chen, and Jesús A. del Alamo

Microsystems Technology Laboratories, Massachusetts Institute of Technology, Cambridge, MA 02139; yufeiw@mit.edu; +1-857-269-0441

Abstract – We have investigated the role of temperature in the degradation of GaN High-Electron-Mobility-Transistors (HEMTs) under high-power stress. We found that two degradation mechanisms take place in a sequential manner: the gate leakage current increases first, followed by a decrease in the drain current. Building on this observation, we demonstrate a new scheme to extract the activation energy (E_a) of device degradation from step-temperature measurements on a single device. The E_a's we obtained closely agree with those extracted from conventional accelerated life test experiments on a similar device technology.

I. INTRODUCTION

In the last few years, high-voltage GaN FET technology has burst into the scene promising to revolutionize high-power high-frequency amplifiers as well as high-voltage power management systems. A critical concern with this new technology is reliability. This is particularly problematic due to the absence of a native substrate for GaN.

In this work, we study the role of temperature in the high-power degradation of GaN HEMTs, a topic that, in contrast with the OFF-state, has received little attention in spite of its importance for power amplifier applications. A key difficulty in high-power stress experiments is managing self-heating and carrier trapping. Unless these issues are correctly handled, it is not possible to isolate the dominant degradation mechanism and obtain its activation energy (E_a). This is required before device lifetime projections to realistic operating conditions can be made. Deriving the E_a of degradation in particular is very time consuming as it requires long-term stress experiments in many devices. In the early stages of development of a new technology, this is also difficult as variations in device characteristics introduce significant ambiguity in the interpretation of the results.

We present here a new methodology to study the high-power degradation of GaN HEMTs. Our approach is based on *step-temperature experiments*. With appropriate care, we show that the effect of trapping can be minimized and the activation energy of the dominant degradation mechanism can be derived from measurements *on a single device*.

II. EXPERIMENTS

The devices used in this study are prototype packaged Gen-I S-band GaN-on-SiC MMICs. The transistor features L_g=0.25 µm and W_g=2x280 µm.

Testing is carried out in an Accel-RF life-test system equipped with a switching matrix that allows device characterization through external test equipment [1]. A flow chart of a typical step-temperature experiment is shown in Fig. 1. At its heart, the device is stressed for some time at high power and at a set base plate temperature, T_{stress}. After a certain stress time, we interrupt the stress, lower the base plate temperature to 50 °C and characterize the device. We call this the "inner loop." After a number of "inner loops" have been repeated, we detrap the device through an in-situ bake at 250 °C for 7.5 hours, characterize it at 50 °C, increase to a higher T_{stress} and resume the high-power stress at this new base plate temperature. We denote this the "outer loop." The 250 °C baking allows us to evaluate permanent degradation, free of carrier trapping effects.

In our study, we focused on the degradation of the maximum drain current, I_{Dmax} (defined at V_{DS} = 5 V,

V_{GS} = 2 V), and the drain resistance, R_D (defined as the extrinsic resistance on the drain side measured at 20 mA/mm using the gate current injection technique [2]). These figures of merit have been found to correlate most closely with RF power degradation [1]. Other figures of merit, such as R_S and I_{Goff} are also tracked where R_S is defined as the extrinsic resistance on the source side measured at 20 mA/mm using the gate current injection technique and I_{Goff} is defined as the gate current at V_{DS}= 0.1 V and V_{GS}= -5 V. Device thermal models are used to estimate the channel temperature during stress.

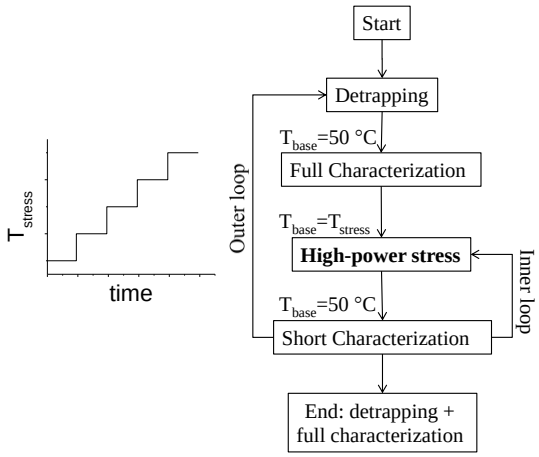

Fig 1. Flow chart of a typical step-temperature stress experiment. The stress temperature is stepped up periodically as the experiment flow goes through the outer loop.

Typical results are shown in Fig. 2. Here, the device is stressed at V_{DSQ}=40 V, I_{DQ}=100 mA/mm with T_{stress} increasing from 50 °C to 230 °C (600 min/step). The off-state gate current I_{Goff} dramatically increases by about 3 orders of magnitude starting at T_{stress}=170 °C and saturating at T_{stress}=190 °C (Fig. 2a) [3][4]. The maximum drain current I_{Dmax} starts to decrease at T_{stress}=190 °C. By the time the device blows up at T_{stress}=230 °C ($T_{channel}$=330 °C), I_{Dmax} has decreased by about 80%. R_D follows a degradation pattern that tracks that of I_{Dmax} (Fig. 2b). R_S exhibits much less degradation. There is a marked difference between inner loop data (most of the data points) and outer loop data (those sticking out every 600 min). Outer loop data reflects permanent damage while inner loop data also includes the effect of trapping. This difference dramatically illustrates the impact of trapping which can also be seen from in-situ current collapse measurements in the outer loop (inset of Fig. 2b), reflecting trap generation as a result of stress. Current collapse in GaN HEMTs is a temporary reduction of drain current immediately after the application of high voltage [5]–[7]. The conventional measurement method is the pulsed technique. Here, we have adopted a DC current collapse technique instead which can be carried out in standard DC characterization equipment, as described in [8]. The rates of permanent I_{Dmax} and R_D degradation are clearly thermally activated as seen in the Arrhenius plot of Fig. 3. E_a for R_D and I_{Dmax} degradation closely correlate reflecting the same underlying degradation physics.

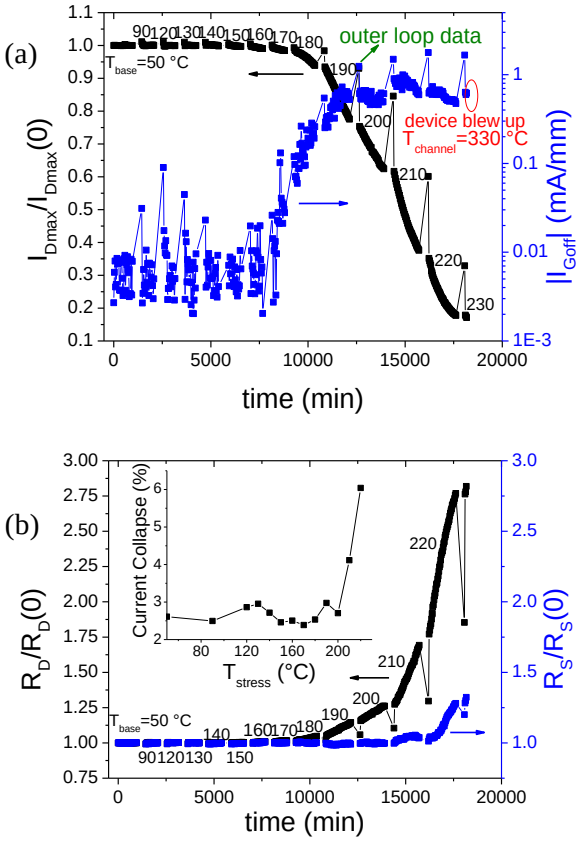

Fig. 2 Evolution of degradation of (a) normalized I_{Dmax} (defined @ V_{DS} = 5V, V_{GS} = 2V) and $|I_{Goff}|$ (defined @ V_{DS} = 0.1 V, V_{GS} = -5 V), (b) normalized R_D and R_S. Both outer loop and inner loop data are included in the graphs. Inset: current collapse measurements in the outer loop. The device was stressed at V_{DSQ}=40 V and I_{DQ}=100 mA/mm at a base temperature that increases from 50 °C up to 230 °C.

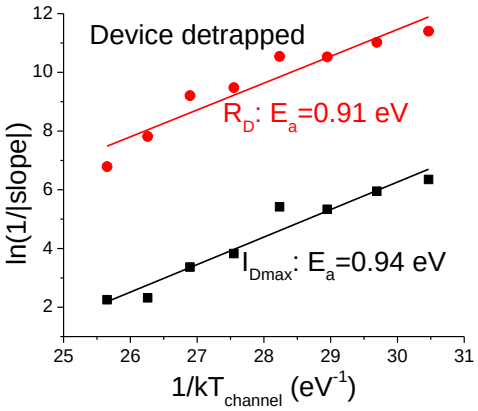

Fig. 3 Arrhenius plot for degradation rates of permanent I_{Dmax} and R_D extracted from data collected after the detrapping step that follows each temperature stress period (outer loop data) for the experiment of Fig. 2.

Similar experiments were carried out on other samples. In some devices, we did not observe significant I_D degradation before they blew up. After detailed analysis, we found that sizable I_D degradation only occurs after I_G degradation is fully saturated. This suggests that in order to study the degradation physics of I_D and R_D, we have to degrade I_G to saturation first. For this, we designed a two-phase experiment with a very short temperature ramp from 50 °C to 220 °C (phase I) which fully saturates I_G degradation without introducing any significant I_D or R_D degradation. This is followed by a phase II that is similar to the experiment of Fig. 1 where we observe I_D degradation without further changes in I_G.

Results from phase II of a typical experiment are shown in Fig. 4. In 4a, $|I_{Goff}|$ stays at the saturated level produced in phase I while I_{Dmax} (Fig. 4b) starts to decrease from T_{stress}=150 °C and ends up at 70% of its original value. R_D (Fig. 4c) correlates well with I_{Dmax} and shows an overall degradation of 25%. The degradation rates of I_D and R_D in the outer loop also suggest thermally activated behavior (Fig. 5) with E_a of 1.04 and 0.84 eV, respectively. E_a for I_{Dmax} obtained here is close to values reported on similar technology: 1.05 eV [9] and 1.12 eV [10].

From experiments like this, a consistent pattern has emerged. Under high-power stress, I_G degradation occurs first and saturates. Only after this, I_D and R_D start to degrade. Fig. 6 and 7 show the correlation between I_{Goff} and I_{Dmax} degradation in a number of experiments on different devices. A striking "universal" behavior confirms this picture for both permanent degradation and trapping-related degradation implying two different degradation mechanisms for I_{Goff} and I_{Dmax} that operate sequentially, just as observed under high-voltage stress in the OFF-state [11].

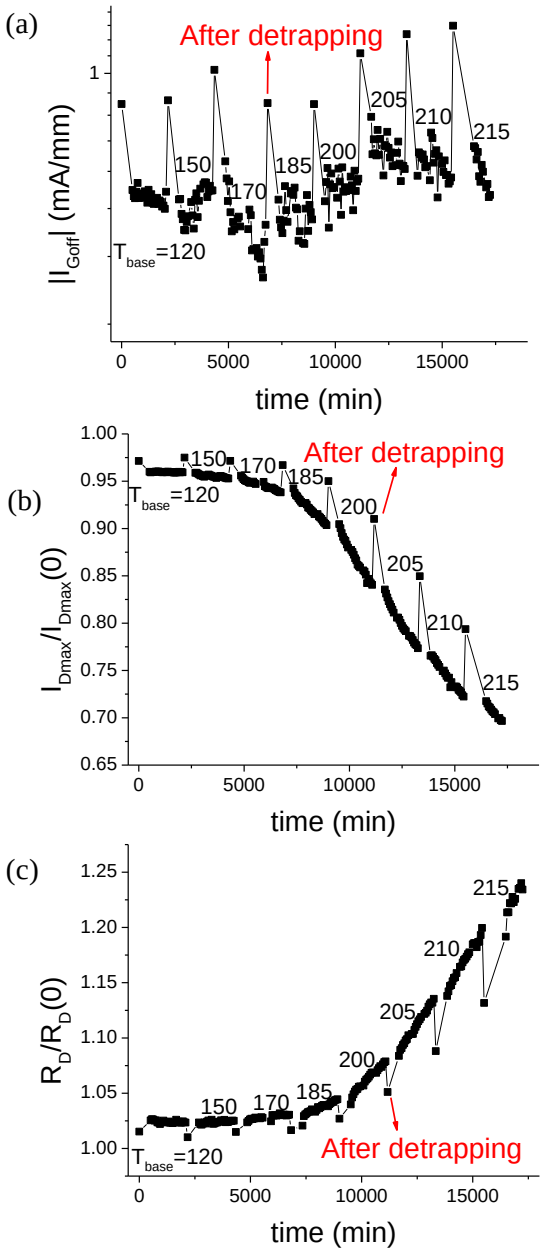

Fig. 4 Inner loop and outer loop results from phase II of 2-phase experiment (T_{stress}=120 °C to 215 °C): (a) $|I_{Goff}|$, (b) normalized I_{Dmax} and (c) normalized R_D. In this second phase, the device was stressed at V_{DSQ}=40 V and I_{DQ}=100 mA/mm and at a base temperature that increases from 120 °C up to 215 °C..

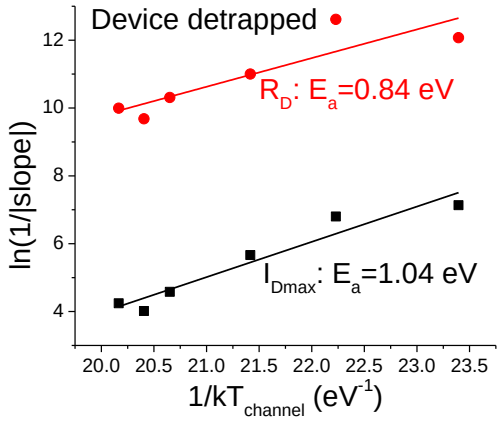

Fig. 5 Arrhenius plot of permanent I_D and R_D degradation rates extracted from outer loop data for the experiment of Fig. 4.

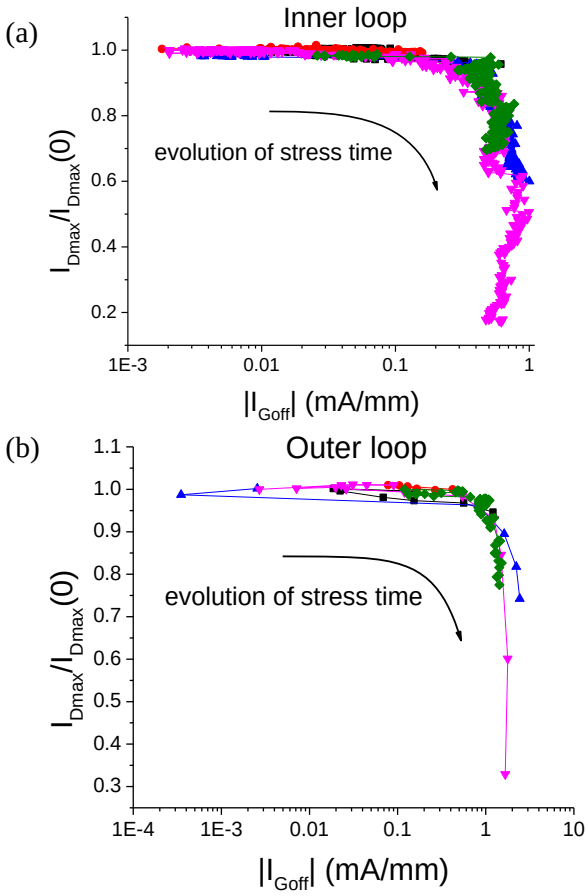

Fig. 6 Evolution of drain current degradation vs. gate current degradation of all devices investigated in this study: (a) data measured within each temperature stress period (inner loop), (b) data measured after detrapping steps (outer loop).

III. CONCLUSIONS

In summary, we have studied the high-power degradation of GaN-on-SiC HEMTs. We have developed a new methodology that allows the extraction of the activation energy for permanent I_D degradation through a new step-temperature stress methodology in a single device. We show that trapping is a major confounding factor in high-power reliability experiments. Under high-power stress we find that there are two sequential degradation mechanisms for I_G and I_D. The activation energy for the permanent degradation of I_D is between 0.94 eV and 1.04 eV in good agreement with separate reports on similar devices.

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