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III-V MOSFETs for CMOS: Recent Advances in Process Technology

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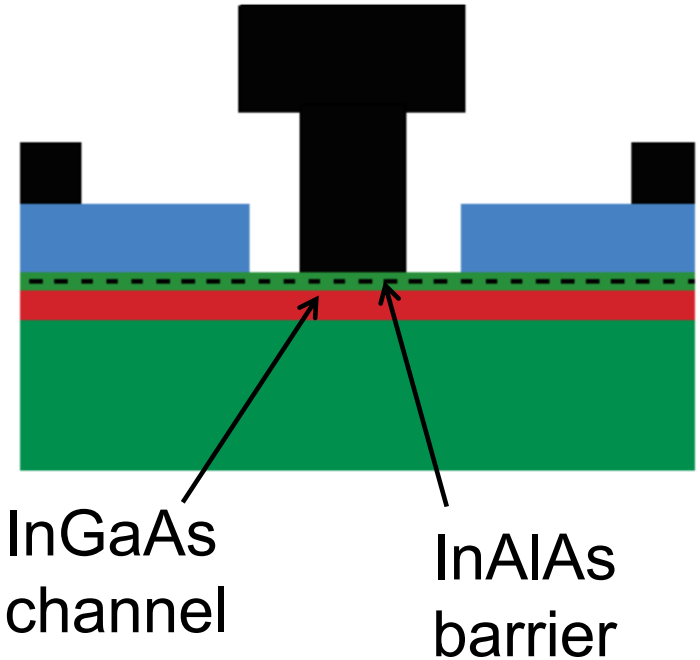
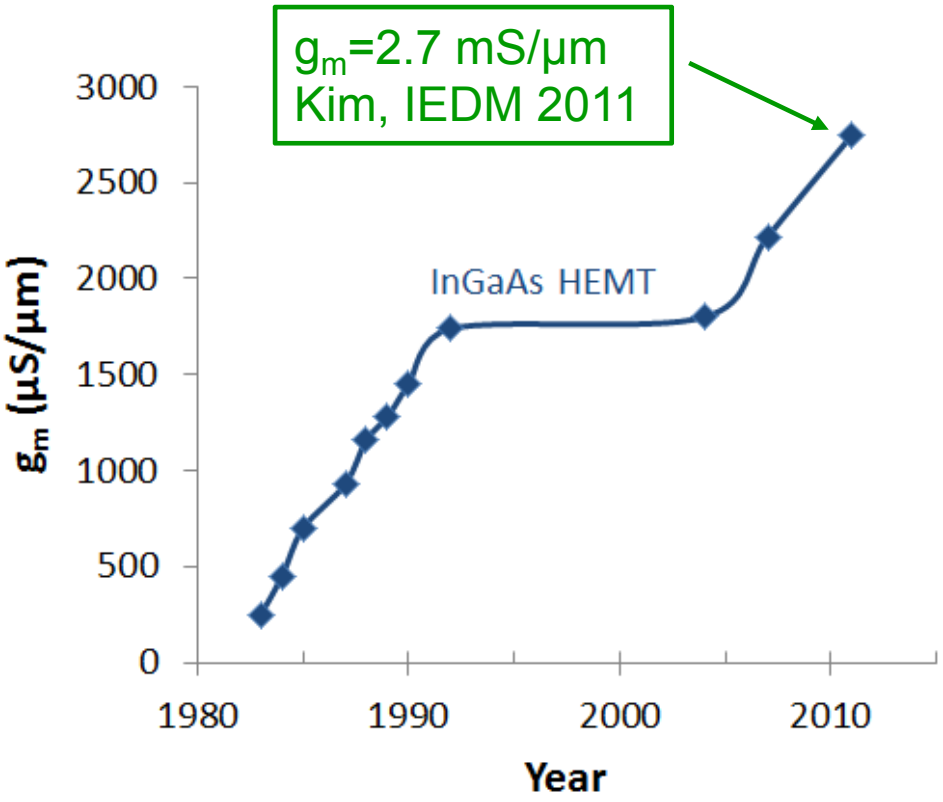
Outline

1. Introduction: recent progress on InGaAs MOSFETs
2. InGaAs MOSFETs: process challenges and opportunities
   - Technology issue #1: MOS gate stack
   - Technology issue #2: ohmic contacts
   - Technology issue #3: self-aligned MOSFET architectures
   - Technology issue #4: 3D MOSFETs
3. Conclusions

InGaAs
High Electron Mobility Transistors

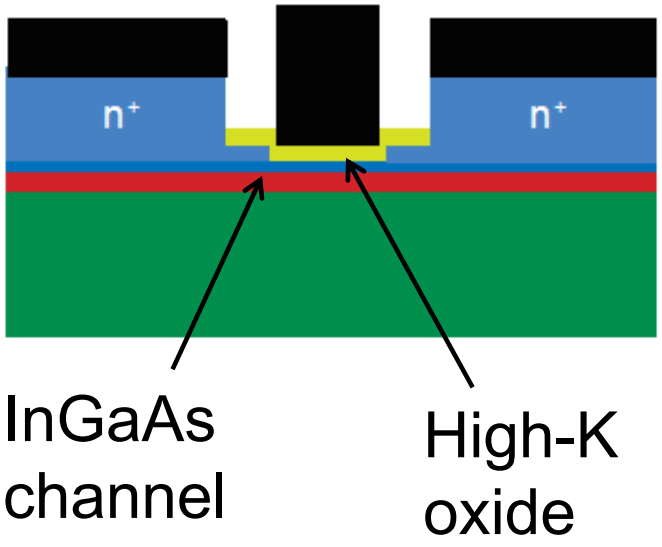


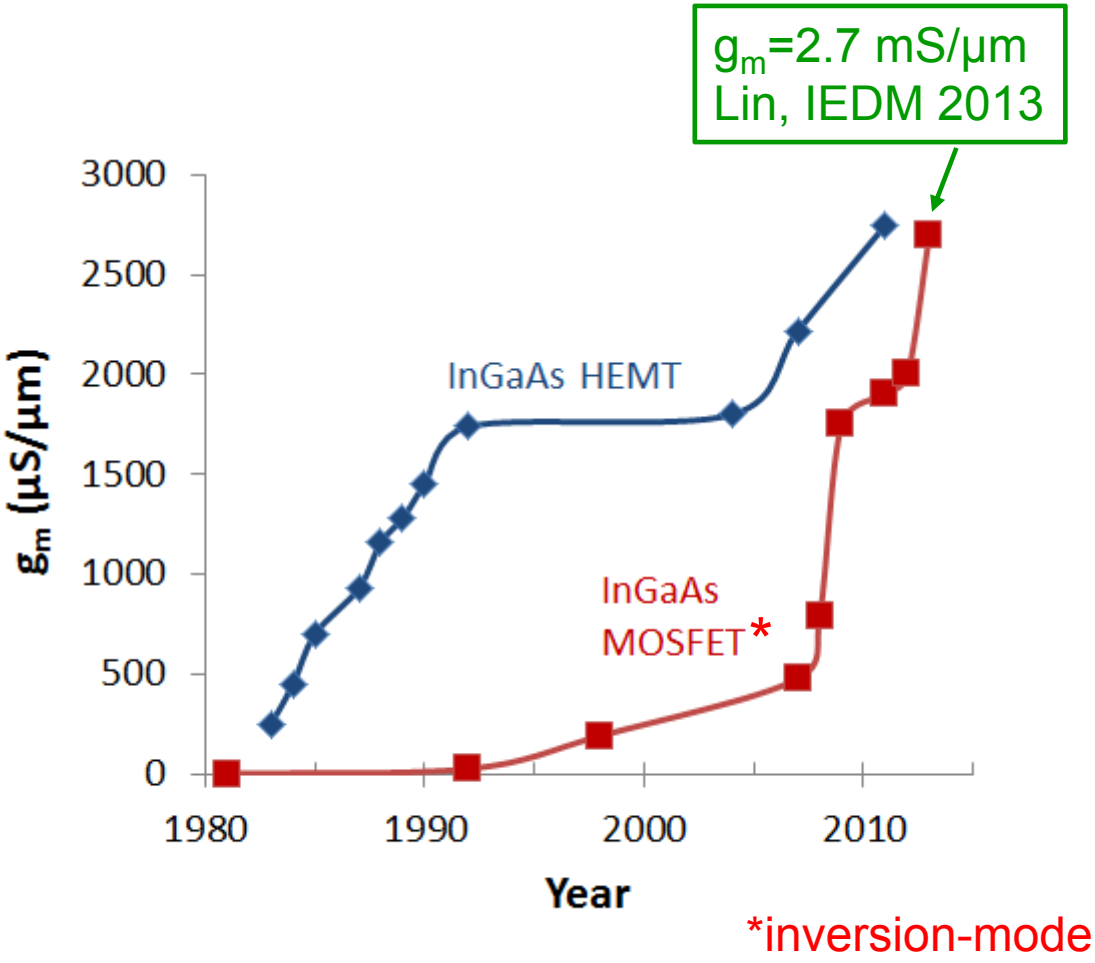


Main attractions of InGaAs:

- μ_e = 6,000 - 30,000 $cm^2/V.s$ @ 300K
- v_{inj} = 2.5 - 3.7x10^7 cm/s @ 300 K

InGaAs MOSFETs





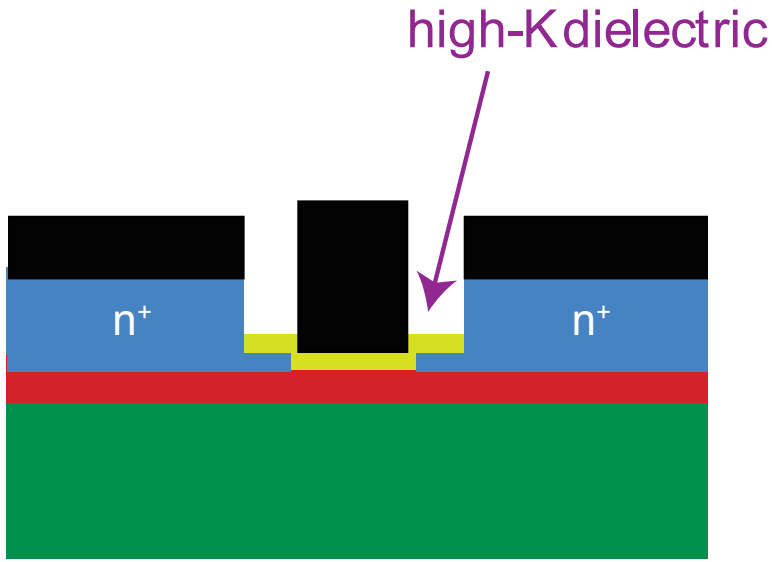
*inversion-mode

Extraordinary recent progress of InGaAs MOSFETs

Technology issue #1: MOS gate stack

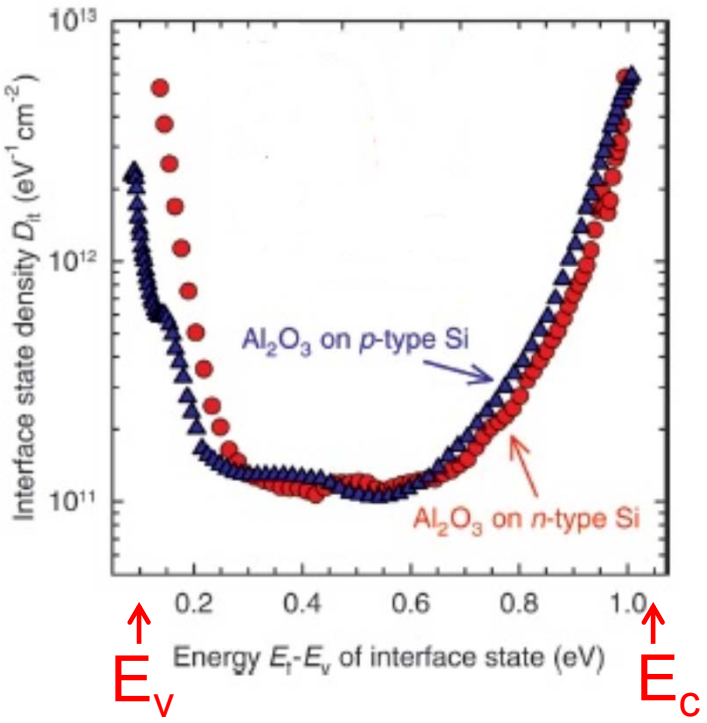
Challenge: metal/high-K oxide gate stack

- Fabricated through *ex-situ* process
- Very thin barrier (EOT ~ 0.5 nm)
- Low gate leakage (I_G<1 A/cm^2 at V_{GS}=0.5 V)
- Low D_{it} (<3x10^{12} eV^{-1}.cm^{-2} in top ~0.3 eV of bandgap and inside CB)
- Reliable



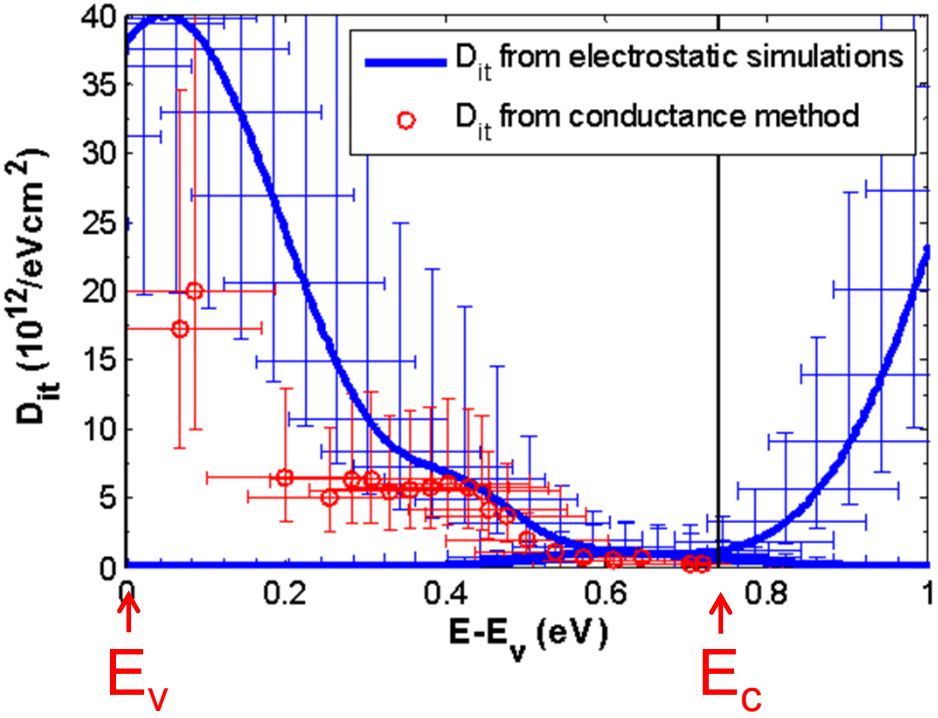
Interface quality: Al_2O_3/InGaAs vs. Al_2O_3/Si

Al_2O_3/Si



Werner, JAP 2011

Al_2O_3/InGaAs



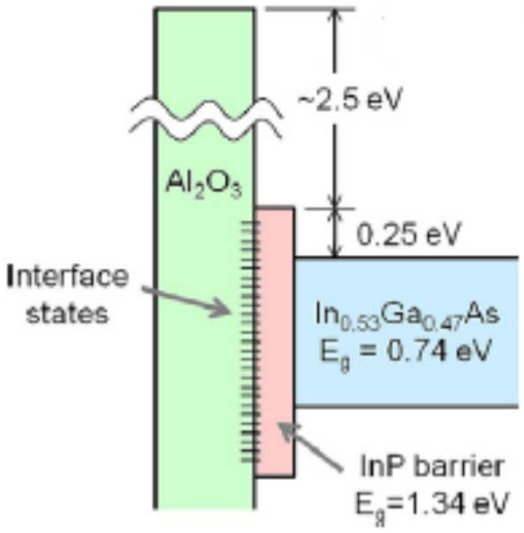
Brammertz, APL 2009

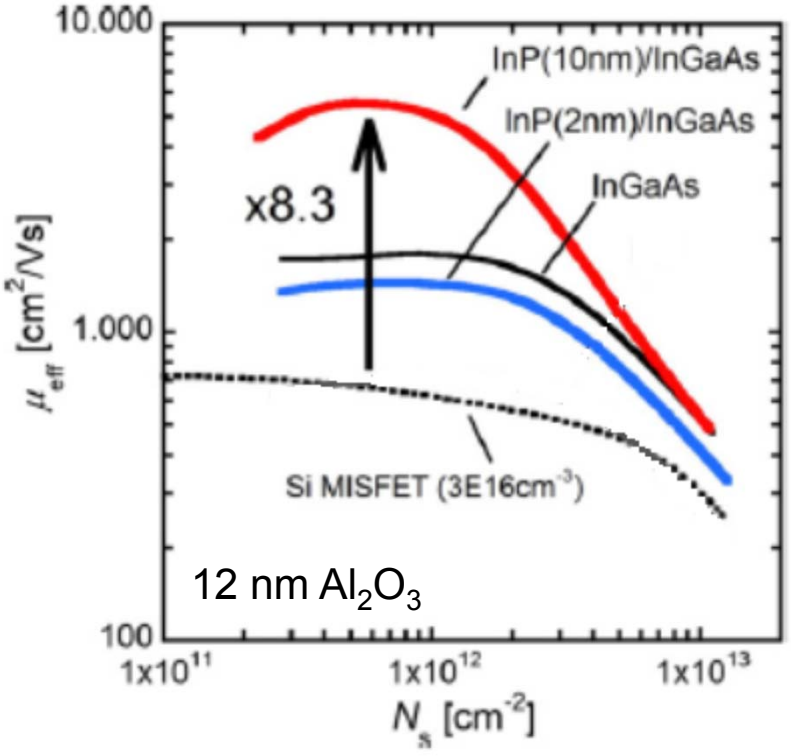
Close to E_c, Al_2O_3/InGaAs comparable D_{it} to Al_2O_3/Si interface

Buried-channel *vs.* surface channel?

Classic trade-off:

- Surface channel: high scalability but low mobility (μ_e<2,000 cm^2/V.s)
- Buried channel: high mobility but high EOT and t_{barr} ↓ → μ_e ↓



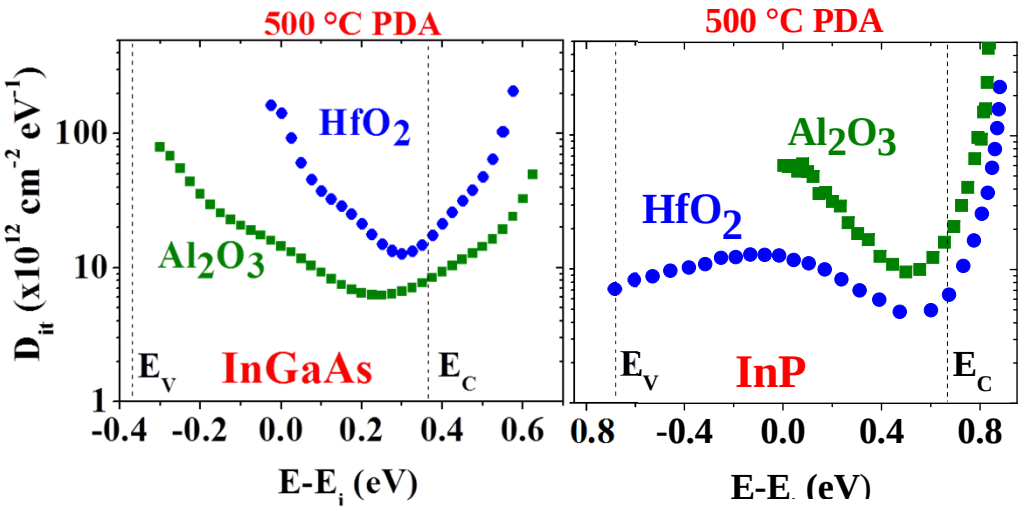


InP good choice for barrier:

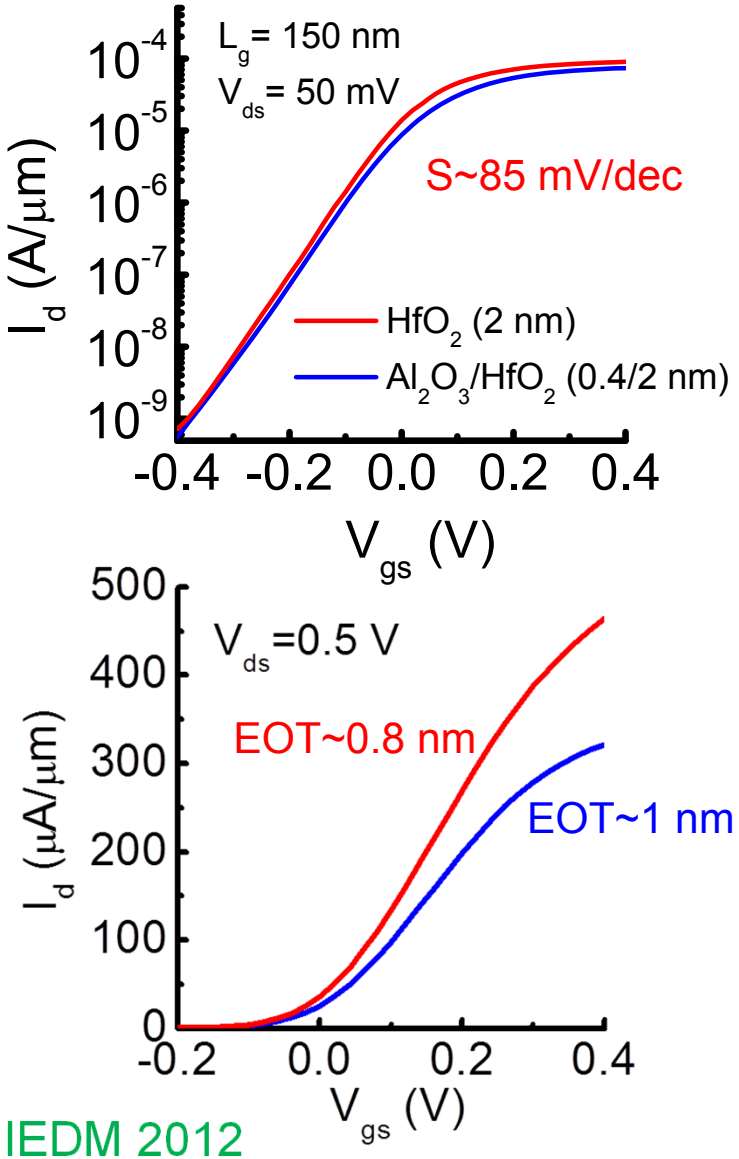
→ wide E_g, lattice matched to $In_{0.53}Ga_{0.47}As$

Urabe, ME 2011

HfO_2 vs. Al_2O_3 in buried-channel MOSFETs



Galatage - UT Dallas, 2012

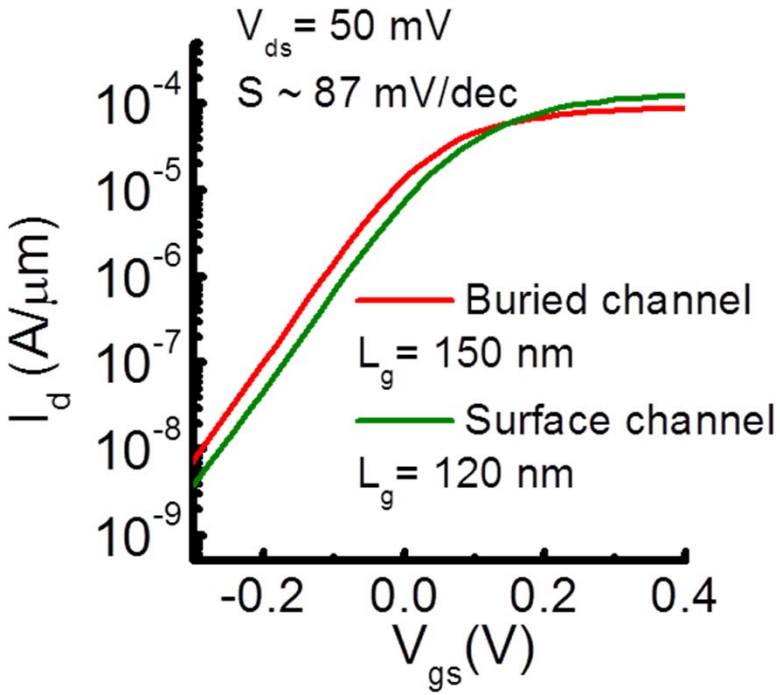


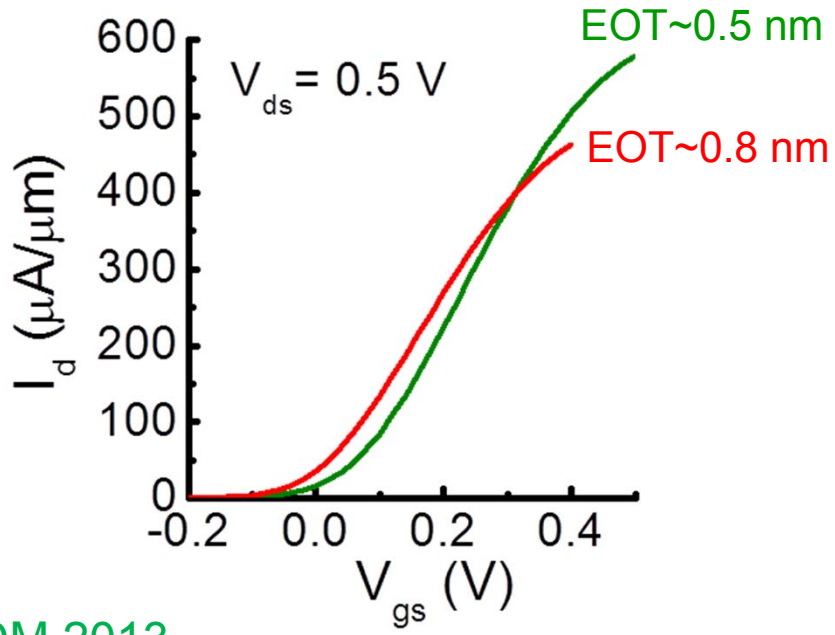
HfO_2 (2 nm) directly on InP (1 nm):

- Low D_{it} close to E_c
- Steep subthreshold swing
- Low I_{off} (nA/μm range)

Lin, IEDM 2012

HfO_2 in surface-channel MOSFETs

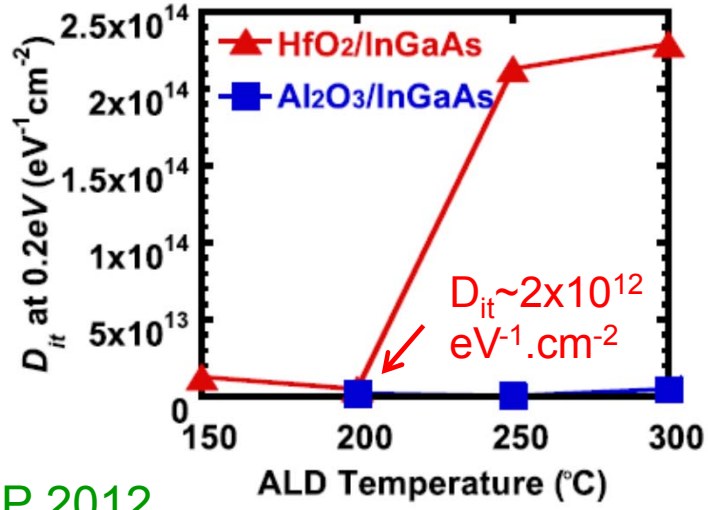




Lin, IEDM 2013

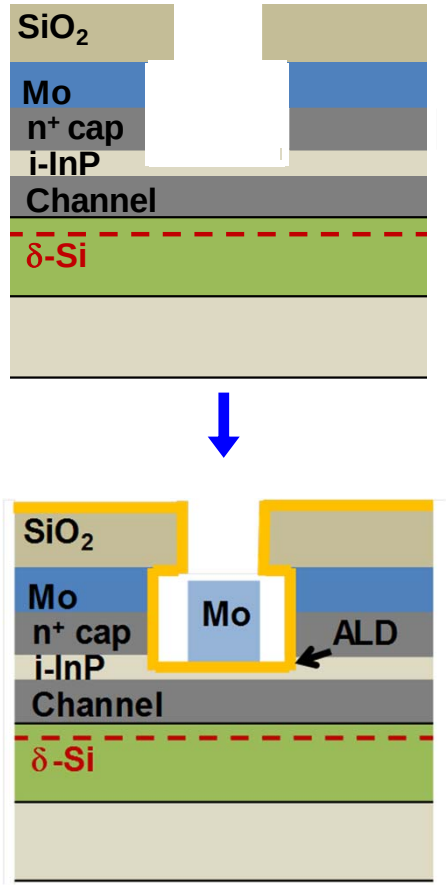
HfO_2 (2.5 nm) directly on InGaAs:

- Comparable S as buried-channel device
- EOT ↓ → I_d ↑
- Low ALD temperature key

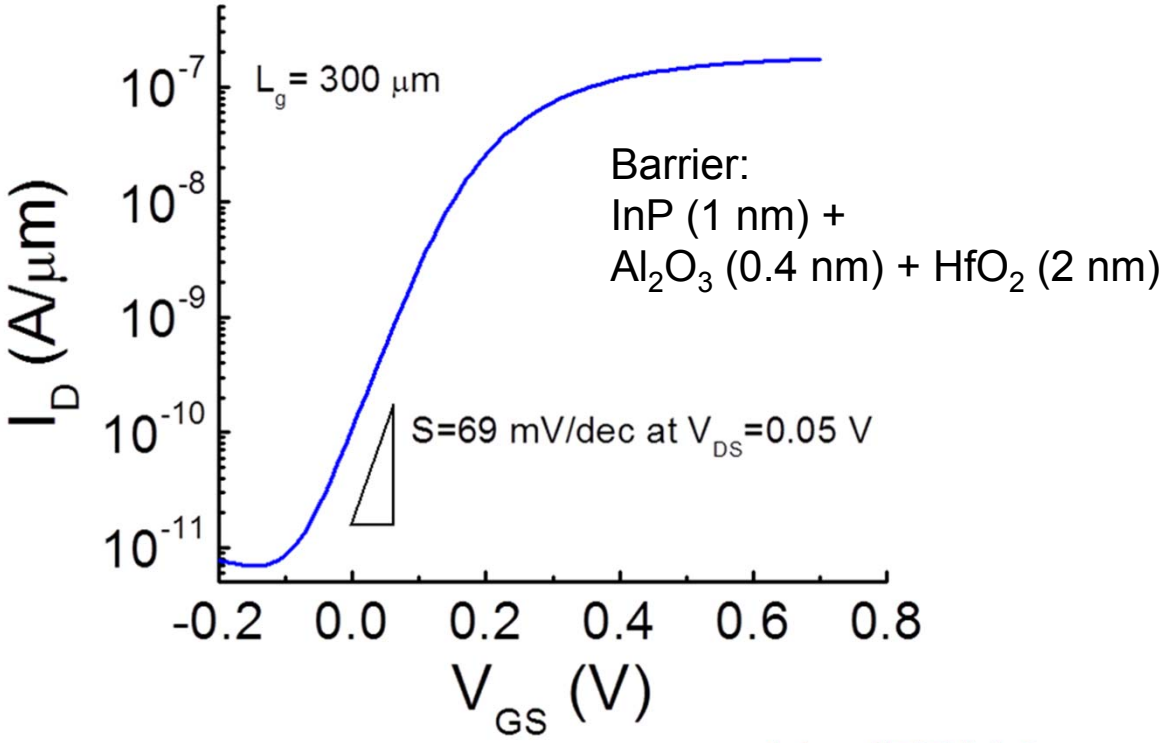


Suzuki, JAP 2012

Pristine interface for high MOS quality



Semiconductor surface exposed immediately before MOS formation



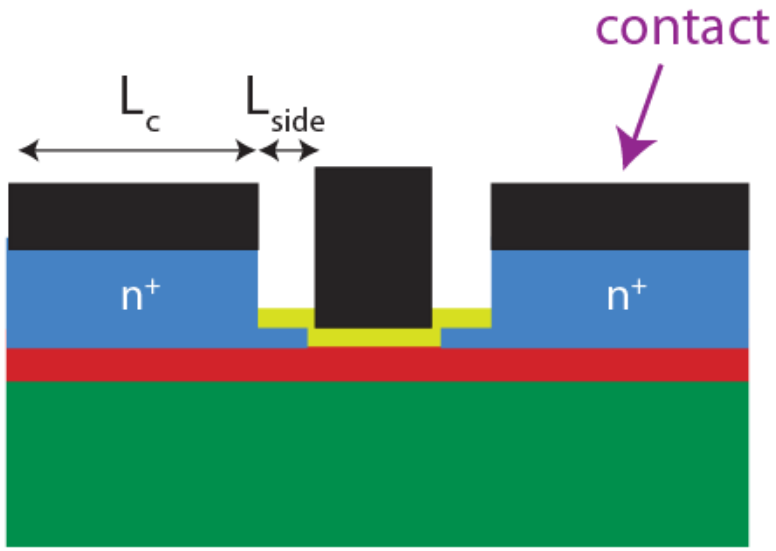
Lin, IEDM 2012

- S = 69 mV/dec at V_{DS} = 50 mV
- Close to lowest S reported in any III-V MOSFET: 66 mV/dec [Radosavljevic, IEDM 2011]

Technology issue #2: ohmic contacts

Challenge: nanometer-scale ohmic contacts with low R_c

- Tiny (L_c < 30 nm)
- Low contact resistance (R_c < 50 Ω.μm)
- Self-aligned to gate (L_{side} < 10 nm)

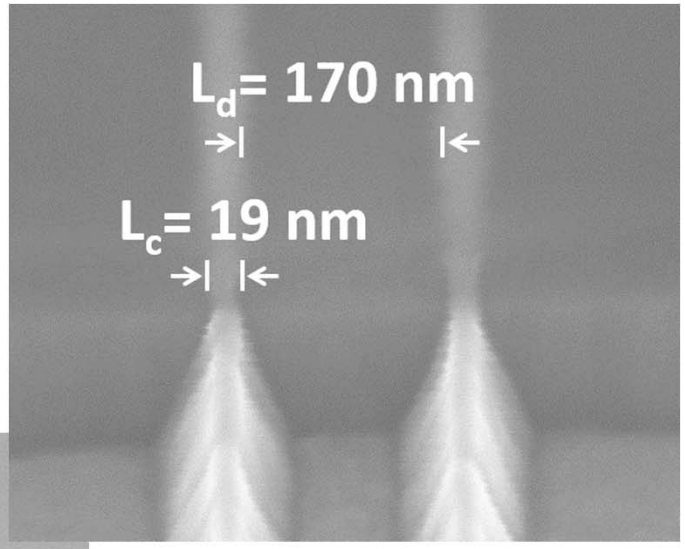


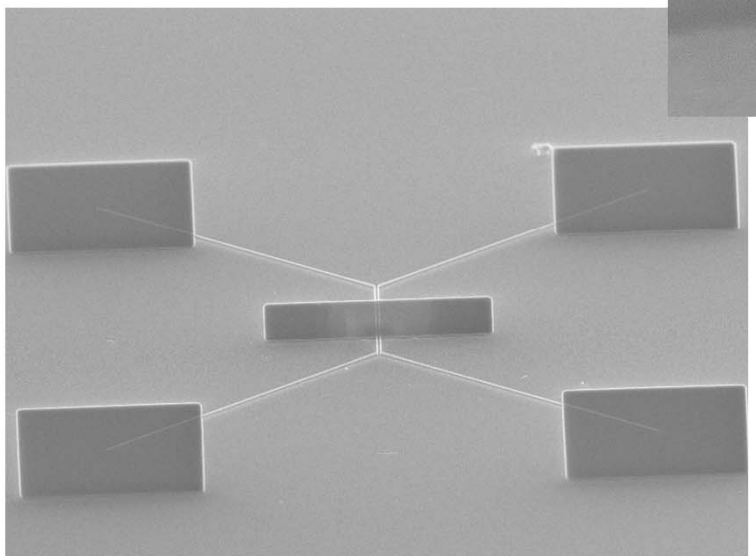
Contact-first process for Mo-InGaAs ohmic contacts

Fabrication process:

- Surface cleaning
- Mo deposition
- E-beam lithography
- Mo RIE
- Mesa isolation
- Pad metallization
- Contact anneal

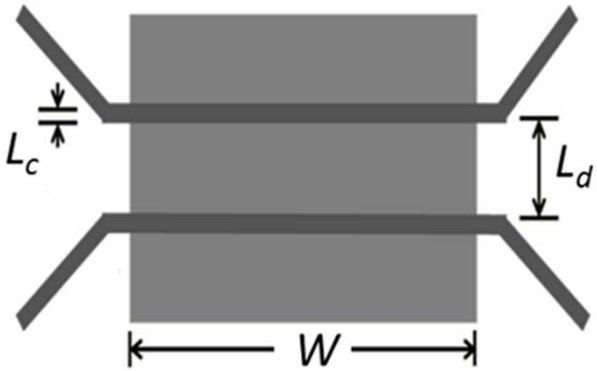
Lu, EDL 2014

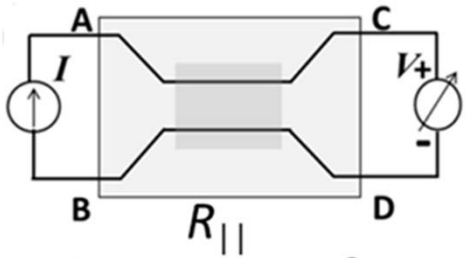


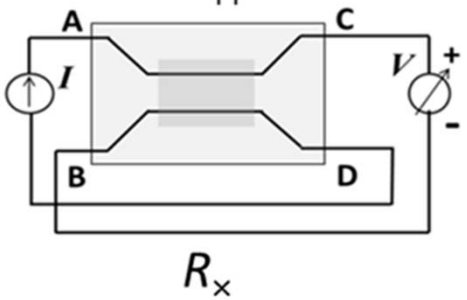


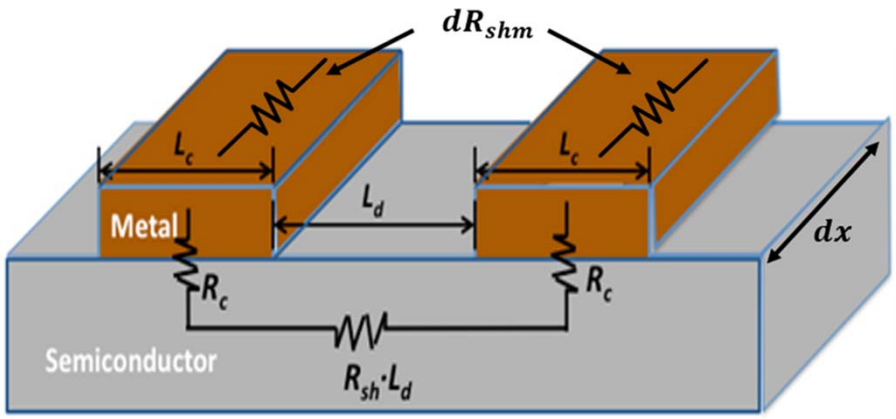
- Achieved contacts with length down to 19 nm
- Contact-first process preserves high-quality interface

New "nano-TLM" test structure to characterize short contacts









$$R_{||} = \frac{R_{TLM}}{L_{Tx}} \operatorname{csch}\left(\frac{W}{L_{Tx}}\right)$$

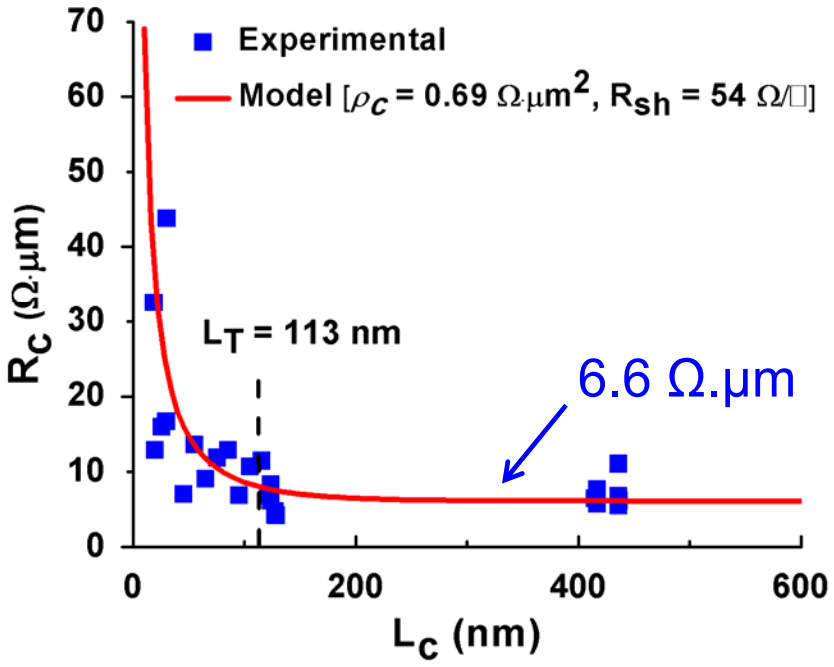
$$R_{\times} = \frac{R_{TLM}}{2L_{Tx}}\left[\operatorname{csch}\left(\frac{W}{L_{Tx}}\right) + \coth\left(\frac{W}{L_{Tx}}\right)\right] - \frac{R_{shm}W}{2L_c}$$

Lu, EDL 2014

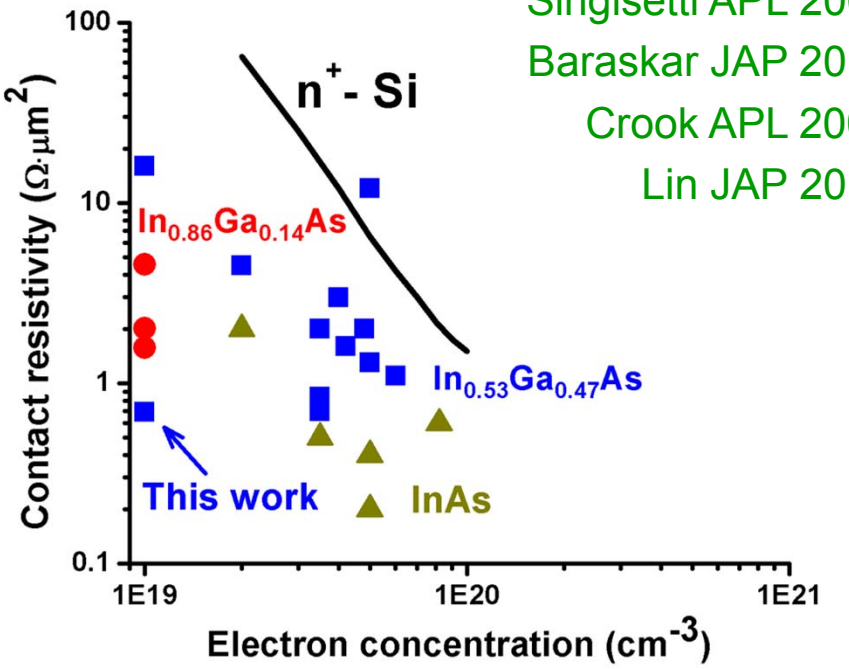
Decouples impact of metal resistance on short contacts

Nanometer-scale Mo-InGaAs contacts

Mo on n^+-$In_{0.53}Ga_{0.47}As$:



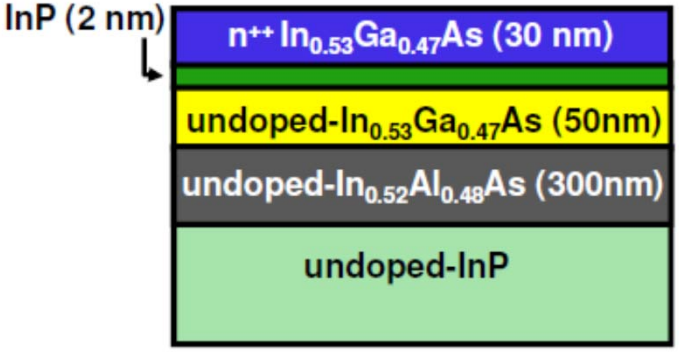
Dormaier JVSTB 2012
Singisetti APL 2008
Baraskar JAP 2013
Crook APL 2007
Lin JAP 2013



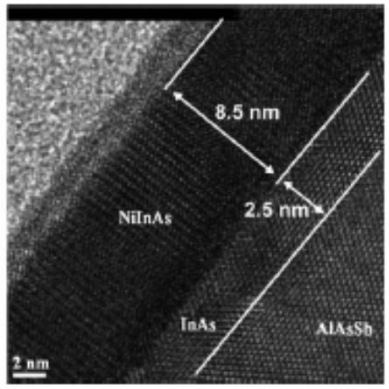
- R_c blows up for very small contacts with $L_c < L_t$ = 113 nm
- R_c ~ 40 Ω.μm for L_c ~ 20 nm
- Average ρ_c = 0.69 Ω.μm^2
- Contacts thermally stable up to 400°C

Lu, EDL 2014

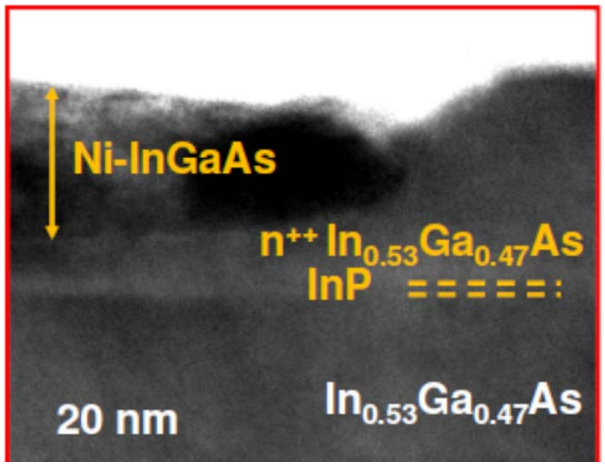
Ni-InGaAs ohmic contact

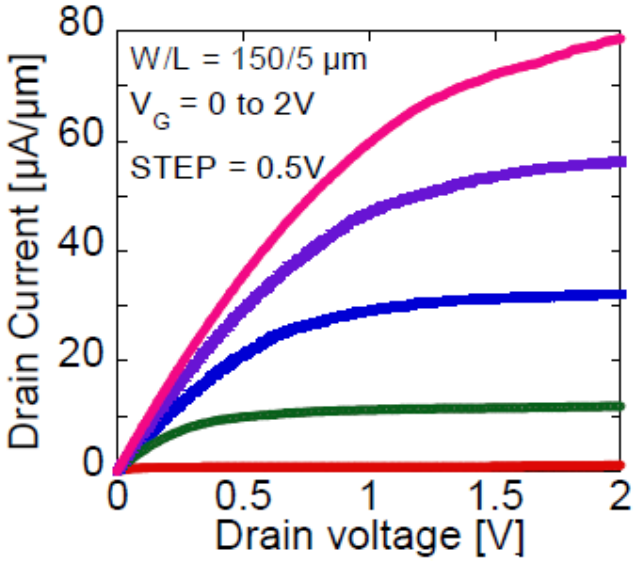


Subramanian, JES 2012



Oxland, EDL 2012





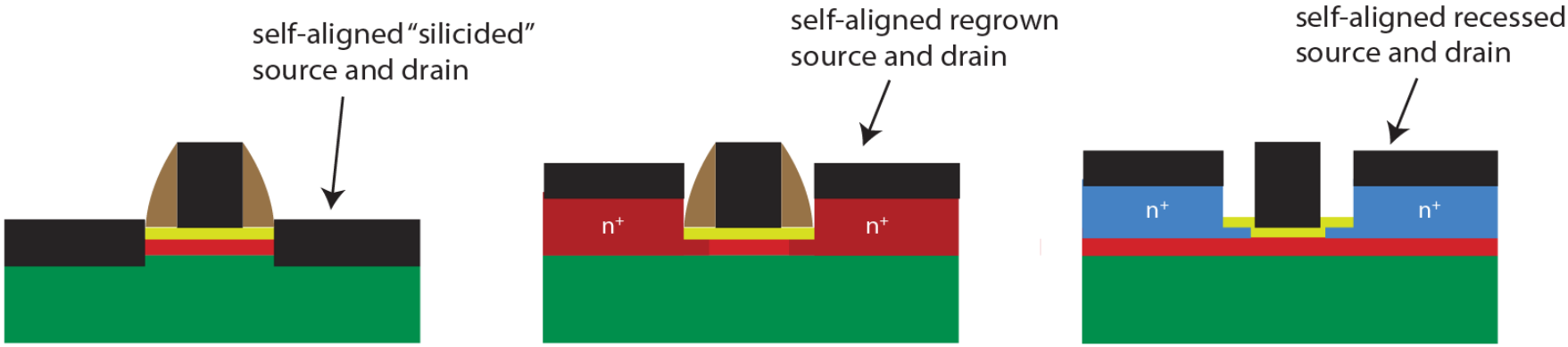
Kim, IEDM 2010

- Ni diffused into InGaAs at 250°C
- Ni-InGaAs formed
- Unreacted Ni removed using HCl-based selective etchant
- R_c ~ 50 Ω.µm demonstrated [Kim VLSI Tech 2013]

Technology issue #3: self-aligned MOSFET architectures

Challenge: ohmic contacts very closely spaced from gate

- Design of access region
- Must maintain high-quality MOS interface and low R_c



Gate-first process: "silicided" S/D

Hill, IEDM 2010
Kim, VLSI Tech 2013

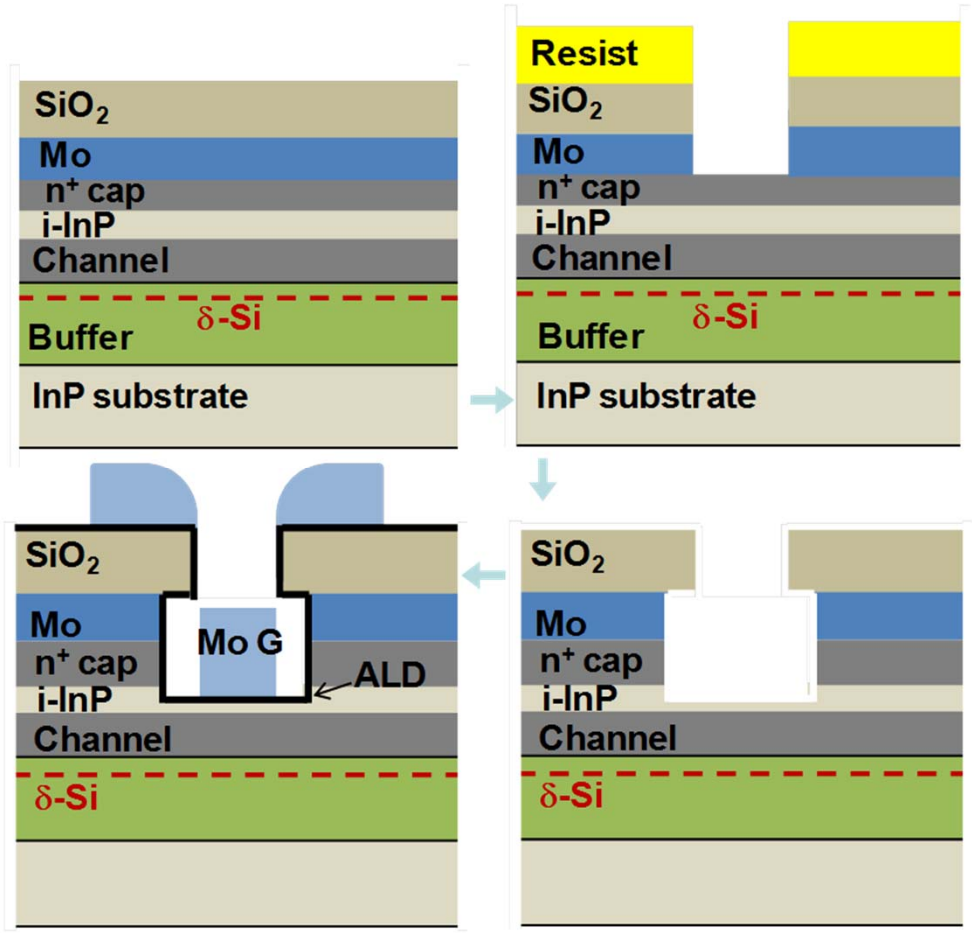
Gate-first process: regrown S/D

Egard, IEDM 2011
Zhou, IEDM 2012
Lee, VLSI Tech 2013

Gate-last process: recessed S/D

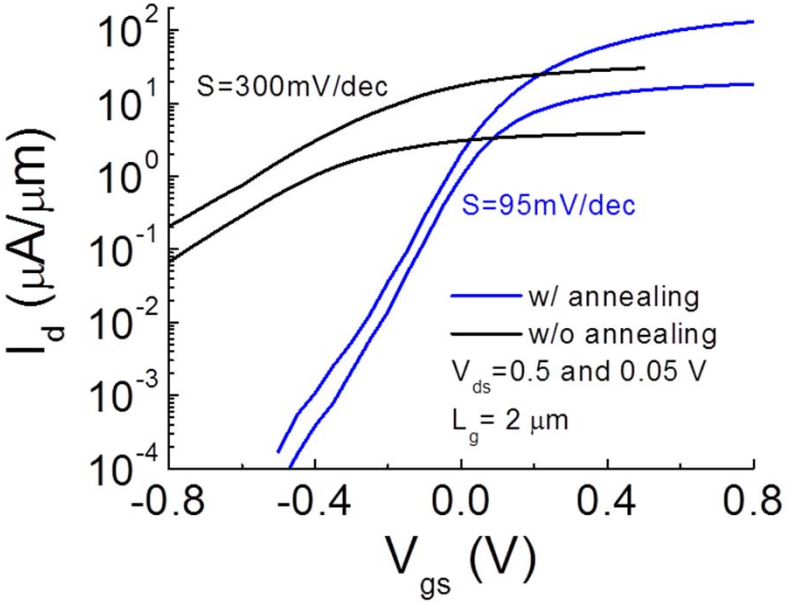
Radosavljevic, IEDM 2009
Lin, IEDM 2012

Gate-last self-aligned InGaAs MOSFETs



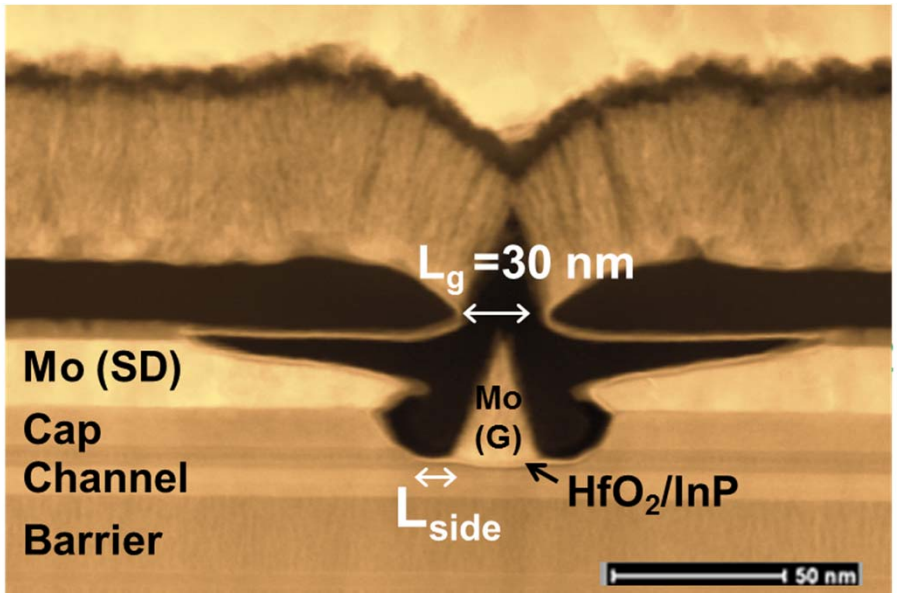
Lin, IEDM 2012

- Ohmic contact first (Mo)
- Extensive RIE (F-based)
- Interface exposed immediately before gate stack formation
- Process designed to be compatible with Si fab
- RIE damage annealed at 340°C:



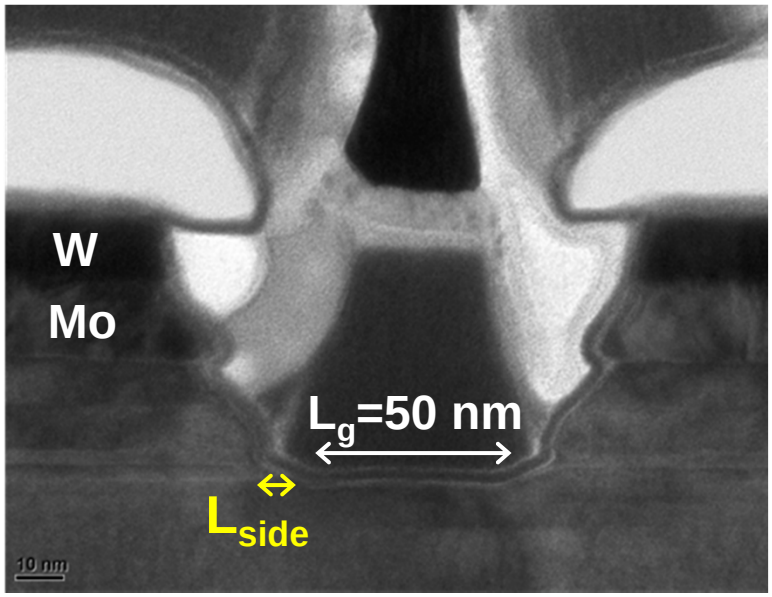
Gate-last self-aligned InGaAs MOSFETs

Lin, IEDM 2012



- Buried-channel (EOT~0.8 nm)
- Wet semiconductor etch
- L_{side} ~ 30 nm

Lin, IEDM 2013



- Surface-channel (EOT~0.5 nm)
- Dry semiconductor etch + digital etch of cap
- L_{side} ~ 5 nm
- W overlayer on Mo contacts

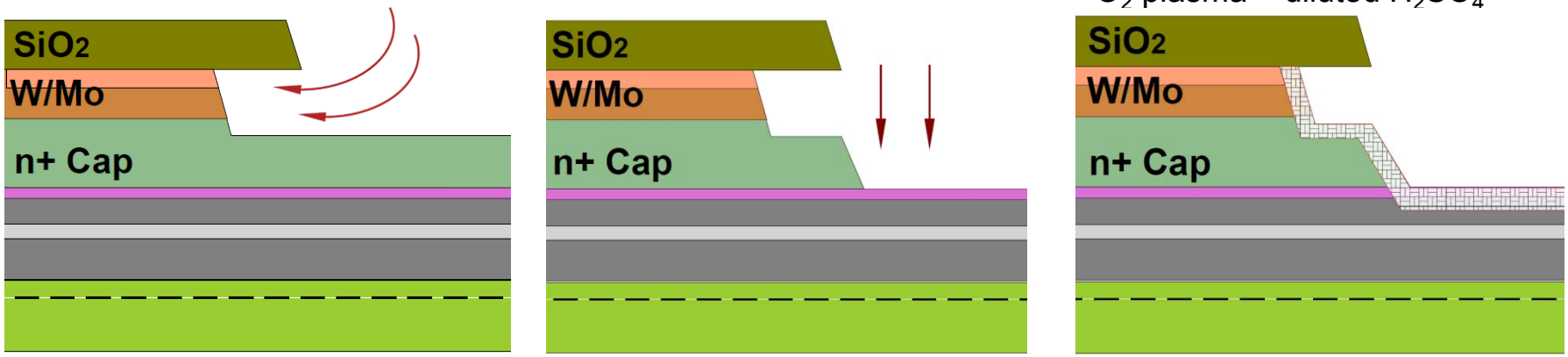
3-step gate recess process

CF_4+O_2 RIE

Cl-based RIE

Digital etch

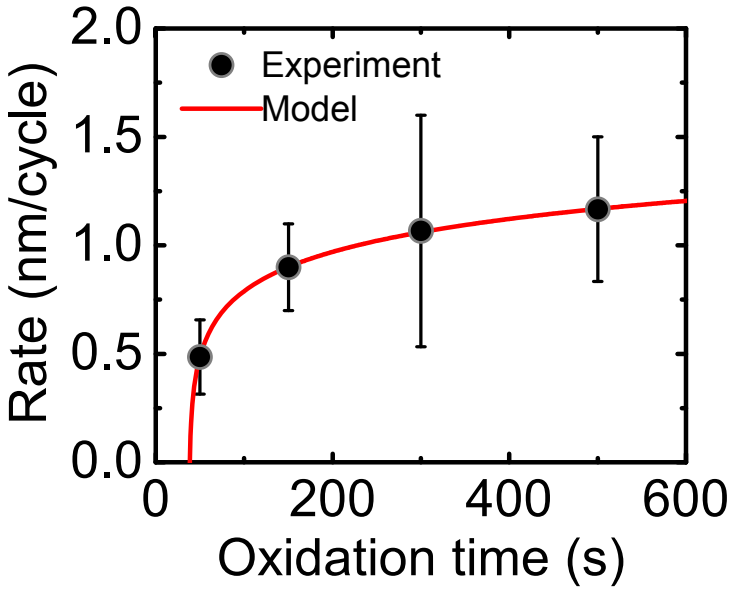
O_2 plasma + diluted H_2SO_4



Waldron, IEDM 2007

Digital etch:

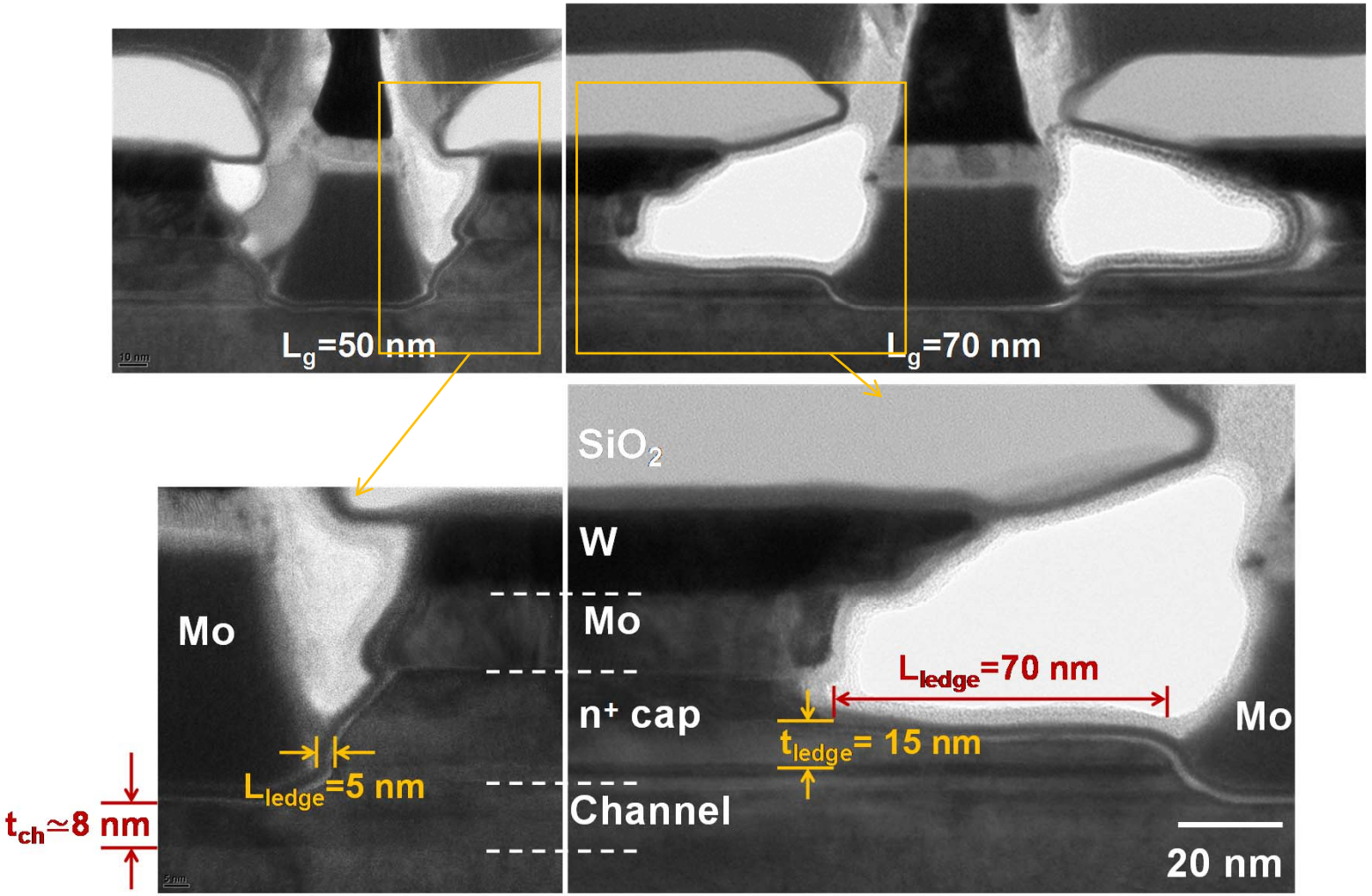
- Separately, oxidation and etching are self-limited
- Etch rate: ~1 nm/cycle



Lin, EDL 2014

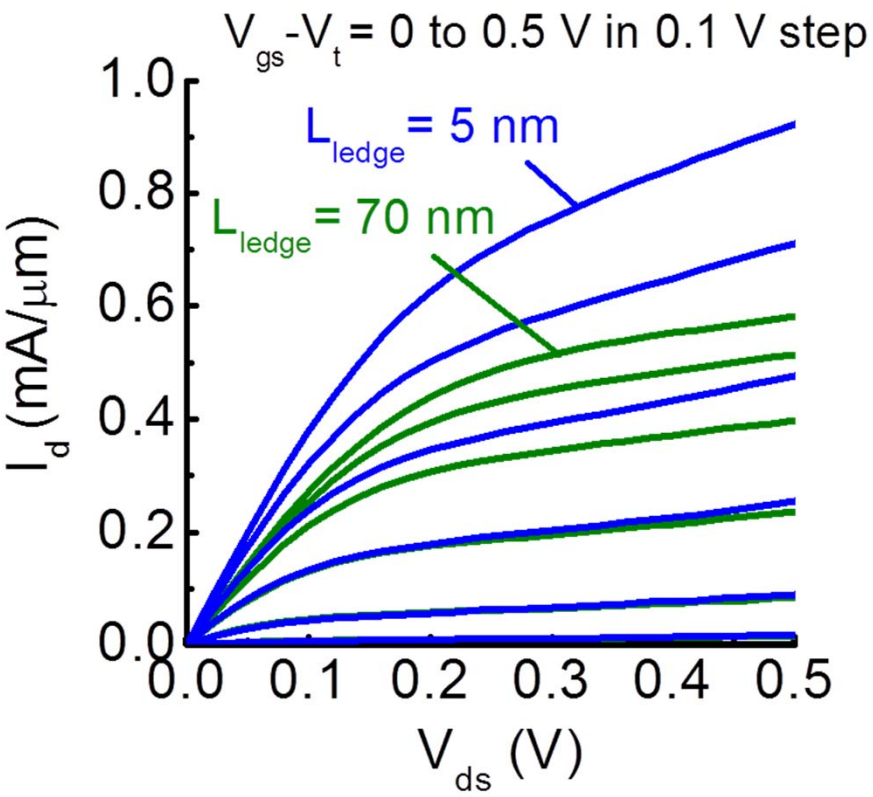
Cross-section TEM of Gen III FETs

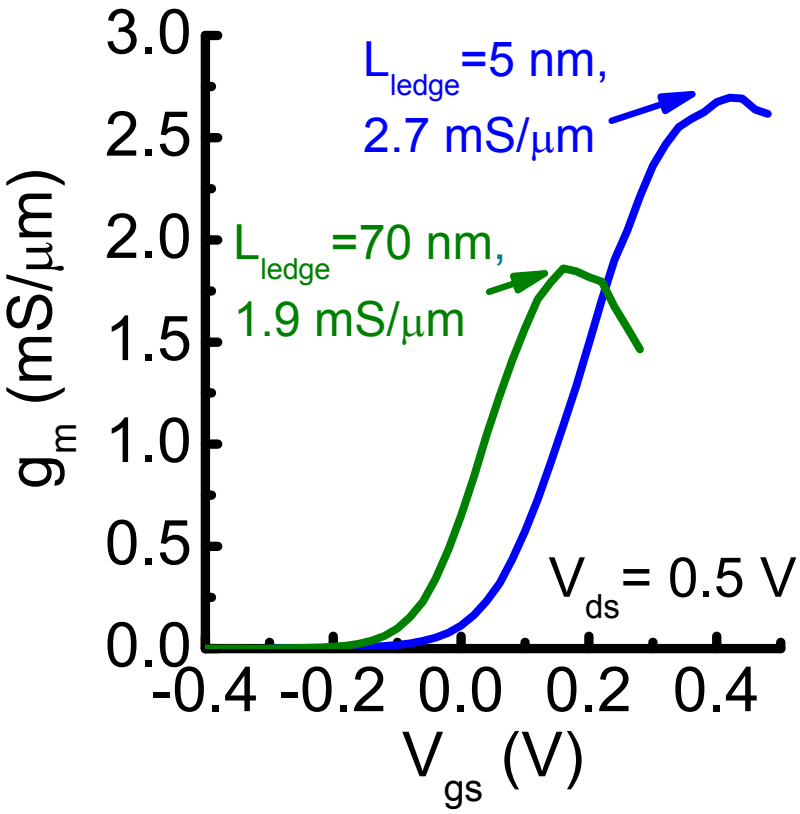
Short Ledge *Long Ledge*



- Surface channel: $In_{0.7}Ga_{0.3}As$ / InAs / $In_{0.7}Ga_{0.3}As$ = 1/2/5 nm
- Gate oxide: HfO_2 , thickness =2.5 nm (EOT~0.5 nm)

I-V Characteristics of surface-channel InGaAs MOSFETs (L_g=70 nm)



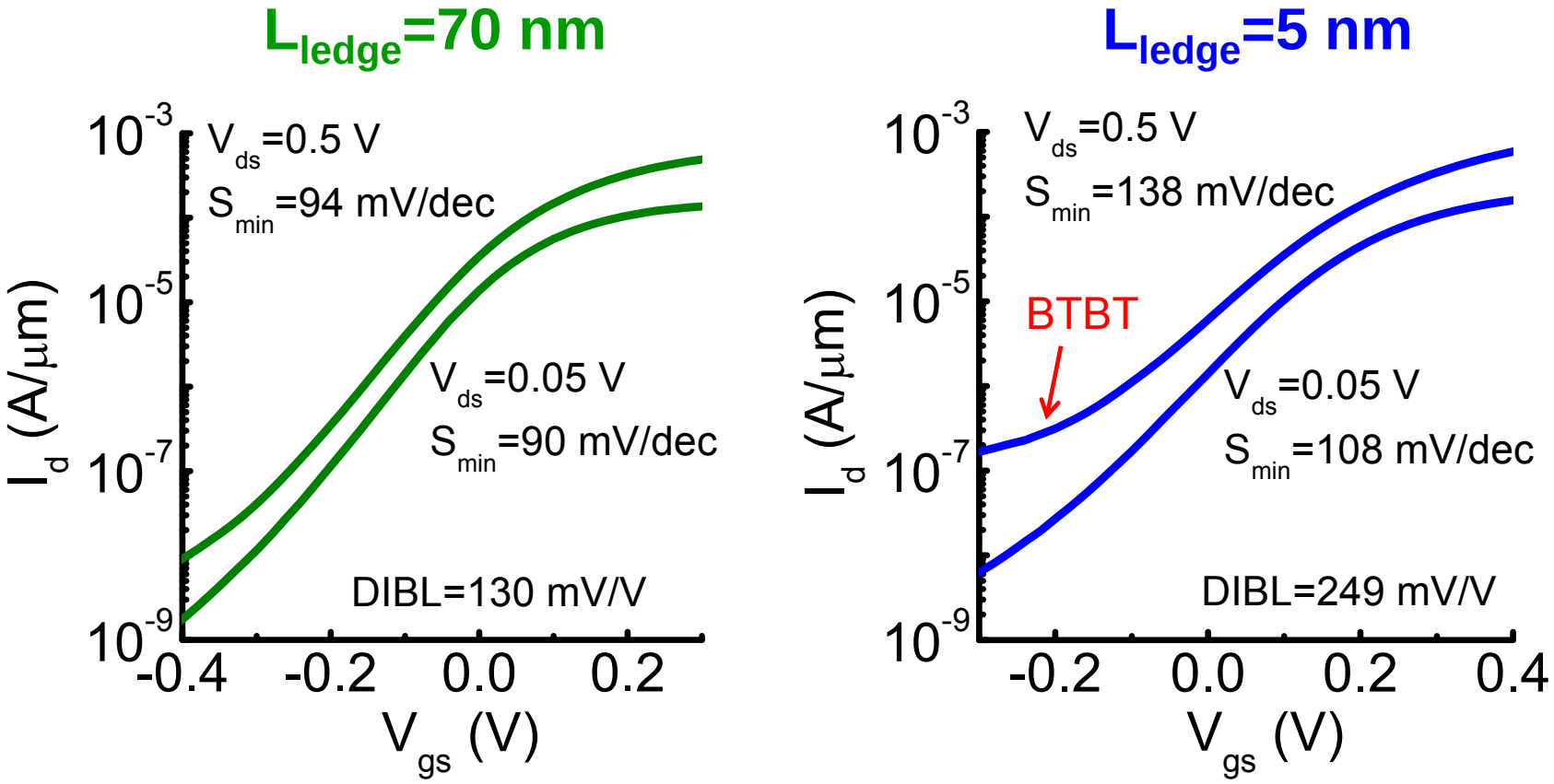


In L_{ledge}=5 nm MOSFET:

- Record g_m achieved: 2.7 mS/μm (V_{DS}=0.5 V)
- R_{on}=220 Ω.μm

Lin, IEDM 2013

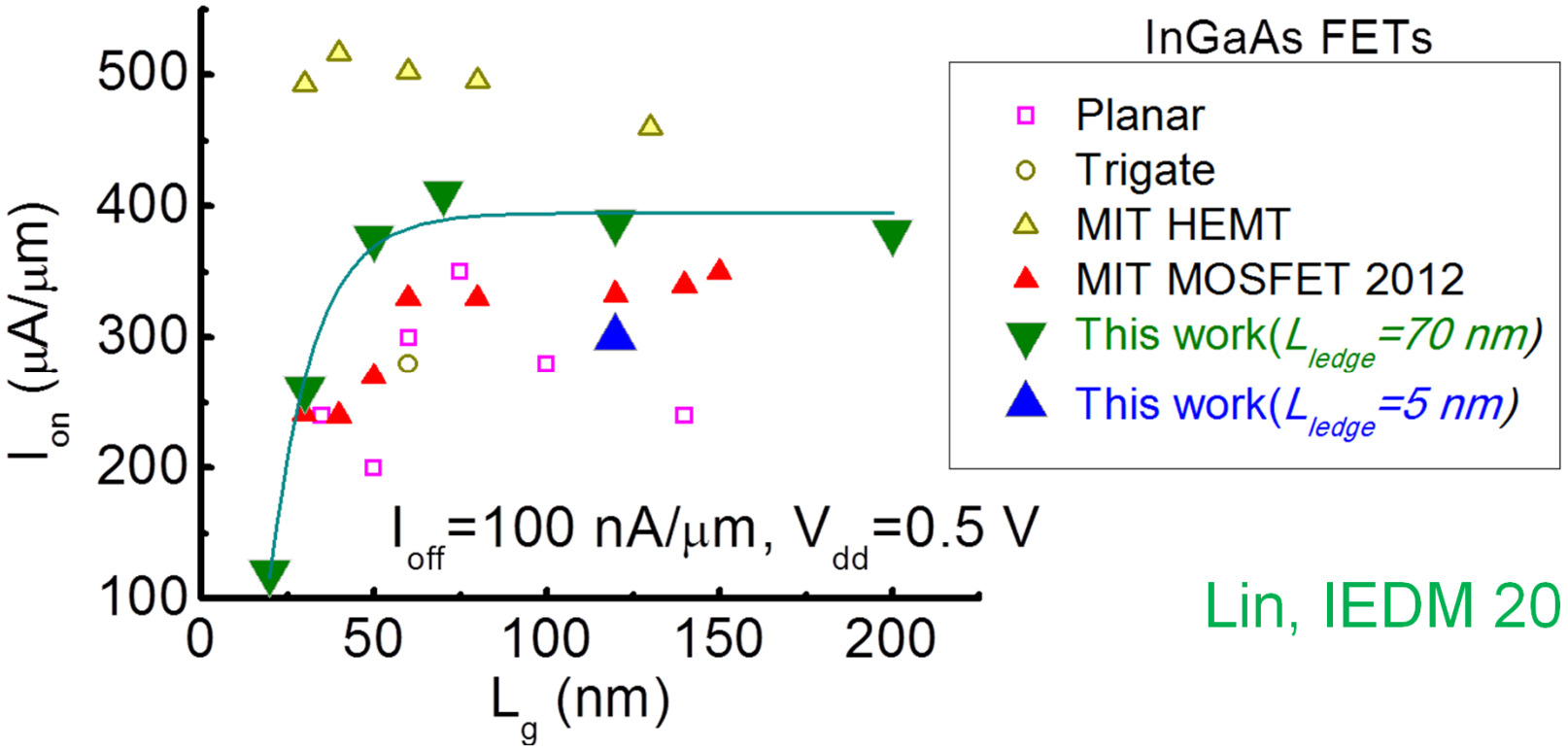
Subthreshold characteristics (L_g=70 nm)



- In L_{ledge} = 70 nm, S = 94 mV/dec at V_{ds} = 0.5 V
- I_g < 10 pA/μm over entire voltage range
  - Further EOT scaling possible

Lin, IEDM 2013

Benchmarking: I_{on} at I_{off}=100 nA/μm, V_{dd}=0.5 V

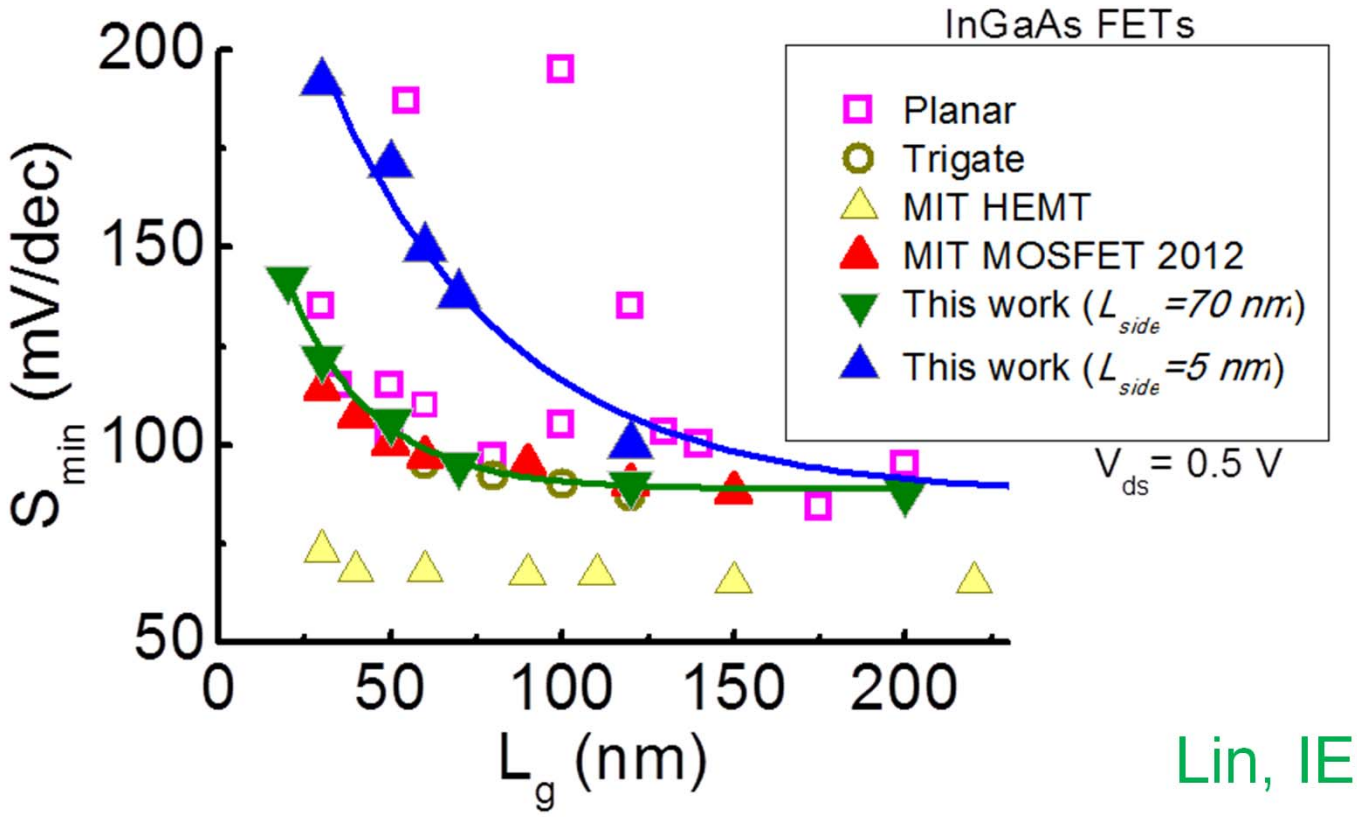


Lin, IEDM 2013

In L_{ledge}=70 nm MOSFET:

- Record I_{on}: 410 μA/μm (at I_{off}=100 nA/μm, V_{DS}=0.5 V)

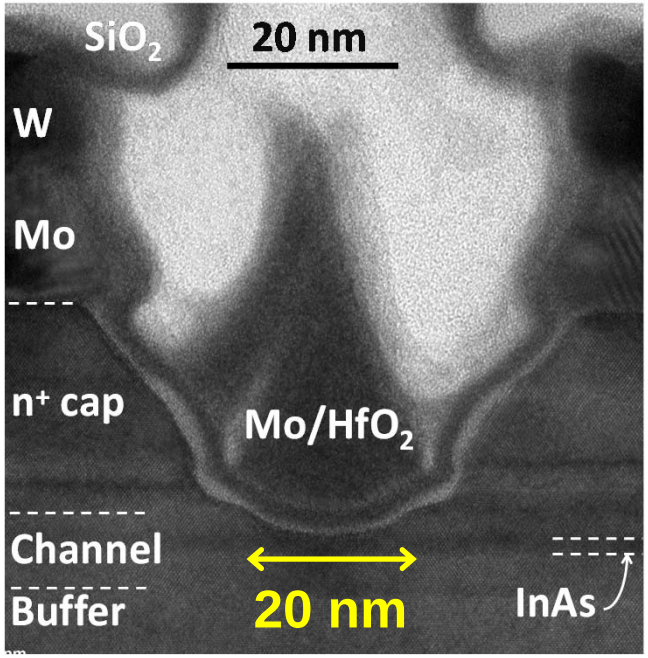
Benchmarking: Subthreshold Swing

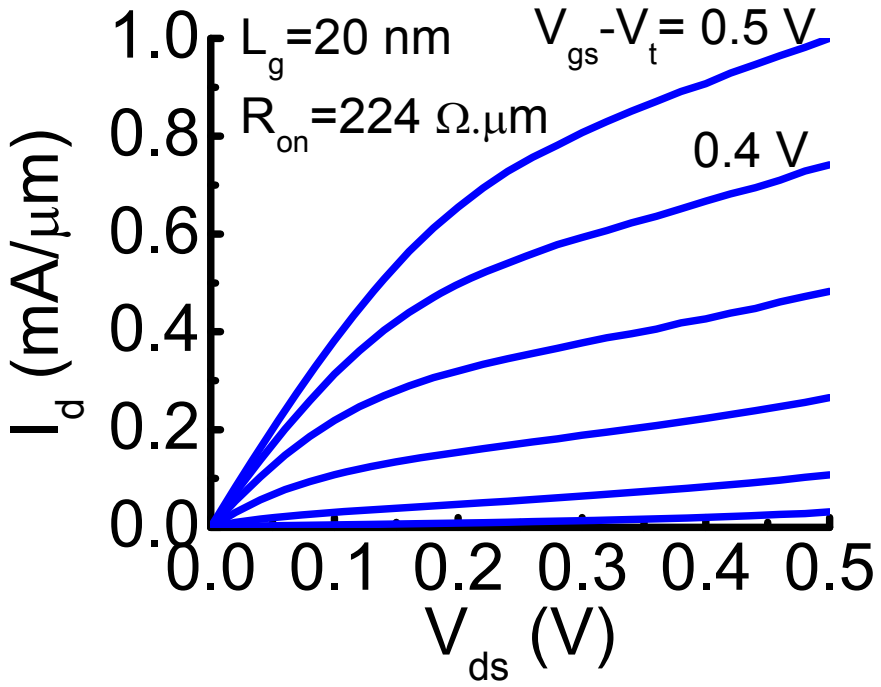


Lin, IEDM 2013

L_{ledge}=70 nm MOSFETs match S of best III-V MOSFET

L_g=20 nm Self-aligned InGaAs MOSFET





L_g = 20 nm, L_{ledge}= 5 nm MOSFET

→ tightest III-V MOSFET ever made?

Lin, IEDM 2013

Technology issue #4: 3D MOSFETs

Challenge: acceptable I_{ON} and SCE on a small-footprint

- Planar design does not provide enough “electrostatic integrity”
- Need tighter channel control through 3D device design

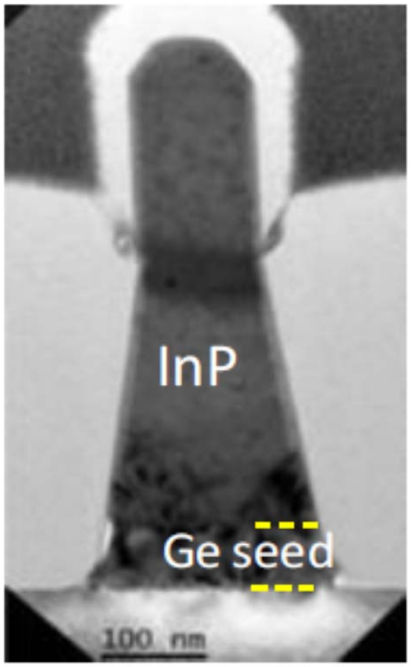
Planar MOSFET

Tri-gate MOSFET

Wu, IEDM 2009
Radosavljevic, IEDM 2010
Chin, EDL 2011
Radosavljevic, IEDM 2011

Fin formation

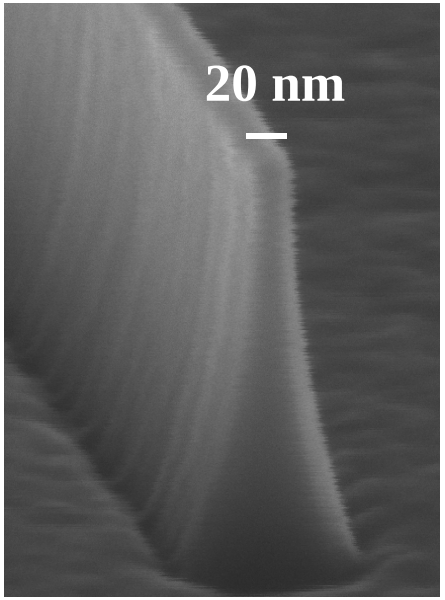
Direct fin growth by Aspect Ratio Trapping



- Some defects reach surface
- Inter-diffusion of dopant species

Fiorenza, ECST 2010
Waldron, ECST 2012

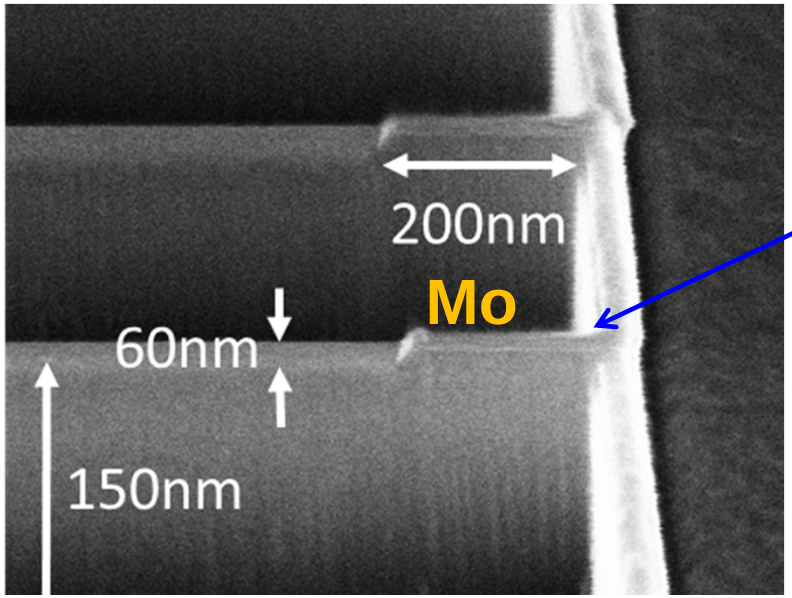
Fin etch by RIE + digital etch



- $BCl_3/SiCl_4$/Ar RIE chemistry
- Digital etch: self-limiting (2 nm/cycle)
- No notching in heterostructures

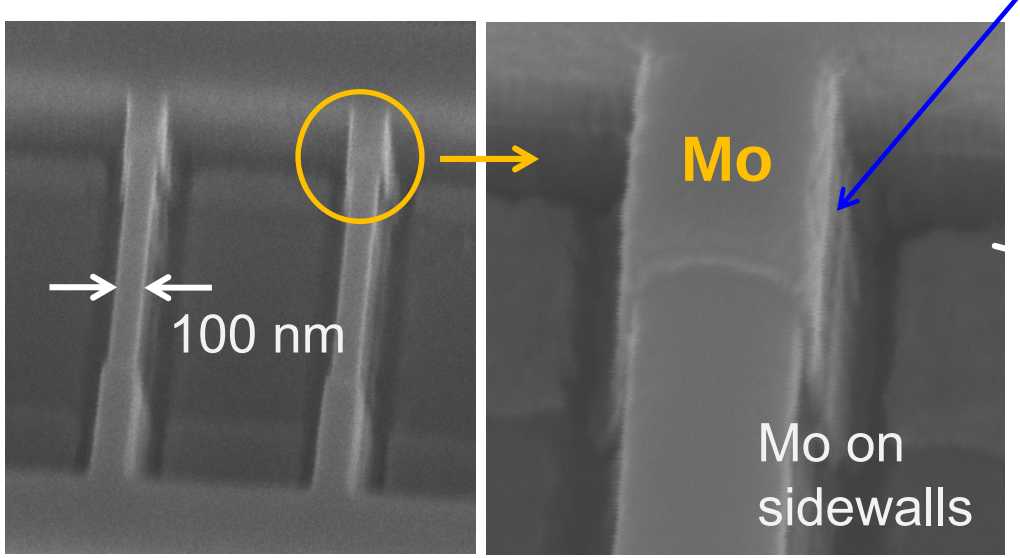
Zhao, IEDM 2013

Mo contacts to fin



- Mo-first process
- Mo used as mask for fin etch

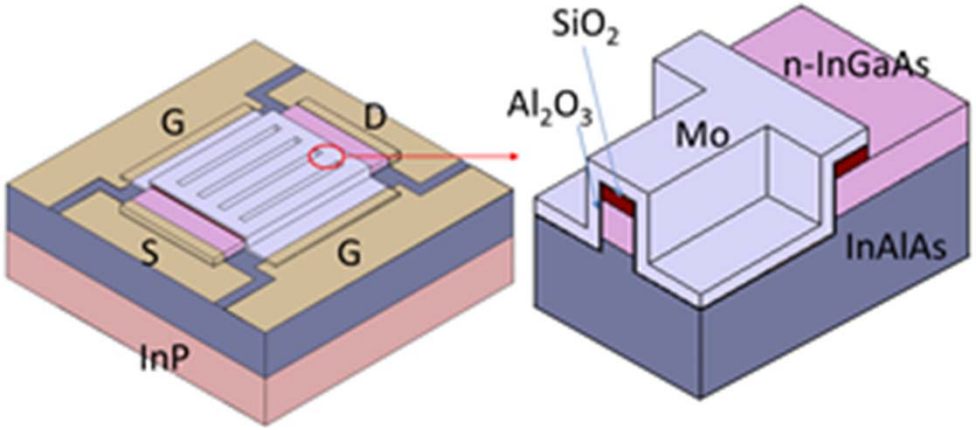
Mo sidewall contacts

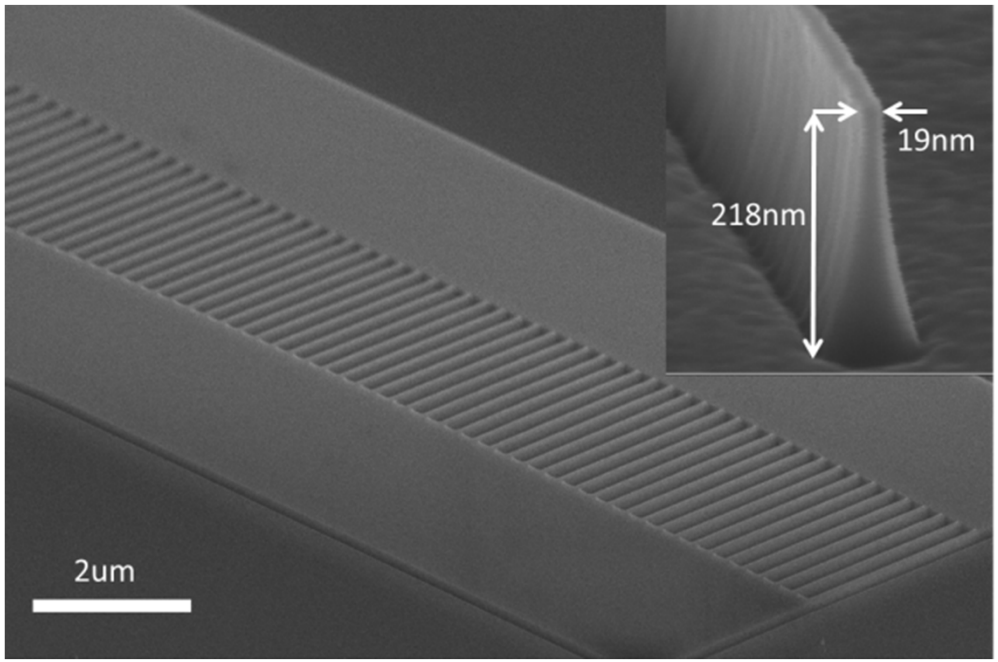


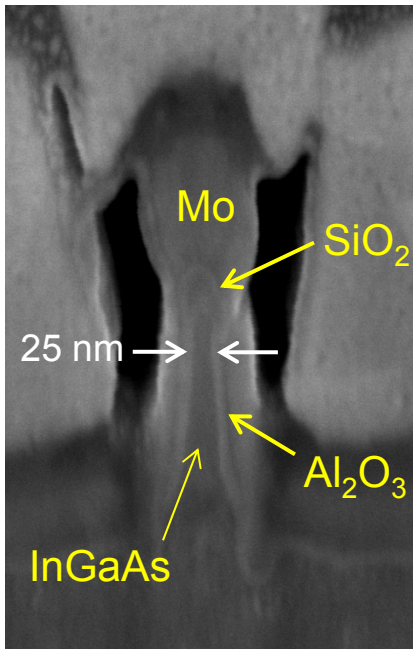
- With top Mo contact:
  - R_c ~ 7 Ω.μm
- With sidewall contact:
  - R_c ~ 12 Ω.μm

Fin double-gate sidewall MOSFET

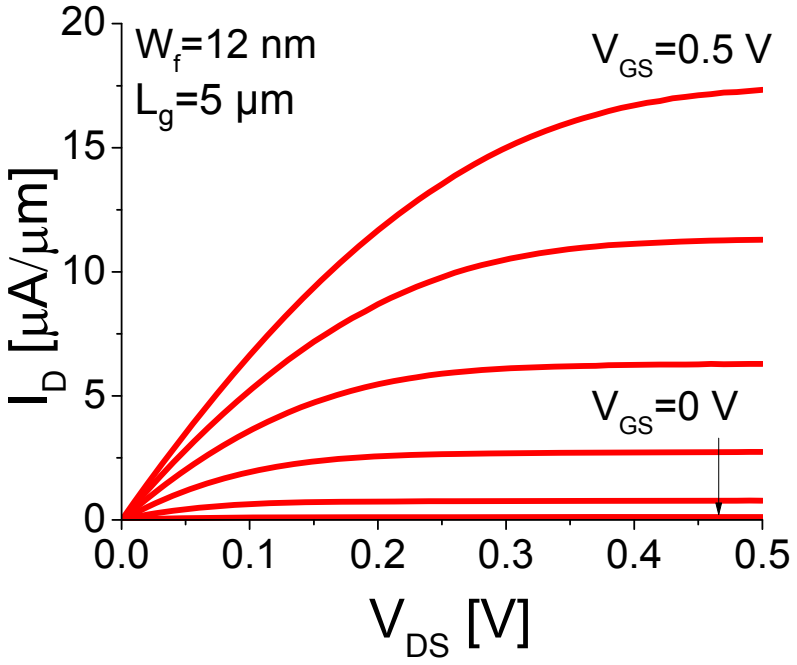
Double-gate sidewall MOSFET to study sidewall MOS quality

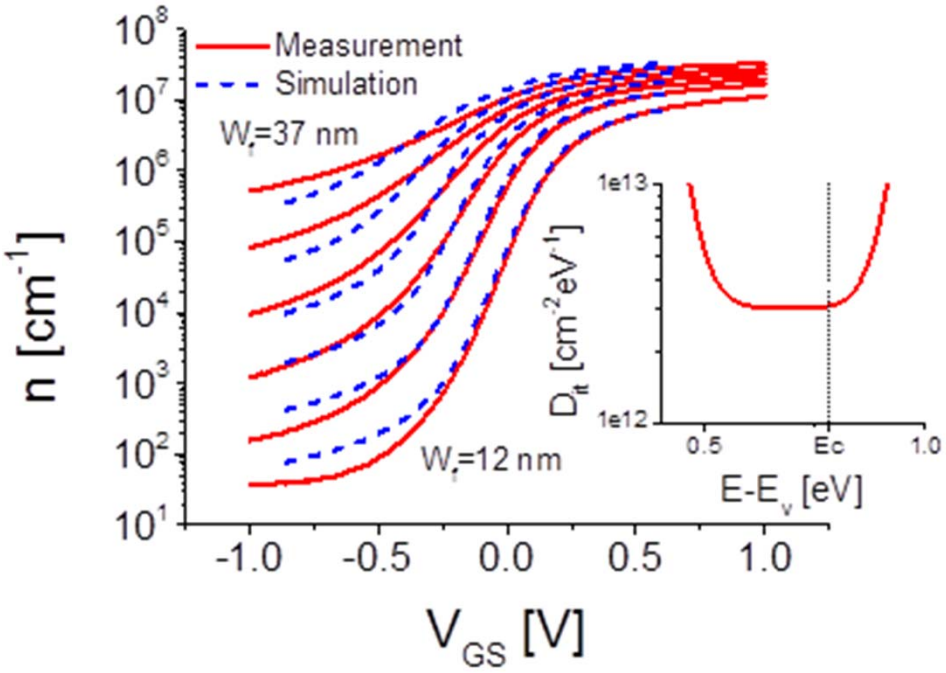






Fin double-gate sidewall MOSFETs
(very recent results)

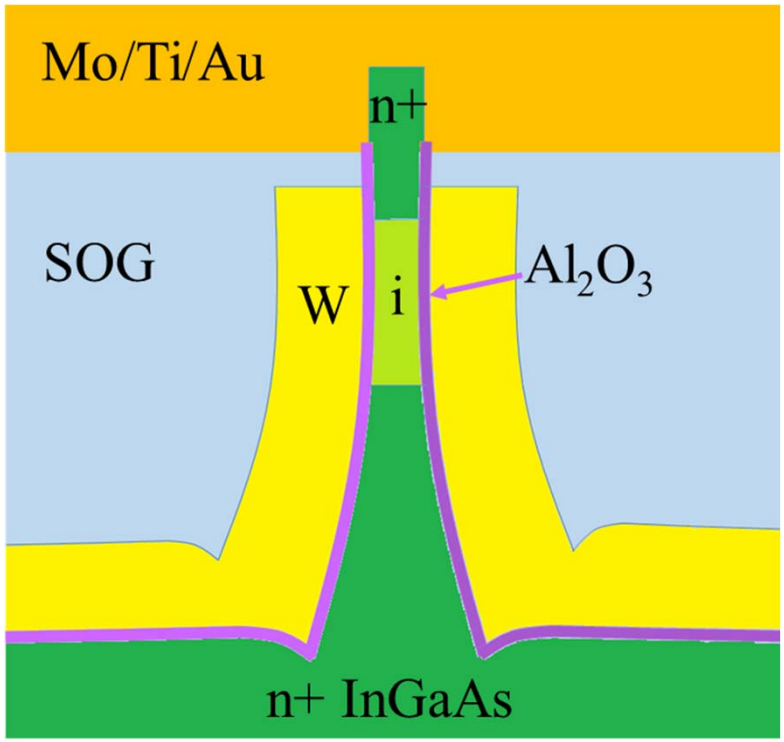




At sidewall: $D_{it,min} \sim 3 \times 10^{12}$ $eV^{-1}.cm^{-2}$

(preliminary)

Vertical nanowire InGaAs MOSFETs fabricated via top-down approach



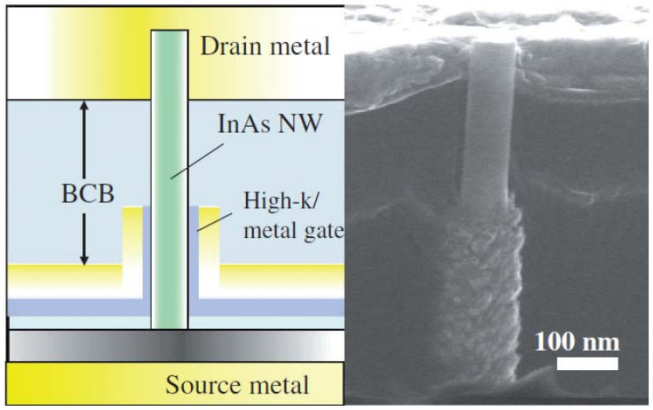
Zhao, IEDM 2013

- Nanowire MOSFET: ultimate scalable transistor
- Vertical NW: uncouples footprint scaling from L_g scaling

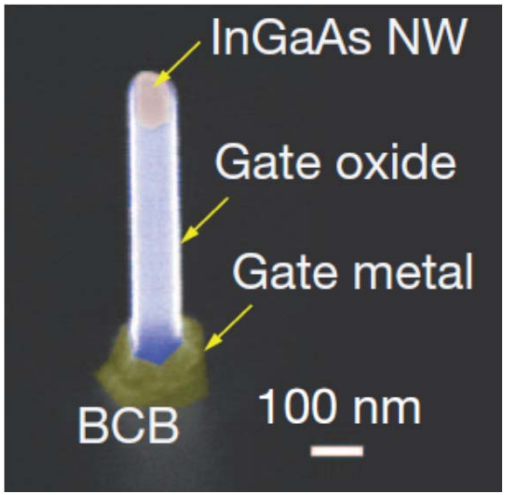
NW-MOSFET by *bottom-up* techniques

Impressive devices demonstrated, but…

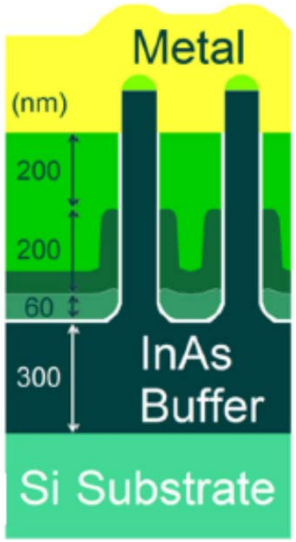
- Complex epi growth limits materials choice and layer design, or
- Au seed particles required



Tanaka, APEX 2010



Tomioka, Nature 2012

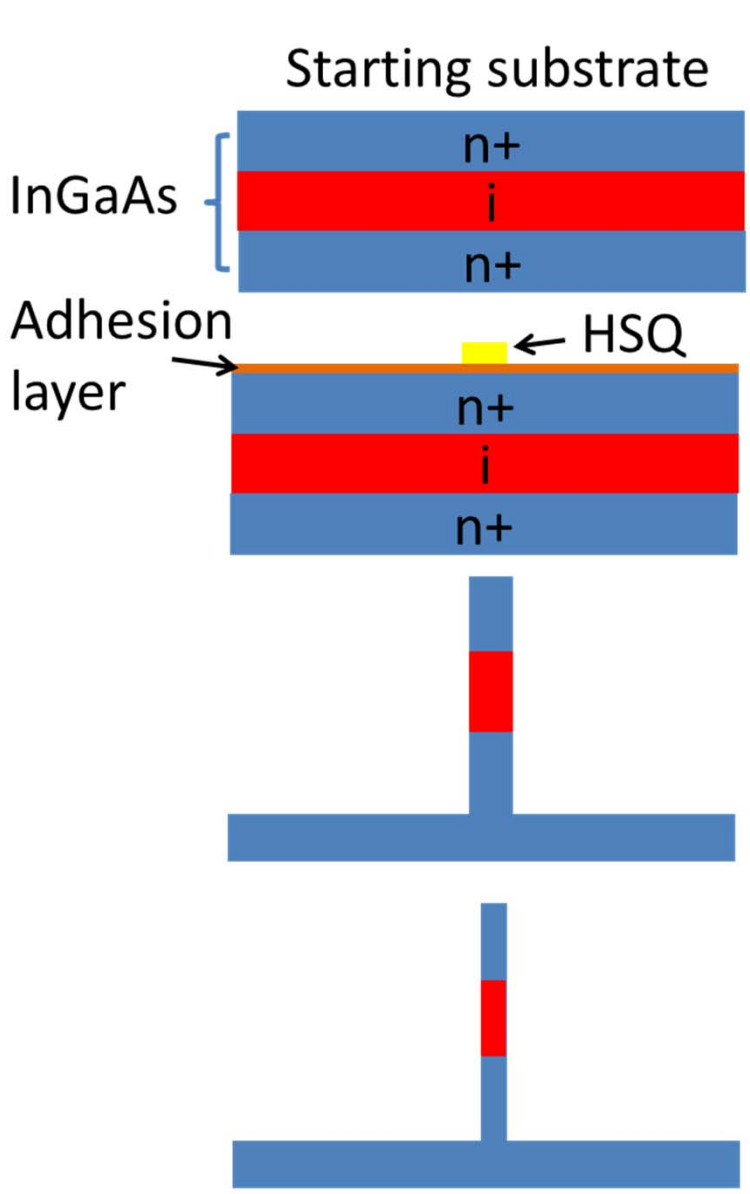


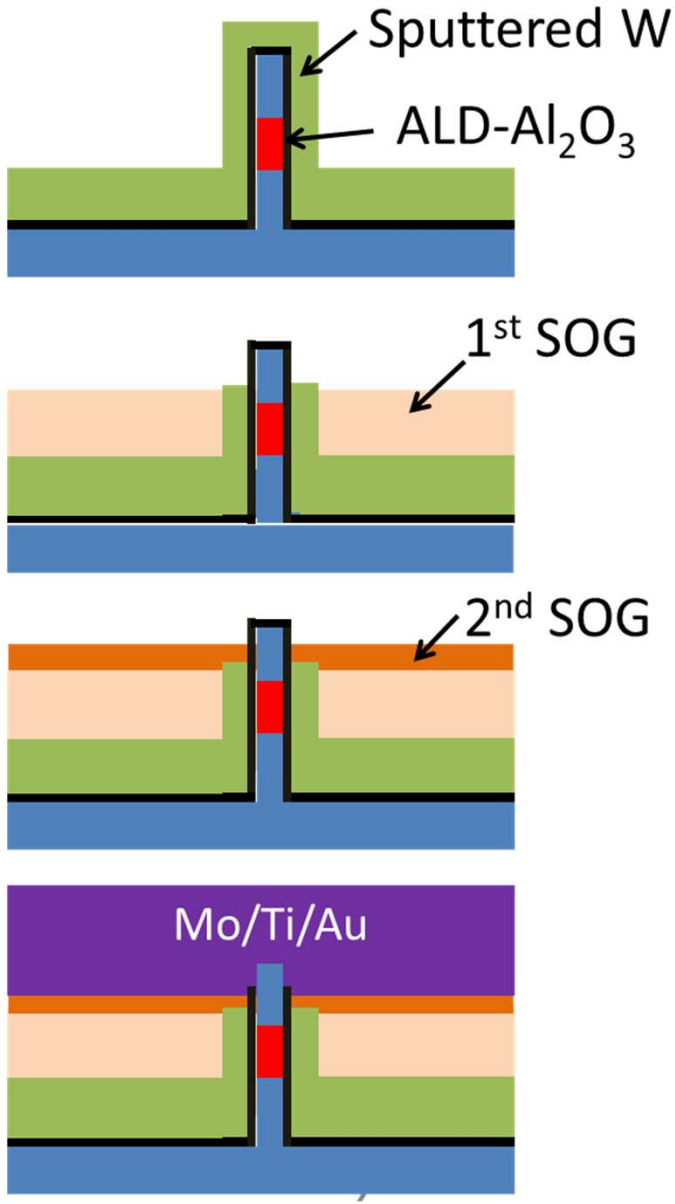
Persson, DRC 2012

Top-down approach: flexible and manufacturable

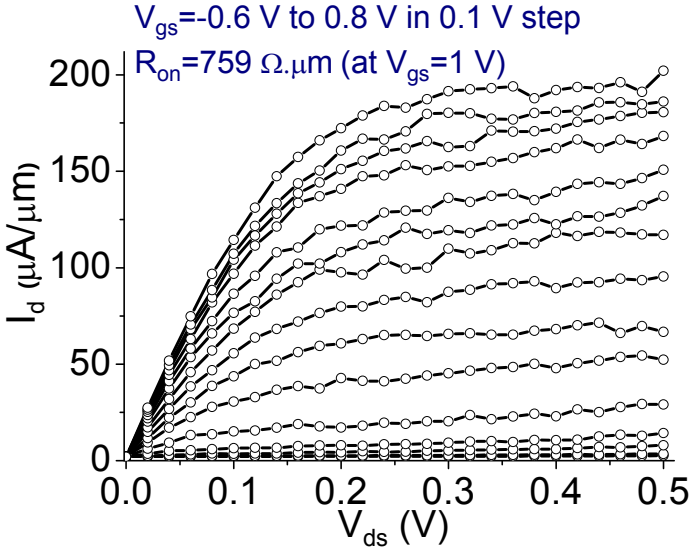
Tomioka, Nature 2012
Persson, DRC 2012

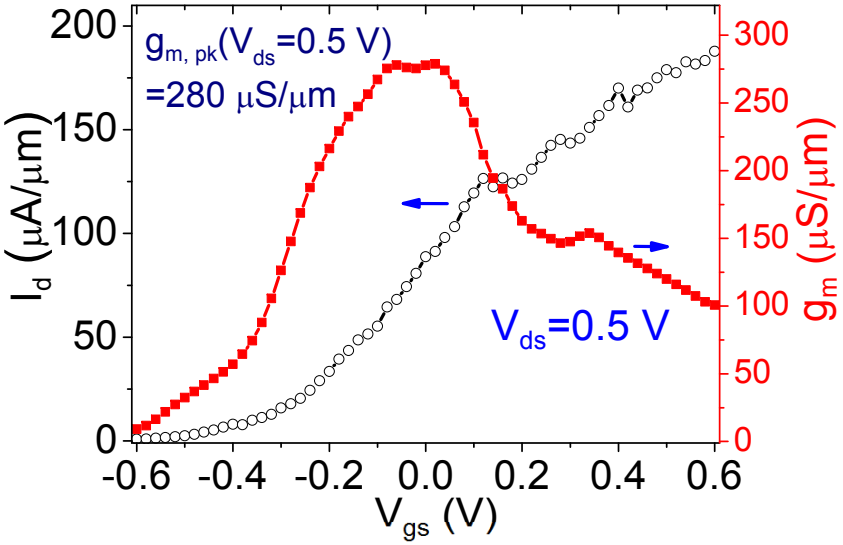
Process flow





NW-MOSFET I-V characteristics
D=30 nm



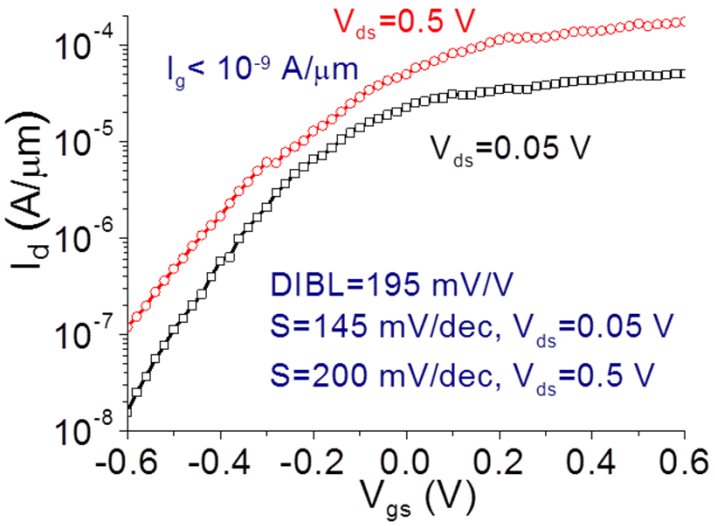


Single nanowire MOSFET:

- L_{ch}= 80 nm
- 4.5 nm Al_2O_3 (EOT = 2.2 nm)

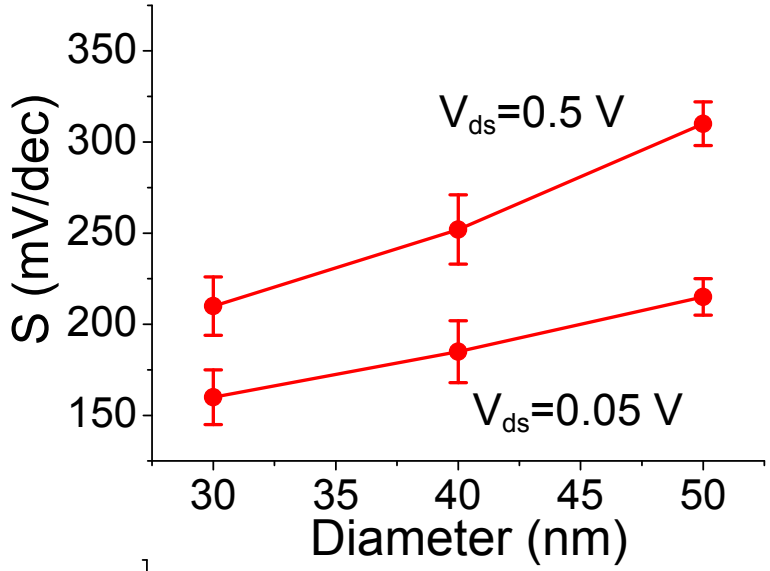
At V_{DS}=0.5 V:

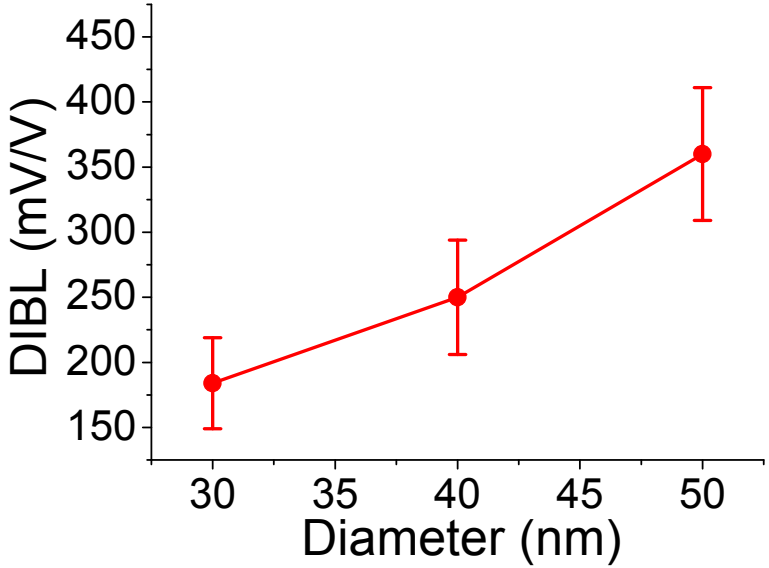
- $g_{m,pk}$=280 μS/μm
- R_{on}=759 Ω.μm

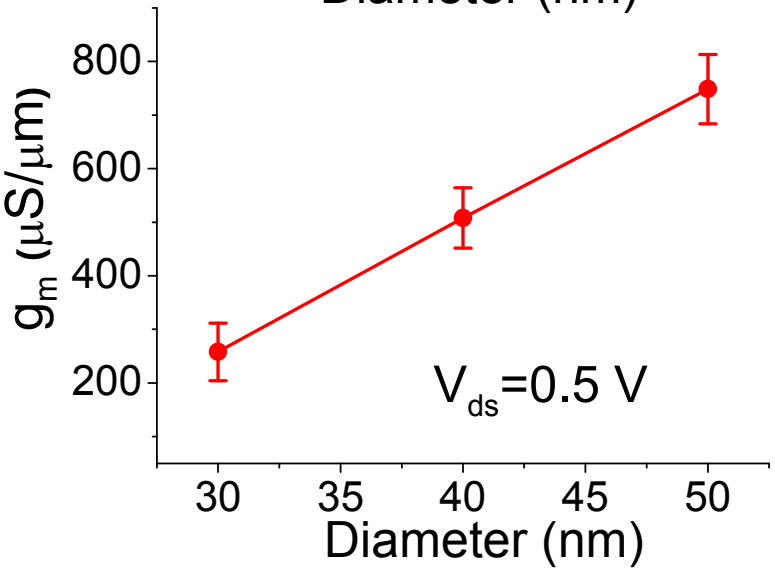


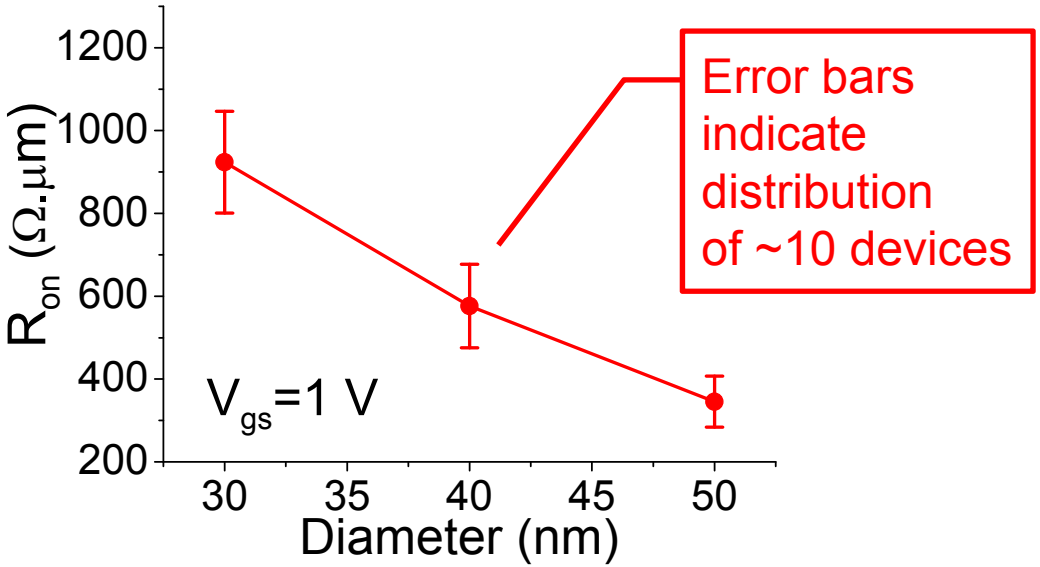
Zhao, IEDM 2013

Impact of nanowire diameter





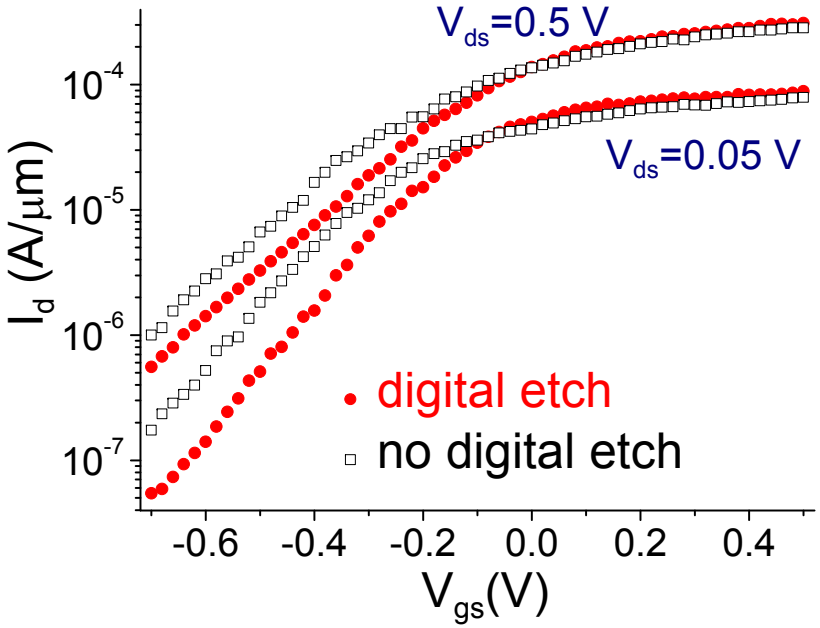


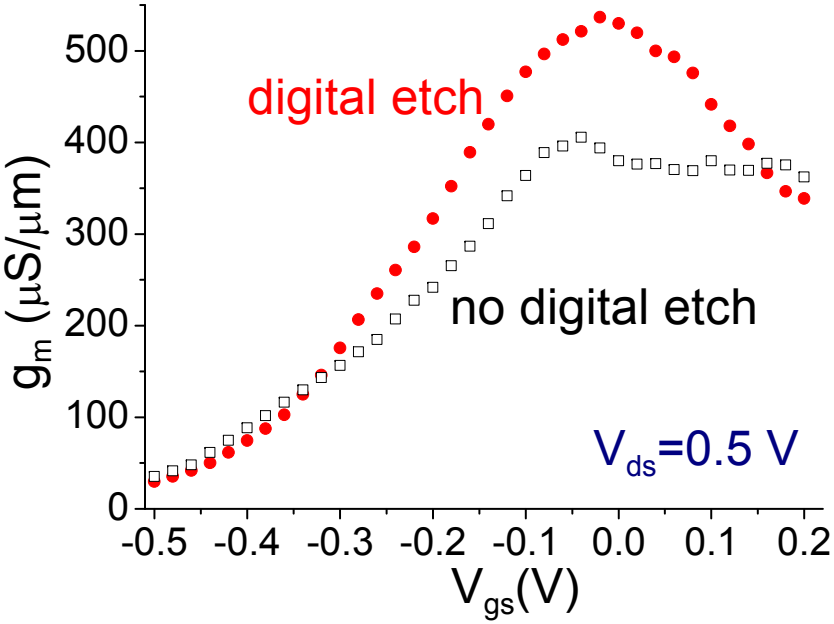


D↓ → S ↓, DIBL ↓, g_m ↓, R_{on} ↑

Impact of digital etch

Single nanowire MOSFET: D= 40 nm (final diameter)

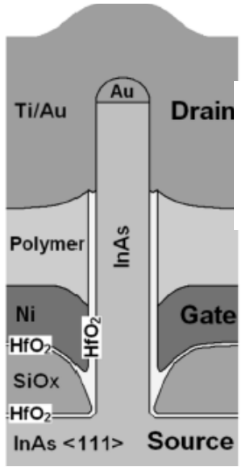




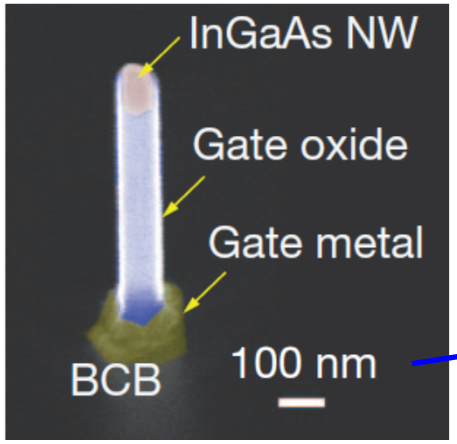
Zhao, IEDM 2013

Digital etch → S ↓, g_m ↑ → Better sidewall interface

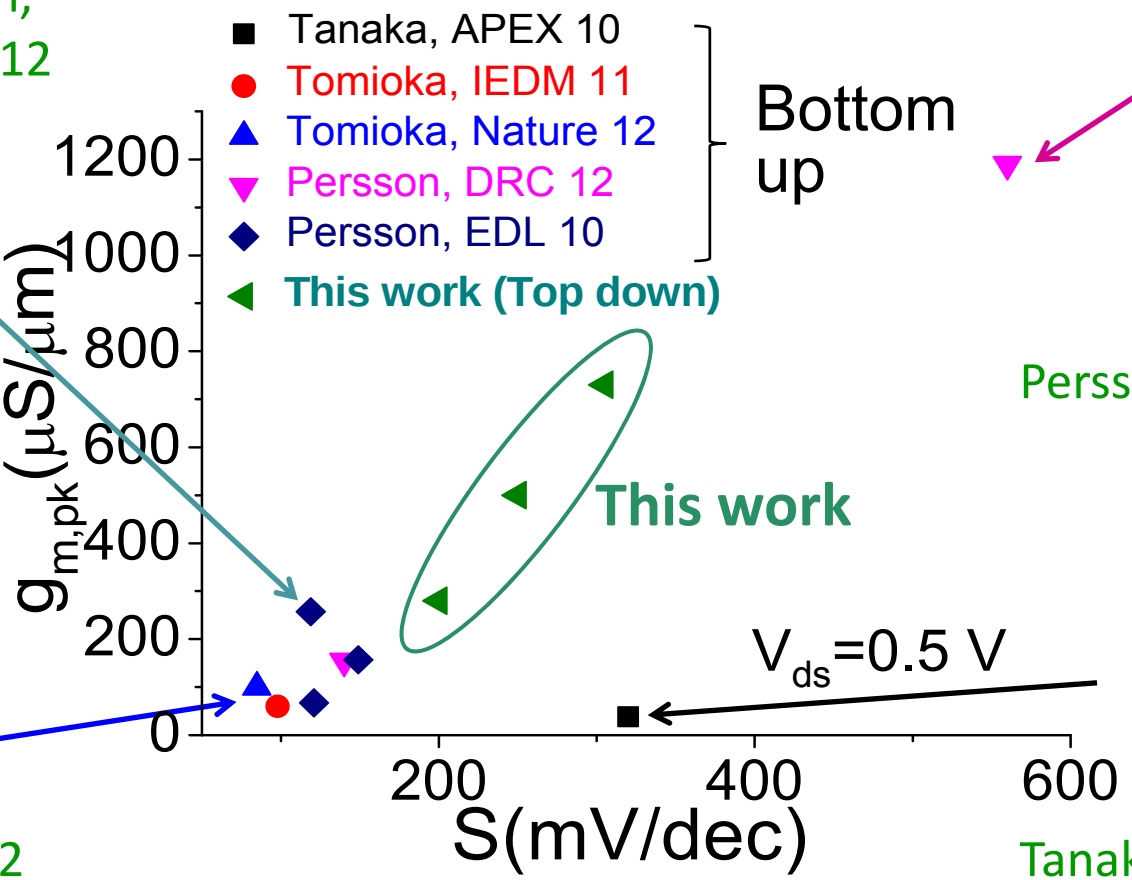
Benchmarking against bottom-up vertical InGaAs NW-MOSFETs

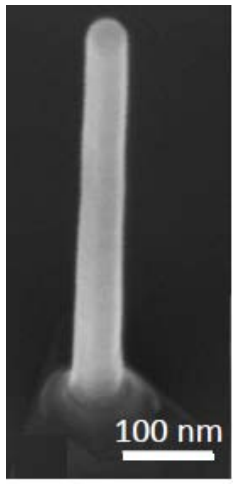


Persson, EDL 2012

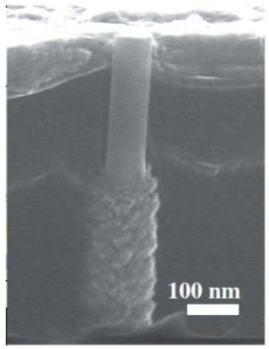


Tomioka, Nature 2012





Persson, DRC 2012

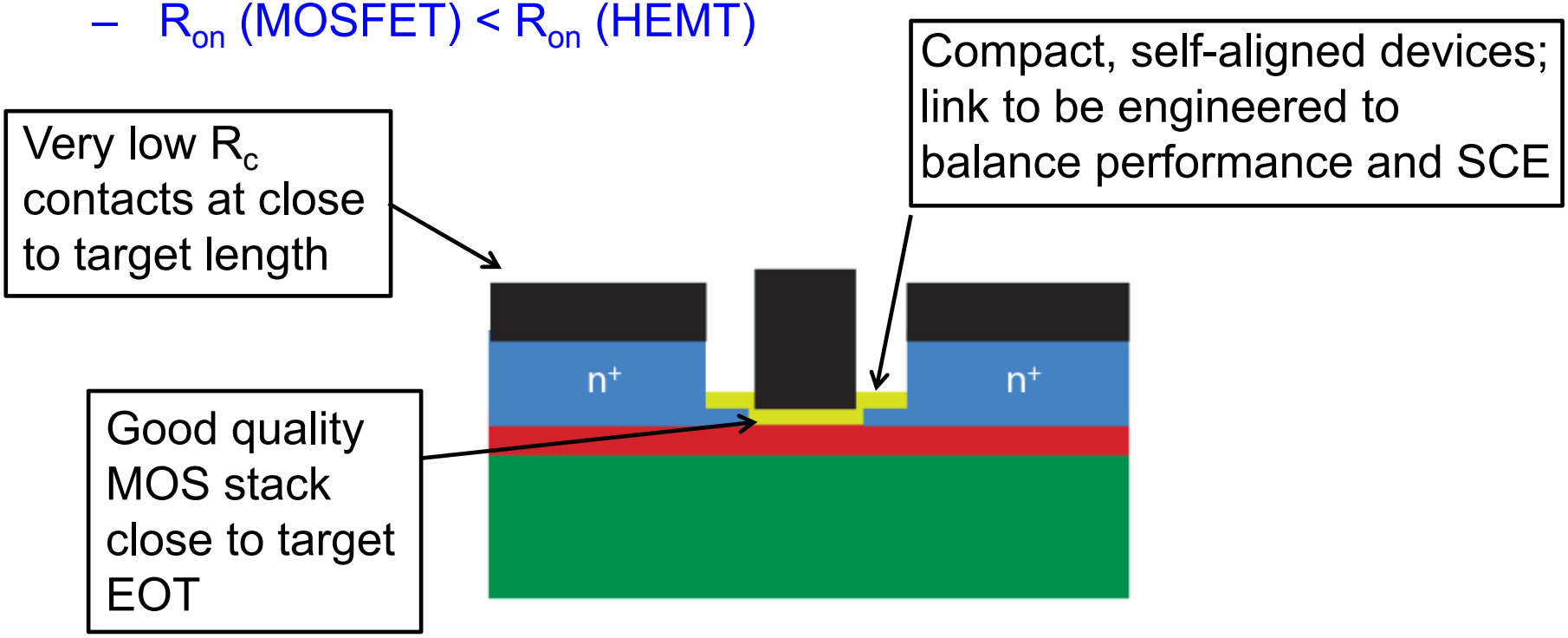


Tanaka, APEX 2010

- Fundamental trade-off between transport and short-channel effects
- Top-down NW-MOSFETs as good as bottom up devices

Conclusions

- Remarkable recent progress in InGaAs MOSFETs
  - g_m (MOSFET) = g_m (HEMT)
  - R_{on} (MOSFET) < R_{on} (HEMT)



- Many issues to investigate:
  - Tri-gate technology, integration with p-MOSFETs on Si, reliability