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Design and modeling of Faraday cages for substrate noise isolation ☆

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ABSTRACT

A Faraday cage structure using through-substrate vias is an effective strategy to suppress substrate crosstalk, particularly at high frequencies. Faraday cages can reduce substrate noise by 32 dB at 10 GHz, and 26 dB at 50 GHz. We have developed lumped-element, equivalent circuit models of the Faraday cages and test structures to better understand the performance of the Faraday cages. These models compare well to measured results and show that the vias of the Faraday cage act as an *RLC* shunt to ground that draws substrate current. Designing a Faraday cage to achieve optimum isolation requires low via impedance and mitigation of via sidewall capacitance. The Faraday cage inductance is correlated to the number of vias and via spacing of the cage and can be optimized for the frequency of operation.

1. Introduction

Suppression of substrate crosstalk is critical for System-on-Chip (SoC) applications that integrate sensitive analog and RF circuits. Substrate noise isolation requirements are already stringent [1] and future mm-wave systems will be even more difficult to isolate [2].

Traditional approaches to reduce substrate crosstalk include guard rings [3–5], silicon-on-insulator (SOI) substrates [4,6,7], high-resistivity substrates [8], junction-isolated wells [1,4]. These methods are attractive because they require little modification to existing technology. However, the drawback of using SOI or high-resistivity substrates is that they cease to work at high frequencies when the substrate becomes capacitive [7–9]. Guard rings cannot shunt noise that travels deep in the substrate [3–5].

Better crosstalk suppression has been obtained through unconventional techniques. Among these are porous silicon [10], metal [11] and air trenches [12], SOI on metal [13], and even chip-level [14] or total substrate transfer [15]. Though difficult to compare different isolation techniques due to different test structures, a key consideration when evaluating isolation schemes is the footprint of the isolation structure. van Zeijl et al. [5] uses a 300-μm wide p-type wall to shield the Bluetooth radio, and the trench is 60-μm wide in [11] and 100-μm in [10]. Also, non-standard substrates can affect device operation, such as the metal ground that lies under the buried oxide in [13].

We propose a Faraday cage exploiting the high-aspect ratio of through-substrate vias as a novel isolation scheme that combines exceptional crosstalk suppression into the mm-wave regime with a small footprint [16]. The Faraday cage consists of a ring of copper vias shorted to a copper backplane on the backside of the substrate and grounded through a ring of metal on the frontside. The vias are electrically isolated from the substrate with silicon nitride liner. In comparison to our earlier work [17,18], this paper presents Faraday cages fabricated with an improved process that yields better isolation at high frequencies [16]. We developed an equivalent circuit model that provides physical understanding of the isolation mechanism and enables the definition of design criteria for the Faraday cage for optimum substrate noise suppression.

2. Test structure design and measurement

The through-substrate via process to form the Faraday cage structures has been previously described by the authors in [16]. Important aspects of the improved fabrication process are a more conformal insulator liner using LPCVD silicon nitride, sidewall smoothing after DRIE, and an efficient copper electroplating process and CMP [16], which significantly reduced via resistance and

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provided electrical isolation of the vias from the substrate. The substrate was locally thinned by etching trenches into the backside by a deep reactive-ion etch (DRIE). This achieved high-aspect ratio vias with a small footprint without thinning the entire wafer for this test vehicle. The vias that form the Faraday cage are 10 μm in diameter and are lined with silicon nitride and filled with copper.

A designed set of test structures were fabricated to measure substrate noise with and without the Faraday cage (Fig. 2). The basic test structure is a two-port, RF, coplanar ground-signal-ground configuration. The signal pads, transmitter (tx) and receiver (rx), are each 50 μm × 100 μm. The top of the Faraday cage vias are connected to the aluminum ground pads, and at the bottom they are connected through a copper film lining the backside DRIE trench. This copper backplane is grounded through the vias and is isolated from other test structures and the wafer chuck. The backside DRIE trench dimensions extend to the edge of the front-side ground pads so that the entire structure lies within the DRIE trench (Fig. 1).

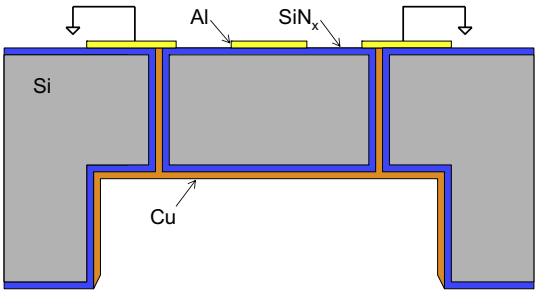

Fig. 1. Cross-section drawing of a Faraday cage test structure taken at line A–A′ in Fig. 2c.

We have designed two types of Faraday cages: *type I*, where a single Faraday cage is placed between the transmitter and receiver (Fig. 2a), and *type II*, where the transmitter and receiver pads each are surrounded by a Faraday cage (Fig. 2c). The separation, *v*, between the vias of the Faraday cage varies from 10 μm to 70 μm to examine the effect of via density. The distance, *d*, between transmitter and receiver varies from 50 μm to 400 μm. The reference structure pictured in Fig. 2b has aluminum pads and no Faraday cage, but still has the copper backplane. In this way we ensure that both structures are identical except for the Faraday cage vias. The test structure pictured in Fig. 2d was measured to quantify the effect of the metal line between transmitter and receiver without the cage.

We use $|S_{21}|$ as the figure-of-merit to evaluate substrate noise from transmitter to receiver. We measured S_{21} from 100 MHz to 50 GHz using an HP8510C network analyzer. A grounded metal screen between the probes reduced air crosstalk.

3. Measurement results and discussion

Fig. 3 plots $|S_{21}|$ against frequency for several Faraday cages of different via densities on p-type substrates. Measurements on n-type substrates show similar performance, confirming that wafer type is not a factor for substrate noise.

The type I Faraday cage (Fig. 3a) obtains exceptional isolation especially at high frequencies (31 dB at 10 GHz, average, compared to the reference) and into the mm-wave regime (21 dB at 50 GHz, average, compared to the reference). The values reported here are average values taken from several measurements, and may differ from values in Fig. 3, which are plots for an individual set of devices. At 10 GHz, this is comparable to the isolation of [17], but at 50 GHz the new Faraday cage performs better by 5 dB on average. This is due to the reduced resistance of the substrate vias.

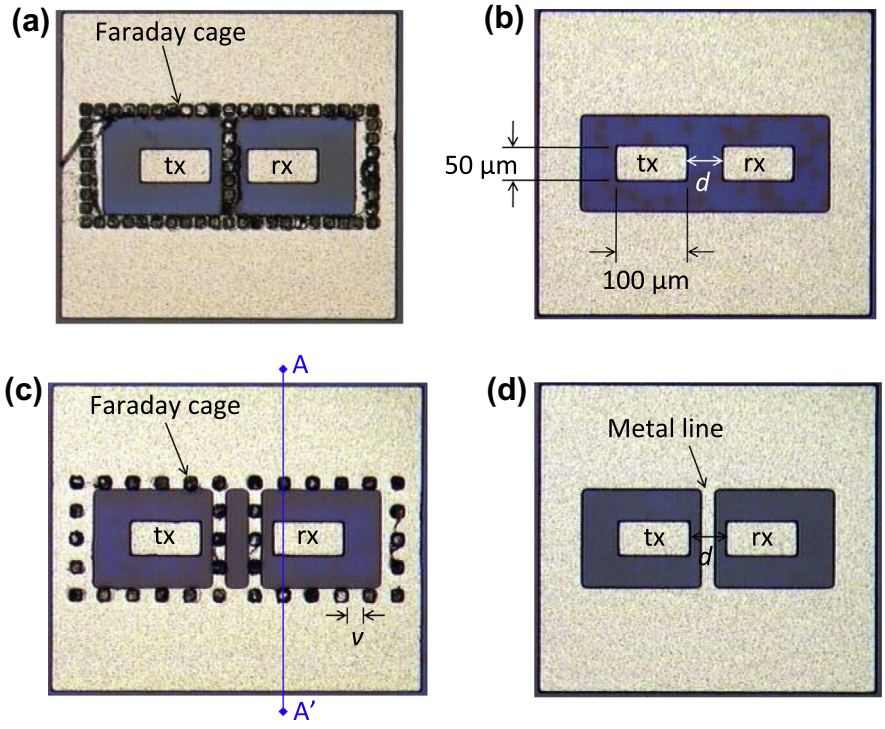

Fig. 2. Two-port, coplanar ground-signal-ground, RF test structures for measuring substrate noise. Vias are 10 μm in diameter. (a) Type I Faraday cage test structure at a 50-μm separation between transmitter and receiver, *d* via spacing, *v*, is 10 μm. (b) Reference test structure, *d* = 50 μm. (c) Type II Faraday cage test structure, *d* = 100 μm, *v* = 30 μm. (d) Test structure with a 20-μm wide metal line between transmitter and receiver, *d* = 50 μm.

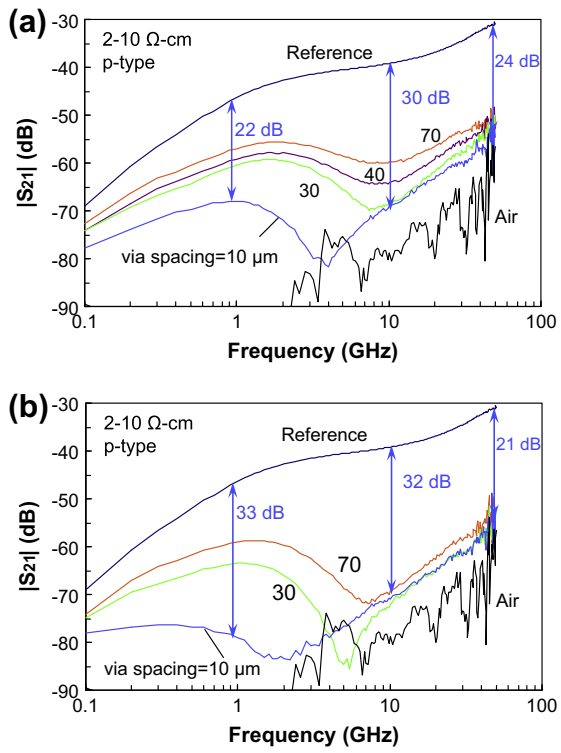

Fig. 3. $|S_{21}|$ measurements of reference and Faraday cage test structures for different via spacing of the (a) type I Faraday cage and (b) type II Faraday cage. d = 100 μm. Substrate resistivity is p-type, 2–10 Ω cm.

Using the type II Faraday cage configuration provides even better noise suppression because each transmitter and receiver pad is surrounded by its own Faraday cage (Fig. 3b). The noise suppression at 50 GHz is on average 32 dB better than the reference, and at 10 GHz is on average 26 dB better than the reference. Although the Faraday cages still perform well at low frequencies, compared to high frequencies the performance suffers. At 1 GHz, the type I Faraday cage is 15 dB better than the reference, and the type II cage is 22 dB better. The broad peak in substrate crosstalk at low frequencies was not observed in [17] and will be discussed in Section 5.

At low to mid-frequencies, decreasing via spacing (or increasing via density) improves Faraday cage isolation. However, at high frequencies, the impact of via density diminishes. This observation will be discussed in Section 4.3.

3.1. Reference measurement results

The reference measurements in Fig. 3 provides insight into substrate noise propagation. $|S_{21}|$ first rises with frequency, plateaus, and then rises again as the frequency increases. The first rise in $|S_{21}|$ is due to improved capacitive coupling between the pad and the substrate [9]. At some intermediate frequency, the substrate acts as a resistor, so $|S_{21}|$ is unaffected by frequency. At higher frequencies, the substrate capacitance becomes significant, and causes $|S_{21}|$ to rise again [9]. The transition to this high-frequency regime corresponds to the dielectric relaxation time constant of the substrate, τ_d, which is directly dependent on the dielectric constant and resistivity of the substrate [9]. The dielectric relaxation transition frequency for 1-Ω cm wafers is 152 GHz, and for 10 Ω cm, 15 GHz. High-resistivity substrates provide crosstalk isolation at frequencies when the substrate is resistive. However, at frequencies when the substrate becomes capacitive, the effect of resistivity disappears [9]. At these high frequencies, the reduction in substrate noise by the Faraday cage can prove most effective.

3.2. Transmission distance

For the Faraday cage test structure, increasing the transmission distance, d, reduces substrate crosstalk (Fig. 4). Because of the high resistivity of the substrate, it does not act as a single node. The reference test structure also shows this in Fig. 5.

To observe the effect of just a metal line, a test structure with a grounded, 20-μm wide Al strip between transmitter and receiver was fabricated (Fig. 2d). Its measurements are plotted in Fig. 5 along with the open reference (Fig. 2b). The metal line suppresses substrate noise by a few dB for distances of 50–200 μm, but its effect is negligible by 400 μm.

3.3. Faraday cage type

The two types of Faraday cages behave differently at increasing transmission distances. Fig. 6 plots both cage types at transmission distances of 100 and 400 μm. At 100 μm, the type II cage performs better because a double cage would suppress more noise than a single cage. However, at a farther distance of 400 μm, the type II cage is actually worse than type I. For the type I cage test structure at 400 μm, the Faraday cage is in the center of the structure with vias surrounding the entire substrate between the pads. The distance to the center line is farther than to vias to either side, so as the signal propagates through the substrate, it is attenuated by not only the substrate but also the grounded sideline vias. In contrast, the type II cage has Faraday cages closely surrounding both pads but no sideline vias in between the pads along the transmis-

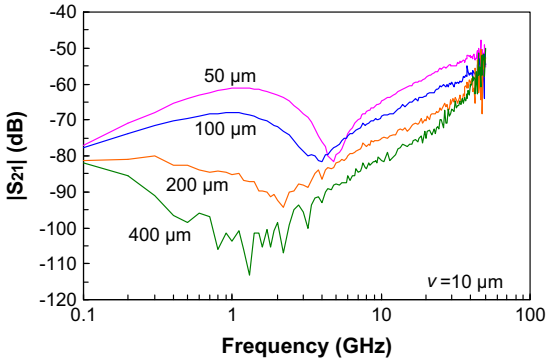

Fig. 4. $|S_{21}|$ vs. frequency of the type I Faraday cage for d between 50 and 400 μm, v = 10 μm. Substrate resistivity is 2–10 Ω cm.

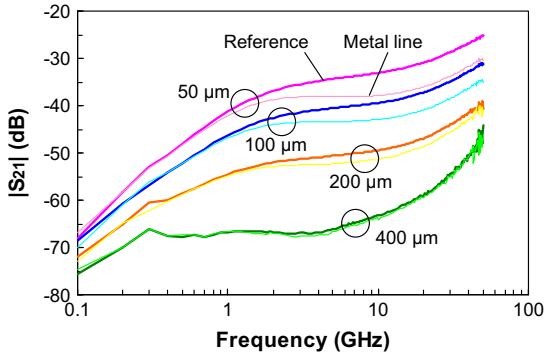

Fig. 5. $|S_{21}|$ vs. frequency of the reference test structure in Fig. 2b (thick lines) and test structure with a metal line in Fig. 2d (thin lines) for d between 50 and 400 μm. Substrate resistivity is 2–10 Ω cm.

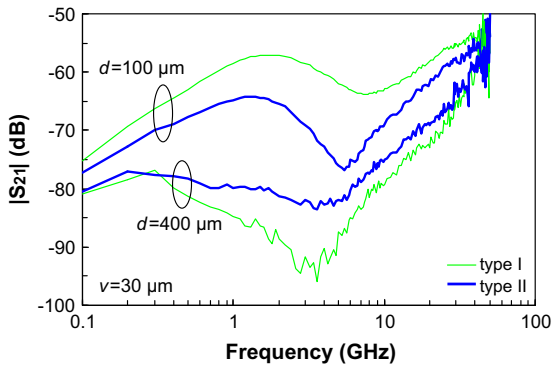

Fig. 6. $|S_{21}|$ vs. frequency of the both Faraday cage types at transmission distances of 100 and 400 μm, v = 30 μm. Substrate resistivity is 2–10 Ω cm.

sion distance. Therefore, once the signal passes through the first Faraday cage, the signal is only attenuated by the substrate.

4. Lumped-element, equivalent circuit model

4.1. Reference equivalent circuit model

The equivalent circuit model of the Faraday cage isolation structure is an extension of the reference test structure. As explained in Section 3.1, at frequencies below that corresponding to its dielectric relaxation time, the silicon substrate behaves as a resistor. But at higher frequencies, the substrate acts as a lossy dielectric. This demands a parallel resistor–capacitor combination [6,7]. A suitable model for the reference structure is therefore one that is similar to the SOI model in [7] and the high-resistivity substrate model in [6], depicted in Fig. 7. C_{pad} is the signal pad-to-substrate capacitance. R_1 and C_1 represent the substrate between the transmitter and receiver pads, and the central node is the substrate halfway between transmitter and receiver. R_2 and C_2 are lumped to represent the substrate beneath the signal pads to ground. C_g is the capacitance from the substrate to the surface ground pads. The copper backplane for the reference structure is floating since there is no connection to the backplane without substrate vias present.

4.2. Faraday cage equivalent circuit model

The Faraday cage model extends from the reference by adding the ground shunt provided by the vias (Fig. 8). From the central node, the *RLC* shunt to ground represents the vias of the Faraday cage. The via silicon nitride liner introduces the sidewall capacitance, C_f, to this shunt. C_f connects the silicon substrate to the metal via, represented by a resistor, R_f, and inductor, L_f, in series. C_g is eliminated in the Faraday cage model because the copper backplane is connected to ground through the vias so that C_g is essentially infinite.

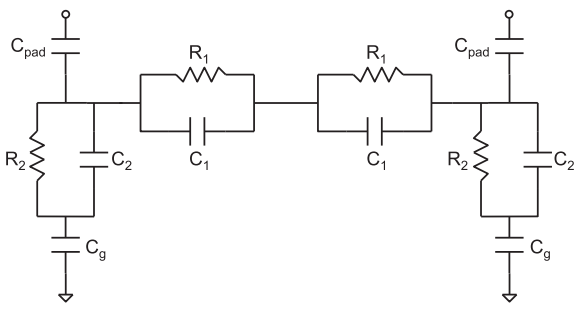

Fig. 7. Lumped-element, equivalent circuit for the reference test structure.

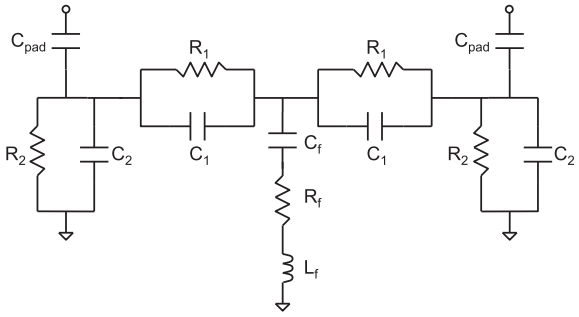

Fig. 8. Lumped-element, equivalent circuit for the Faraday cage test structure. The center *RLC* shunt to ground represents the vias of the Faraday cage.

4.3. Circuit simulations and via density

Equivalent circuit models were simulated using Agilent Advanced Design System software. Simulation and measurement data match well for different via spacings and were reported previously in [19] and are duplicated here in Fig. 9 and Table 1 for reference. The lumped-element values follow a logical succession as via spacing decreases from 70 to 10 μm. C_1 decreases and R_1 increases as the via spacing decreases because less substrate is present between the transmitter and receiver. C_2 decreases and R_2 increases also because less substrate is available to ground. C_{pad} remains constant because the pad size is identical for all test structures. For the Faraday cage circuit branch, R_f decreases with more vias in parallel (smaller via spacing). C_f increases because of greater via sidewall surface area by adding more vias in parallel. However, L_f shows a minimum between the 30 and 40-μm via spacing. As via density increases, more vias are put in parallel so that the self-inductance decreases, but placing vias in close proximity increases the mutual inductance. For very dense cages (10-μm spacing), the Faraday cage inductance increases substantially due to rising mutual inductance. As seen in the via-array measurements in [19], the overall inductance actually increases with greater number of vias in parallel. Therefore, using a denser cage is better only up to a point, the crossover being via spacings between 10 and 40 μm.

4.4. Circuit simulations and transmission distance

Circuit simulations of type I Faraday cages with varying transmission distance show excellent agreement with measurement data (Fig. 10). Corresponding component values are listed in Table 2. Increasing the transmission distance increases the amount of silicon

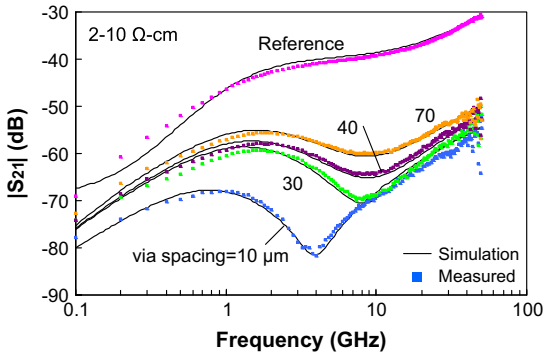

Fig. 9. $|S_{21}|$ vs. frequency of measurements and simulations of the lumped-element models in Figs. 7 and 8 for type I Faraday cages with different via spacing and the reference. d = 100 μm.

Table 1
Lumped-element values obtained from simulations of the type I Faraday cage and reference shown in Fig. 9.

	Reference	v = 10 μm	30 μm	40 μm	70 μm
C_1	2.5 fF	1 fF	1 fF	3 fF	3 fF
R_1	3.5 kΩ	1.2 kΩ	750 Ω	700 Ω	650 Ω
C_2	20 fF	50 fF	50 fF	50 fF	60 fF
R_2	500 Ω	900 Ω	500 Ω	450 Ω	400 Ω
R_f	–	2 Ω	3 Ω	5 Ω	8 Ω
L_f	–	165 pH	75 pH	70 pH	90 pH
C_f	–	10 pF	5 pF	4.5 pF	3.5 pF
C_{pad}	0.3 pF	0.3 pF	0.3 pF	0.3 pF	0.3 pF
C_g	1.5 pF	–	–	–	–

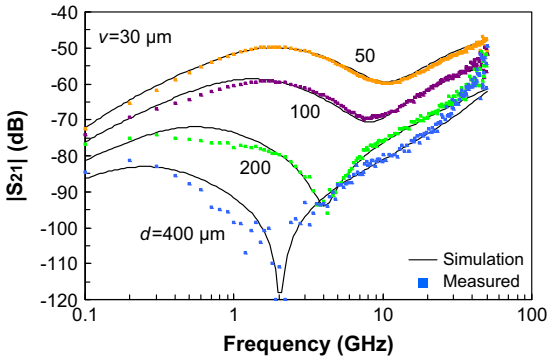

Fig. 10. $|S_{21}|$ vs. frequency of measurements and simulations of the circuit model in Fig. 8 for type I Faraday cages with increasing transmission distance.

Table 2
Lumped-element values obtained from simulations of the Faraday cage and reference shown in Fig. 10.

	d = 50 μm	100 μm	200 μm	400 μm
C_1	1 fF	1 fF	1 fF	1 fF
R_1	400 Ω	750 Ω	1.8 kΩ	3.8 kΩ
C_2	50 fF	50 fF	50 fF	50 fF
R_2	400 Ω	500 Ω	1.2 kΩ	3.2 kΩ
R_f	3.5 Ω	3 Ω	1 Ω	0.2 Ω
L_f	55 pH	75 pH	140 pH	290 pH
C_f	4 pF	5 pF	12 pF	21 pF
C_{pad}	0.3 pF	0.3 pF	0.3 pF	0.3 pF

between the two pads and decreases substrate noise. This translates to an increase in substrate resistance and a decrease in capacitance. To match simulation to measurement, we increased R_1, which represents the increase in silicon between the transmitter and receiver, and R_2, which represents the increase in silicon from the transmitter or receiver pad to ground because the distance to the grounded cage vias has increased on one side of the cage. Decreasing C_1 and C_2 had little effect, so these remained unchanged. Also, as d increases, the type I Faraday cage extends so that more vias are included in the cage. The increase in number of vias changes the *RLC* shunt so that although L_f is larger, R_f decreases and C_f increases, reducing $|S_{21}|$.

5. Discussion

To explore the physics of the Faraday cage, we varied several key parameters in the equivalent circuit model. This investigation was previously explored in [19] and is expanded here. The effect of the Faraday cage is to shunt the central node to ground through the substrate vias. Lower via resistance of the Faraday cage, R_f, is advantageous as seen in Fig. 11. L_f and C_f are more complicated. C_f dominates at low frequencies, while L_f dominates at high

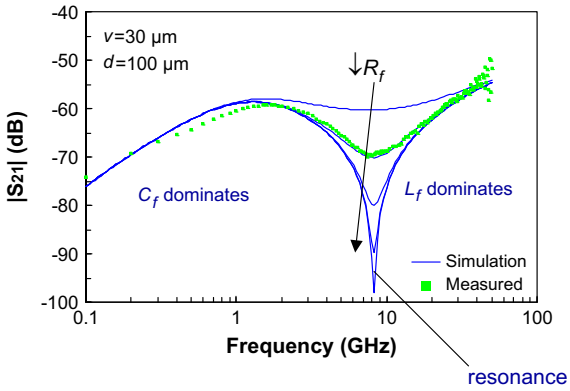

Fig. 11. $|S_{21}|$ vs. frequency of Faraday cage simulations varying R_f (0.1–10 Ω). $|S_{21}|$ drops with smaller values of R_f. d = 100 μm and v = 30 μm.

frequencies. The minimum in $|S_{21}|$ seen at mid-frequency is the resonance between L_f and C_f when the series combination shorts out, and the impedance of the via is determined by R_f. To verify this, we varied values of C_f and L_f separately. Fig. 12 shows simulations where C_f was varied from 1 to 11 pF with all other elements held constant to values in Table 1 for v = 30 μm. As C_f increases with a denser cage, the vias gain a better grasp on the substrate so that more substrate current can be shunted to ground, and $|S_{21}|$ drops. At the limit as C_f goes to infinity, the peak at low frequencies disappears, the low-frequency behavior is dominated by R_f, and the substrate noise is minimized (Fig. 12). In Fig. 13, L_f was varied from 50 to 150 pH, and at high frequencies when L_f dominates, decreasing L_f reduces $|S_{21}|$.

The broad peak in $|S_{21}|$ of the Faraday cage at low frequencies was not present in previous work [18]. Its equivalent circuit model lacks the sidewall capacitance, C_f, in the center shunt because of a defective nitride liner. Comparing the circuit simulations of current and previous work [18] confirms that the peak at low frequencies is due to C_f.

For vias to be effective in suppressing crosstalk, the frequency has to be high enough for C_f to short out. With more vias, this occurs at lower frequencies (Fig. 9). Fig. 12 shows the simulation result for a Faraday cage without C_f and all other elements held at their original values in Table 1. This shows that $|S_{21}|$ at low frequency is minimized by eliminating C_f. C_f can be completely eliminated by using a metal liner instead of an insulator. Simulations of the Faraday cage circuit model without C_f are plotted in Fig. 14 with varying values of R_f and L_f. Without C_f, R_f determines the low-frequency behavior, L_f dominates the high-frequency

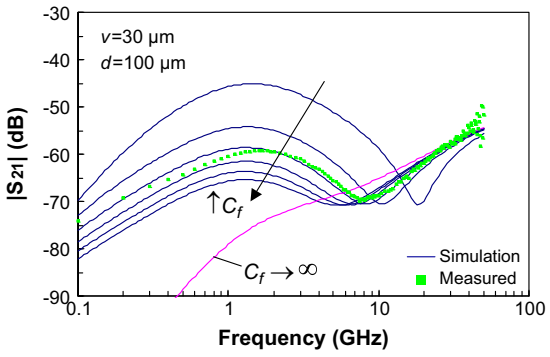

Fig. 12. $|S_{21}|$ vs. frequency of Faraday cage simulations varying C_f (1–11 pF). $|S_{21}|$ drops with higher values of C_f at low to mid-frequencies. $|S_{21}|$ is minimized at the limit when C_f goes to infinity (C_f is eliminated).

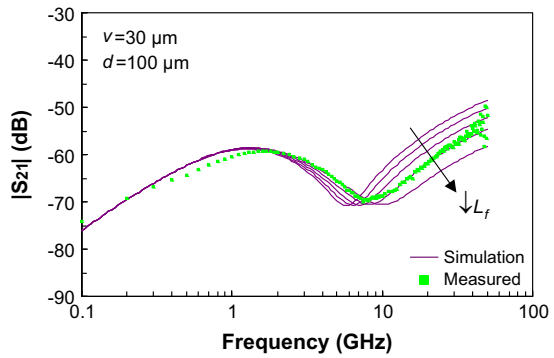

Fig. 13. $|S_{21}|$ vs. frequency of Faraday cage simulations varying L_f (50–150 pH). $|S_{21}|$ drops with lower values of L_f at high frequencies.

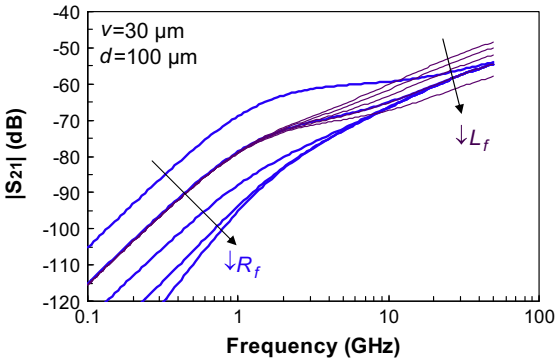

Fig. 14. $|S_{21}|$ simulations of the Faraday cage model without C_f. R_f varied from 0.1 to 10 Ω (thick blue lines). R_f dominates the low-frequency behavior, so smaller values of R_f reduce $|S_{21}|$.L_f varied from 50 to 150 pH (thin purple lines). L_f dominates the high-frequency behavior, so smaller values of L_f reduce $|S_{21}|$. (For interpretation of the references to color in this figure legend, the reader is referred to the web version of this article.)

behavior, and the *LC* resonance disappears. Therefore, the smaller the R_f and L_f branch is, the more effective the ground shunting of the substrate between the transmitter and receiver, resulting in a reduction in crosstalk.

6. Faraday cage design guidelines

Faraday cage measurements and simulations can be summarized into design guidelines to reduce substrate noise. Increasing the transmission distance reduces crosstalk but wastes area. The type II Faraday cage performs better at short distances and so is recommended over type I. Reducing the resistance of the Faraday cage, R_f, will reduce substrate noise. Eliminating via sidewall capacitance by using a metal liner instead of a dielectric will reduce low-frequency noise and eliminate the *LC* resonance. Reducing the Faraday cage inductance, L_f, will reduce noise at high frequencies. The via density of the Faraday cage determines L_f, which has two competing mechanisms, self and mutual inductance. For our technology, the minimum inductance lies between via spacings of 10 and 40 μm.

7. Conclusion

A Faraday cage of through-substrate vias effectively suppresses substrate noise into the mm-wave regime. Equivalent circuit models of the Faraday cage accurately capture the behavior of substrate noise isolation. These models have been used to develop design criteria that optimizes Faraday cage structures at the desired frequency of operation.

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