High-Speed E-Mode InAs QW MOSFETs With Al_2O_3 Insulator for Future RF Applications

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***Abstract*—We demonstrate $L_g = 100$ nm high-speed enhancement-mode (E-mode) InAs quantum-well MOSFETs with outstanding high-frequency and logic performance. These devices feature a 3-nm Al_2O_3 layer grown by atomic layer deposition. The MOSFETs with $L_g = 100$ nm exhibit $V_T = 0.2$ V (E-mode), $R_{ON} = 370\ \Omega \cdot \mu m$, $S = 105$ mV/dec, DIBL = 100 mV/V, and $g_{m_max} = 1720\ \mu S/\mu m$ at $V_{DS} = 0.5$ V. They also have an excellent high-frequency response of $f_T = 248$ GHz and $f_{max} = 302$ GHz at $V_{DS} = 0.5$ V, the highest f_T and f_{max} in III–V MOSFETs ever reported.**

***Index Terms*—Cutoff frequency (f_T), drain-induced barrier lowering (DIBL), InAs, logic, MOSFET, ON resistance (R_{ON}), subthreshold swing (S).**

I. Introduction

As THE heterogeneous integration of novel technologies, including compound semiconductors, MEMS, and photonic devices, has matured on a large-diameter silicon platform, the single-chip integration of RF, communication, and logic blocks on a system-on-chip (SOC) platform has become increasingly appealing [1], [2]. Historically, III–V-based high-electron-mobility transistors (HEMTs) have offered a record high-frequency performance, as assessed by current-gain cutoff frequency (f_T), maximum oscillation frequency (f_{max}), and minimum noise figure (NF_{min}), due to the superior carrier transport properties of III–V channel materials. To date, $In_{0.7}Ga_{0.3}As$ HEMTs on GaAs substrates have exhibited the best balanced high-frequency response (high f_T and high f_{max}) of any transistor technology [3].

Recently, these materials have started showing great promise for new ultralow-power and high-density III–V CMOS logic technologies [4]. In the last few years, the quality of high-k dielectric/channel interfaces in III–V MOSFETs formed by atomic layer deposition (ALD) has been dramatically improved [5]–[9], making this technology promising for future scaled III–V CMOS devices. The best III–V MOSFET features $R_{ON} = 440\ \Omega \cdot \mu m$, $g_{m_max} = 1750\ \mu S/\mu m$, $S = 100$ mV/dec, and DIBL = 130 mV/V at $V_{DS} = 0.5$ V [5].

A critical problem with III–V HEMTs that has received little attention is harmonious scaling, in which all the physical dimensions and electrical device parameters scale proportionally with the channel length. However, there are two fundamental bottlenecks for the absence of any significant scaling of III–V HEMTs in the last ten years: gate leakage current and barrier tunneling resistance ($R_{Barrier}$) [10]. Without scaling the barrier thickness and R_S, gate length scaling in III–V HEMTs results in diminished performance, particularly transconductance (g_m). This increases the extrinsic and parasitic delay contributions to the total delay which hurts the overall high-frequency response [3]. Now, the ultimate pathway to overcome both limitations is the high-k-dielectric-based III–V MOSFET architecture [4], which not only allows the aggressive EOT scaling but also minimizes $R_{Barrier}$ significantly. Moreover, these are attractive to achieving enhancement-mode (E-mode) devices, where III–V HEMTs with E-mode suffer from excessive gate leakage current, limiting their applications.

In this letter, we report on $L_g = 100$ nm InAs quantum-well (QW) MOSFETs with an Al_2O_3 insulator. We show how III–V MOSFET architecture overcomes the aforementioned challenges, yielding a well-balanced high-frequency response and excellent logic performance in scaled InAs MOSFETs.

II. Process Technology

A cross section of our device structure is shown in Fig. 1. From top to bottom, the epitaxial layer consists of a heavily doped 10-nm $In_{0.53}Ga_{0.47}As$ cap, a 2-nm InP etch stopper, a 10-nm $In_{0.53}Ga_{0.47}As/InAs/In_{0.53}Ga_{0.47}As$ channel, a 5-nm $In_{0.52}Al_{0.48}As$ spacer, inverted Si δ doping, and a 300-nm $In_{0.52}Al_{0.48}As$ back barrier or buffer on an InP substrate. From the Hall calibration wafer, the electron mobility ($\mu_{n,Hall}$) was 8000 $cm^2/V \cdot s$ with $n_s = 1 \times 10^{12}/cm^2$ at room temperature.

Devices were fabricated much like previously reported InGaAs MOSFETs [9], with thinner cap thickness to tightly control the side recess spacing on both edges of the gate. Fabrication began with mesa isolation and source/drain ohmic contact with nonalloyed Mo/Ti/Mo/Au ohmic metal stack and 1-μm spacing ($L_{GS} = L_{GD} = 0.5\ \mu m$). After growing 20 nm of SiO_2 by PECVD, a fine gate pattern with single-layer ZEP-520A was defined by e-beam lithography and transferred to the

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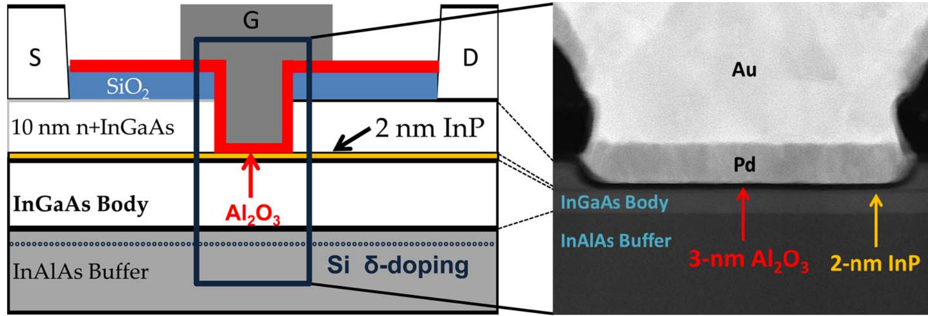

Fig. 1. (Left) Device schematic and (right) TEM image for the cross section of 100-nm InAs MOSFETs with $Al_2O_3 = 3$ nm.

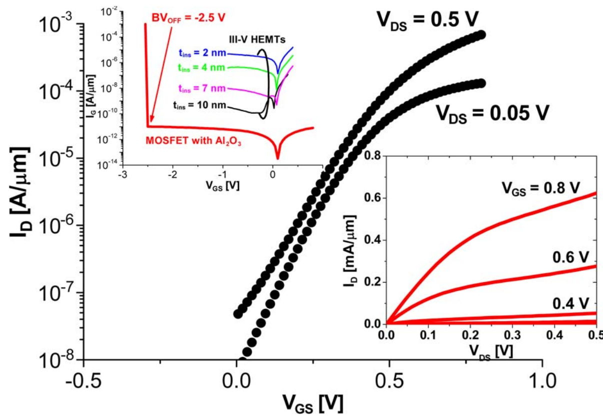

Fig. 2. DC subthreshold characteristics of $L_g = 100$ nm InAs MOSFETs. Inset on the right shows I_G against $V_{\rm GS}$ for InAs MOSFET with Al_2O_3 and III–V HEMTs with various values of $t_{\rm ins}$. Inset on the left shows output characteristics.

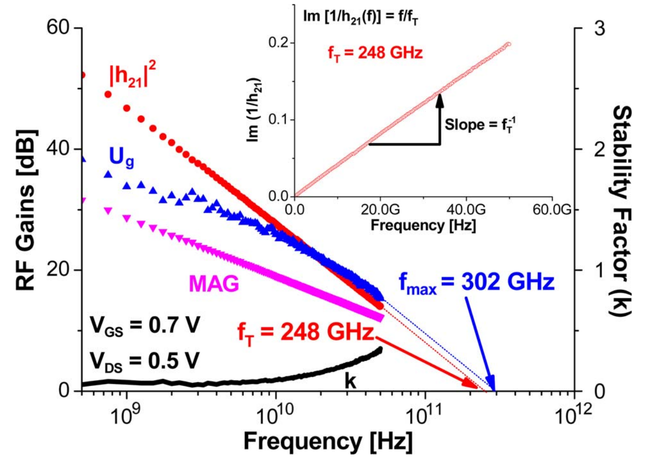

Fig. 3. $|h_{21}|^2$, Mason's unilateral gain U_g, and MAG, against frequency for $L_g = 100$ nm InAs MOSFETs at $V_{\rm GS} = 0.7$ V and $V_{\rm DS} = 0.5$ V. Inset shows f_T extraction by Gummel's approach [11].

SiO_2 layer using plasma etching. Subsequently, a gate recess process was carried out, using a diluted mixture of citric acid, H_2O_2, and H_2O. Immediately after removing the e-beam resist using solvents (NMP, acetone, IPA, and ethanol), 3 nm of ALD Al_2O_3 was grown on top of the 2-nm InP layer. Finally, a Pd/Au gate metal was formed. Fig. 1 shows a TEM image for the cross section of an $L_g = 100$ nm device with $Al_2O_3 = 3$ nm. The TEM image clearly reveals tight control of the side recess spacing $(L_{\rm side})$ on each edge of the gate.

III. Result and Discussion

The subthreshold characteristics of a representative $L_g = 100$ nm InAs QW MOSFET are shown in Fig. 2. Defining threshold voltage (V_T) as the value of $V_{\rm GS}$ that yields $I_D = 1\ \mu$A$/\mu$m, the device exhibits E-mode operation with $V_T = 0.2$ V at $V_{\rm DS} = 0.5$ V. More importantly, the device demonstrates excellent short-channel controls as manifested by a subthreshold swing (S) of 105 mV/dec and drain-induced barrier lowering (DIBL) of 100 mV/V at $V_{\rm DS} = 0.5$ V. As shown in the inset of Fig. 2, the gate leakage current (I_G) is less than 1 nA$/\mu$m at all the measured bias conditions. This is at least 10^5 times lower than that in III–V HEMTs at forward-gate bias regime. OFF-state breakdown voltage $(\mathrm{BV}_{\rm OFF})$ is -2.5 V. The device also displays excellent pinchoff characteristics up to $V_{\rm DS} = 0.6$ V and a low ON resistance $(R_{\rm ON})$ of $370\ \Omega \cdot \mu$m at $V_{\rm GS} = 0.8$ V. This outstanding $R_{\rm ON}$ contributes to the maximum transconductance $(g_{m,\max}) = 1720\ \mu$S$/\mu$m at $V_{\rm DS} = 0.5$ V.

Microwave performance was characterized with an off-wafer line–reflection–reflection–match calibration from 0.5 to 50 GHz. On-wafer open and short structures were used to subtract pad capacitances and inductances from the measured device S-parameters. Fig. 3 plots h_{21}, maximum available gain (MAG), and Mason's unilateral gain (U_g) against frequencies for the $L_g = 100$ nm device with $W_G = 2\ \times 20\ \mu$m at $V_{\rm GS} = 0.7$ V and $V_{\rm DS} = 0.5$ V. In this particular measurement, $f_T = 248$ GHz and $f_{\max} = 302$ GHz were obtained by extrapolating $|h_{21}|^2$ and U_g with a slope of -20 dB/dec using a least squares fit. The value of f_T in our device was also verified by Gummel's approach (inset) [11], yielding $f_T = 248$ GHz. To the knowledge of the authors, these are the best combination of f_T and $f_{\max}$ at $V_{\rm DS} = 0.5$ V, ever reported in any III–V MOSFET technology, and approach to advanced III–V HEMTs with similar gate lengths. Furthermore, the short-circuit current gain $(|h_{21}|^2)$ in low-frequency regime displays about -20-dB/dec slope even with $V_{\rm GS} = 0.7$ V. This is another manifestation of the benefit of using Al_2O_3 dielectric as a gate insulator, since it dramatically reduces I_G, as opposed to conventional HEMTs with a Schottky gate, making it of great interest to RF applications.

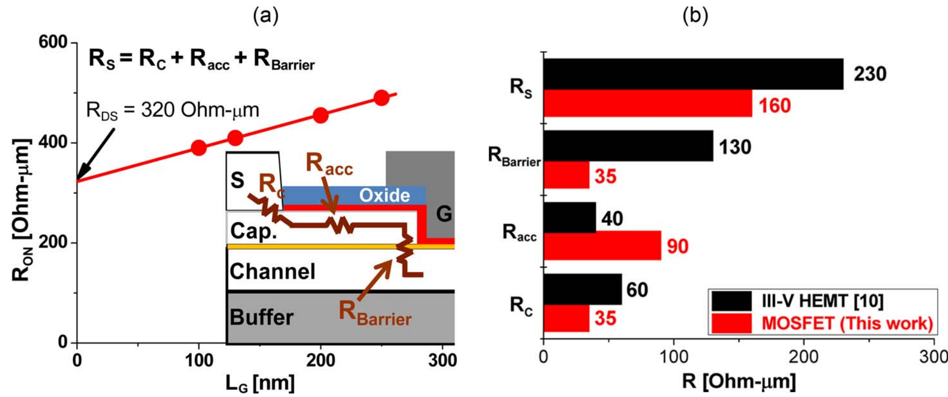

Fig. 4. (a) R_{ON} as a function of L_g for our InAs MOSFETs and (inset) simple model for R_s and (b) extracted components for R_s which arise from TLM and R_{ON} analysis.

Plotting the R_{ON} values from a number of identical devices with different gate lengths allows us to evaluate the source resistance (R_S). Fig. 4(a) shows the extracted R_{ON} as a function of L_g. In principle, R_{ON} consists of R_{DS} (sum of R_S and R_D) and R_{ch} (channel resistance under the gate), where R_{ch} is proportional to L_g. As a result, R_{DS} can be extracted from the Y-intercept. This process yields a value of $R_{\mathrm{DS}} = 320\ \Omega \cdot \mu$m in our family of devices. To understand and decompose the constituent components of R_S, we have used a simple model in [10], as shown in the inset of Fig. 4(a). Here, R_c is the contact resistivity between the nonalloyed ohmic metal and heavily doped InGaAs cap, R_{acc} is the access resistivity between the ohmic metal and gate, and R_{Barrier} is the resistivity through the 2-nm InP etch stopper between the cap and channel. Values of $R_c = 35\ \Omega \cdot \mu$m and $R_{\mathrm{acc}} = 90\ \Omega \cdot \mu$m were obtained from the separate TLM measurements, and therefore, R_{Barrier} was estimated to be around 35 $\Omega \cdot \mu$m. Finally, each component of R_s in our InAs MOSFETs was compared to that in III–V HEMTs [10], as shown in Fig. 4(b). As would be expected from the InAs MOSFET architecture, R_{Barrier} is negligible in comparison to that in III–V HEMTs [10]. From this analysis, we find that R_{acc} is the dominant component of R_s in our InAs MOSFETs, accounting for 56% of the total value. Further optimization in the form of a self-aligned design should lead to significant reductions in R_s.

IV. CONCLUSION

We have demonstrated E-mode $L_g = 100$ nm InAs QW MOSFETs with an Al_2O_3 insulator. These devices exhibit excellent logic characteristics at $V_{\mathrm{DS}} = 0.5$ V, such as $V_T = 0.2$ V, DIBL $= 100$ mV/, $S = 105$ mV/dec, $R_{\mathrm{ON}} = 370\ \Omega \cdot \mu$m, and $g_{m_\max} = 1720\ \mu$S/μm. These devices also feature a well-balanced high-frequency response ($f_T = 248$ GHz and $f_{\max} = 302$ GHz). This outstanding performance arises from aggressive EOT scaling using Al_2O_3 insulator. Our work demonstrates that, with further device optimization in the form of self-aligned ohmic contacts, the InAs MOSFET architecture will be a strong contender for next-generation RF and SOC applications.

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