Vertical Nanowire InGaAs MOSFETs Fabricated by a Top-down Approach

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Fabrication: MTL, SEBL at MIT

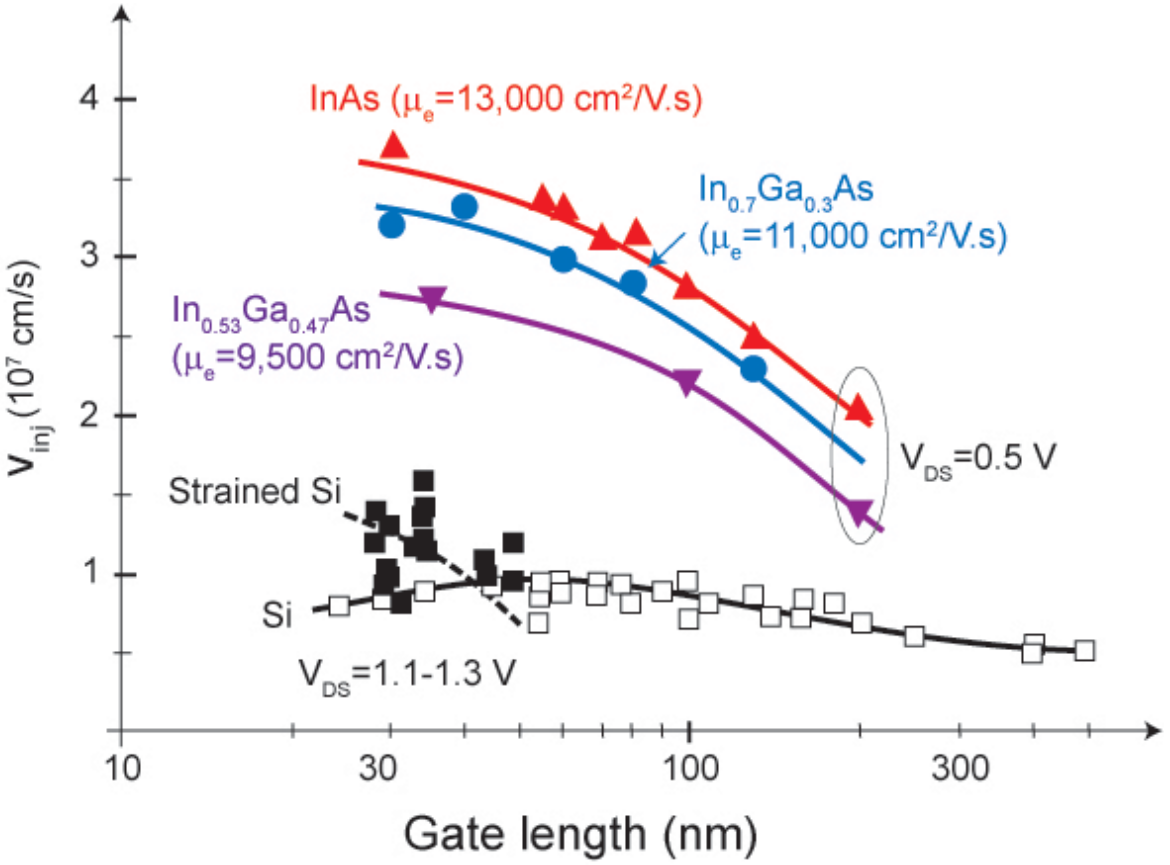
Outline

- Motivation
- Device technology
- Device electrical characteristics
- Conclusions

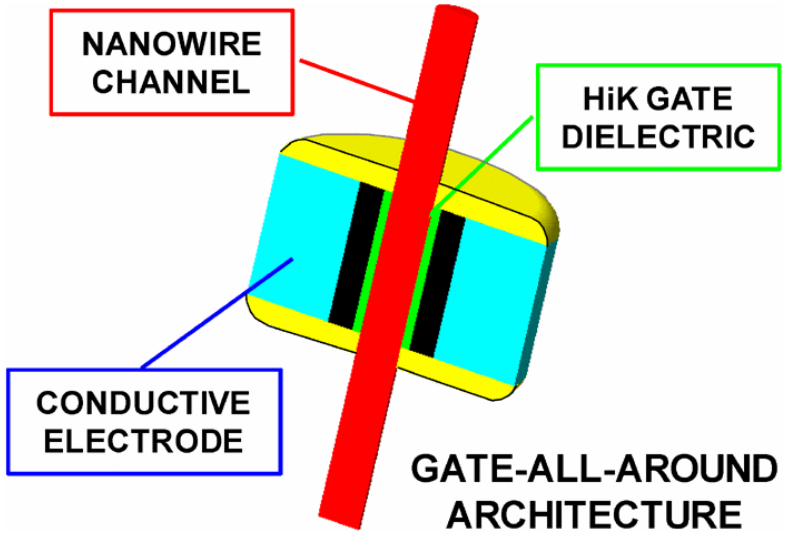
Motivation

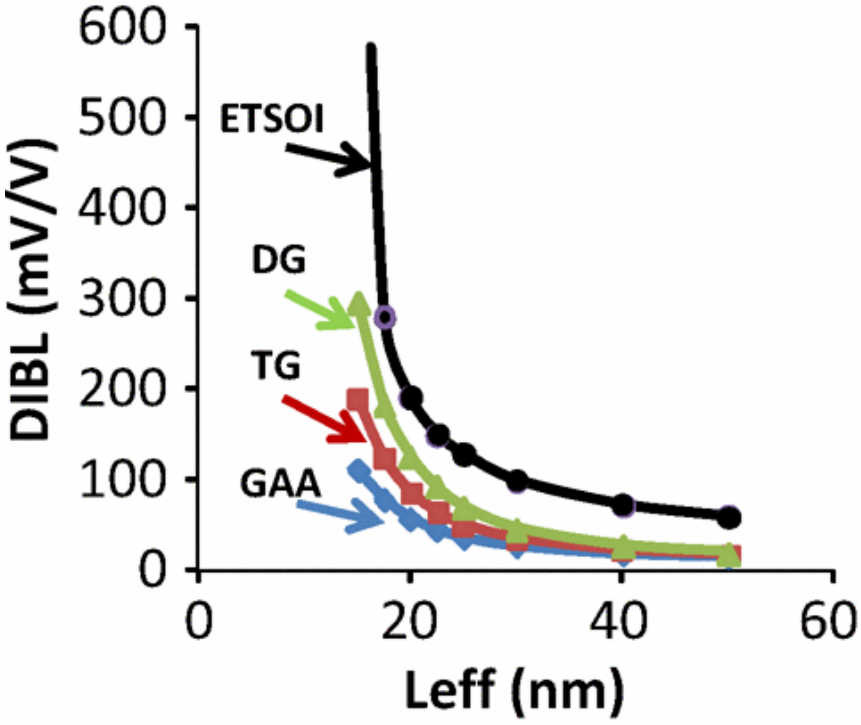
Superior electron transport properties of InGaAs material system – high mobility and electron velocity

del Alamo, Nature 2011



Gate-all-around (GAA) nanowire MOSFETs



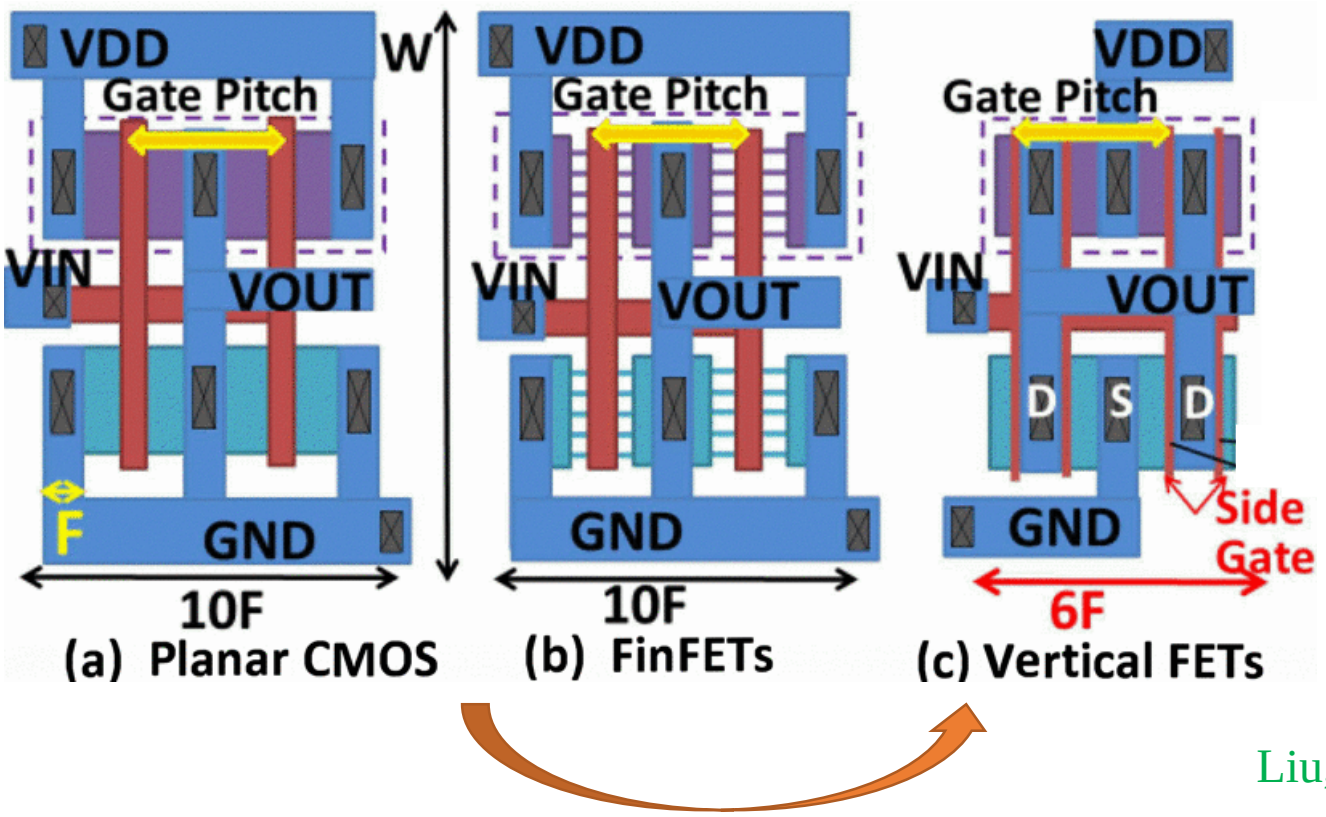


Kuhn, TED 2012

- Nanowire MOSFET provides ultimate scalability

Vertical channel MOSFETs

Vertical nanowire decouples footprint scaling and gate length scaling → high density



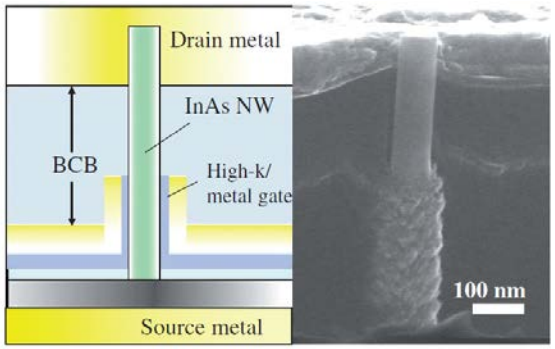
Liu, DRC 2012

- Use of vertical FETs saves 40% of total chip area

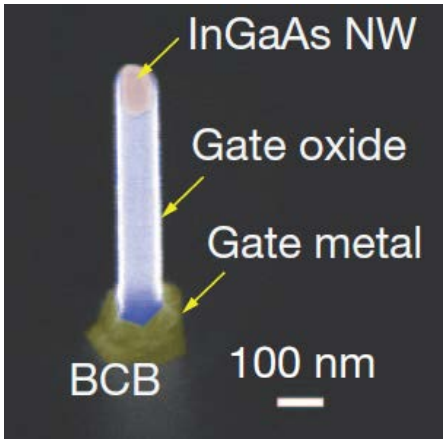
Bottom-up approach

Impressive devices via bottom-up techniques demonstrated

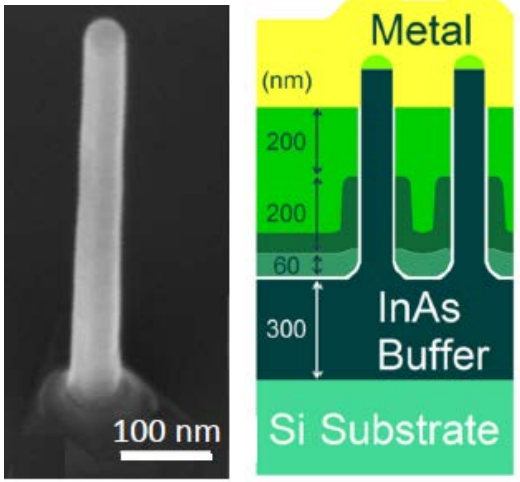
- Complicated epitaxial growth or Au seed particles required



Tanaka, APEX 2010



Tomioka, Nature 2012



Persson, DRC 2012

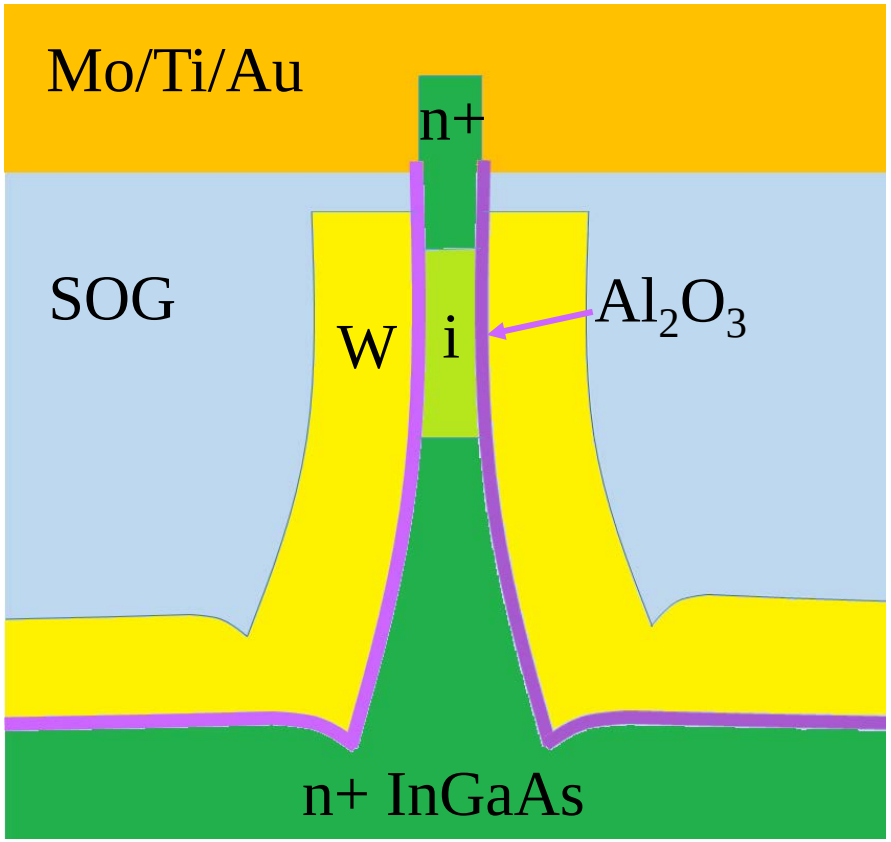
- Top-down approach worth investigating!

Goal: vertical nanowire InGaAs MOSFETs fabricated via top-down approach

Starting heterostructure:

n+ InGaAs, 70 nm
i InGaAs, 80 nm
n+ InGaAs, 300 nm

n+: 6×10^{19} Si doping

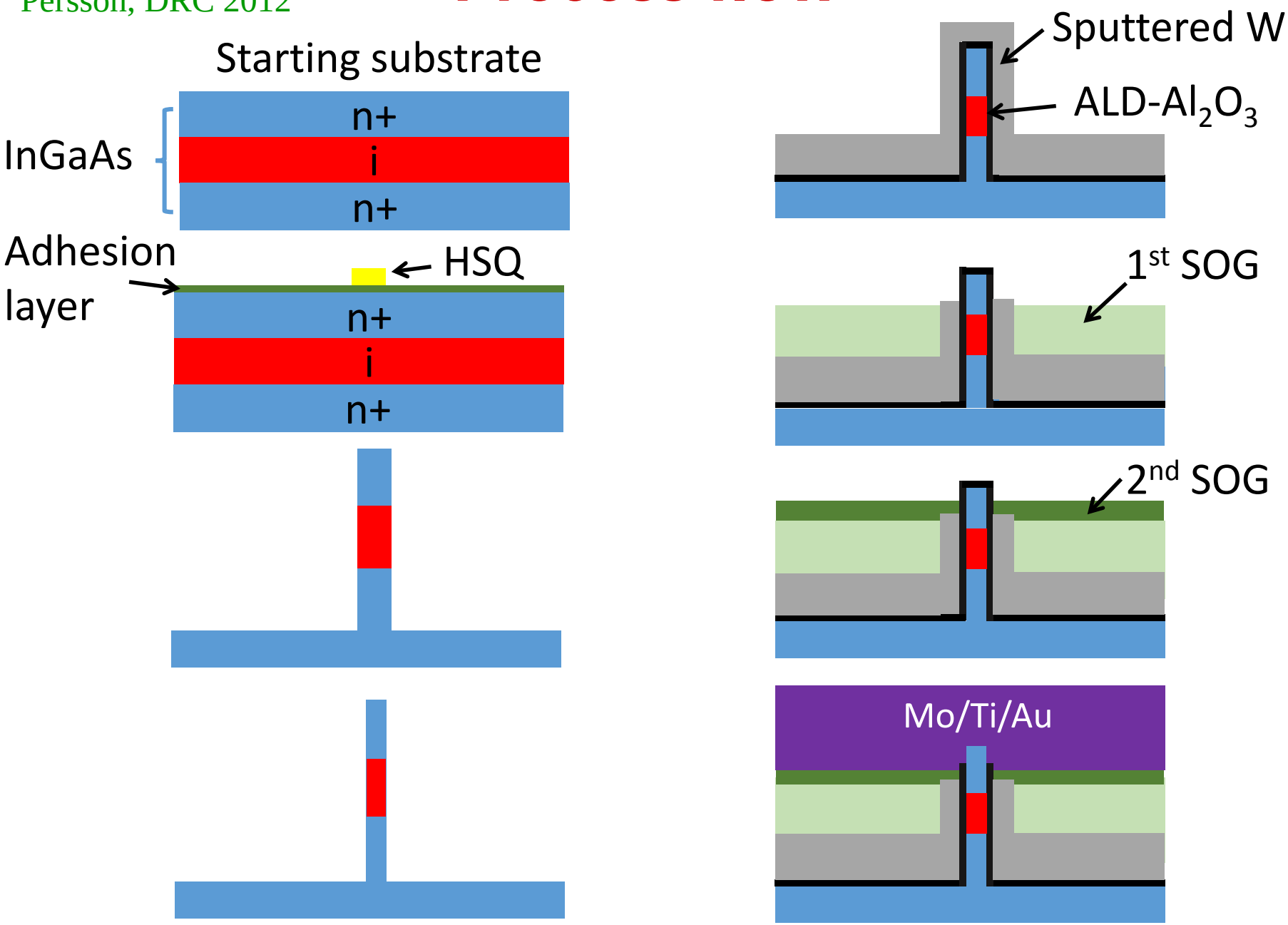


Key elements:

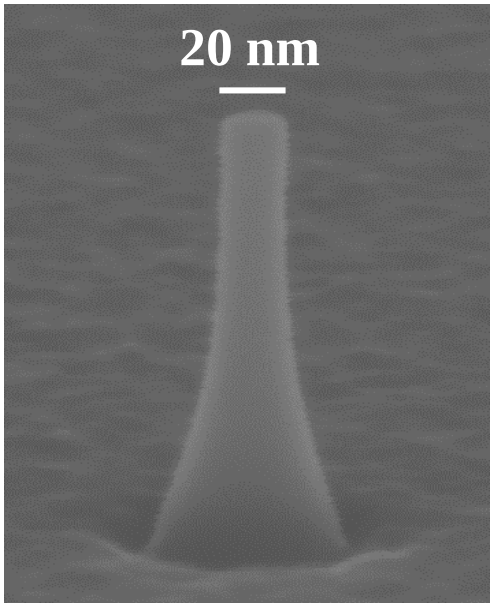
- Top-down approach based on RIE
- Single nanowire MOSFETs

Tomioka, Nature 2012
Persson, DRC 2012

Process flow

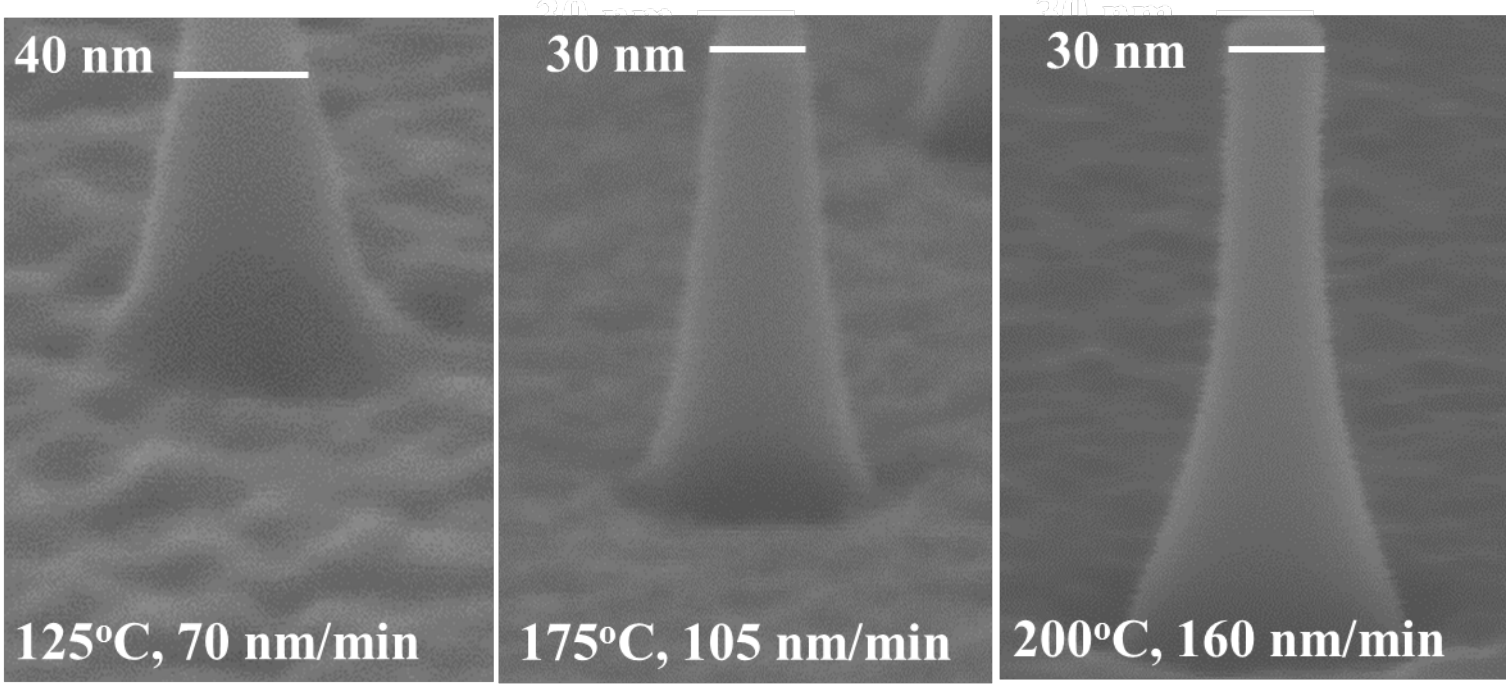


Key enabling technology: RIE by $BCl_3/SiCl_4/Ar$ Chemistry



- Sub-20 nm resolution
- Aspect ratio > 10
- Smooth sidewall and surface
- $BCl_3/SiCl_4/Ar$ RIE chemistry used for III-V optical devices, never used for nm-scale features

Critical parameter: Substrate temperature during RIE



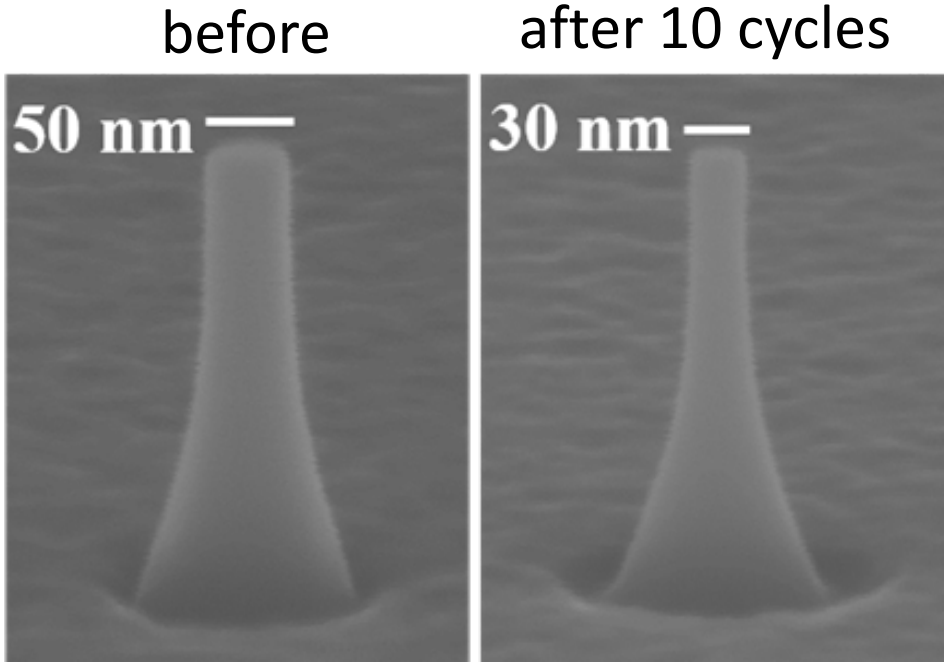
T↑ → etch rate↑, surface roughness↓, sidewall verticality ↑

Nanowire RIE followed by *digital etch*

Digital etch:

Lin, IEDM 2012

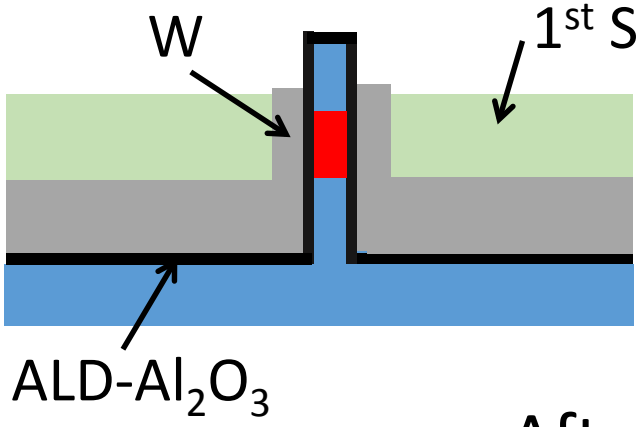
- self-limiting O_2 plasma oxidation + H_2SO_4 oxide removal

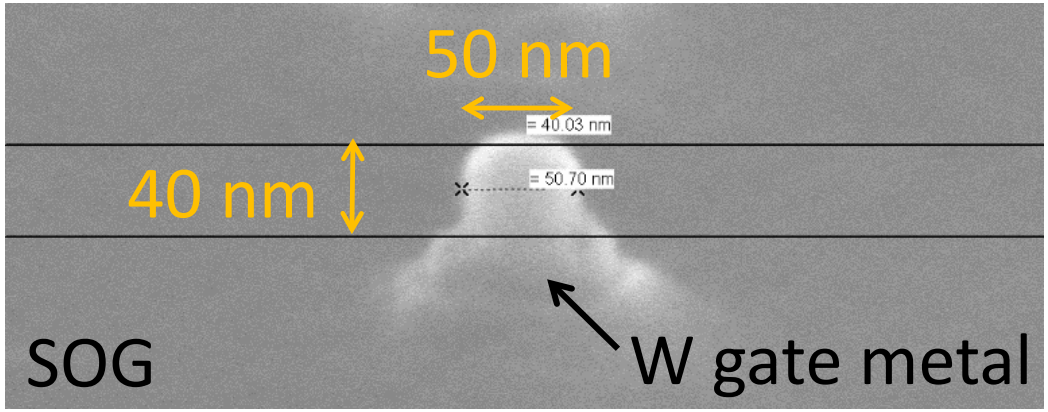


- Shrinks NW diameter by 2 nm per cycle
- Unchanged shape
- Reduced roughness

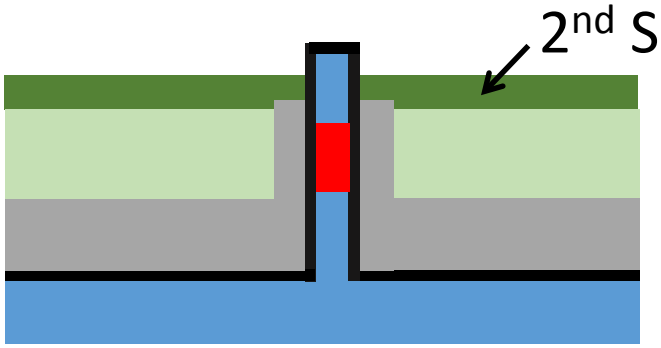
Planarization and etch back

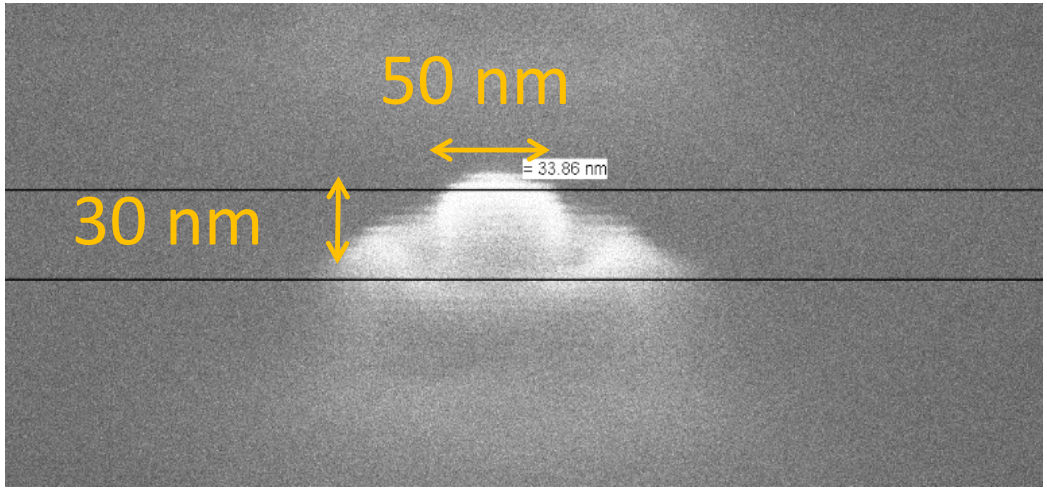
After 1st planarization



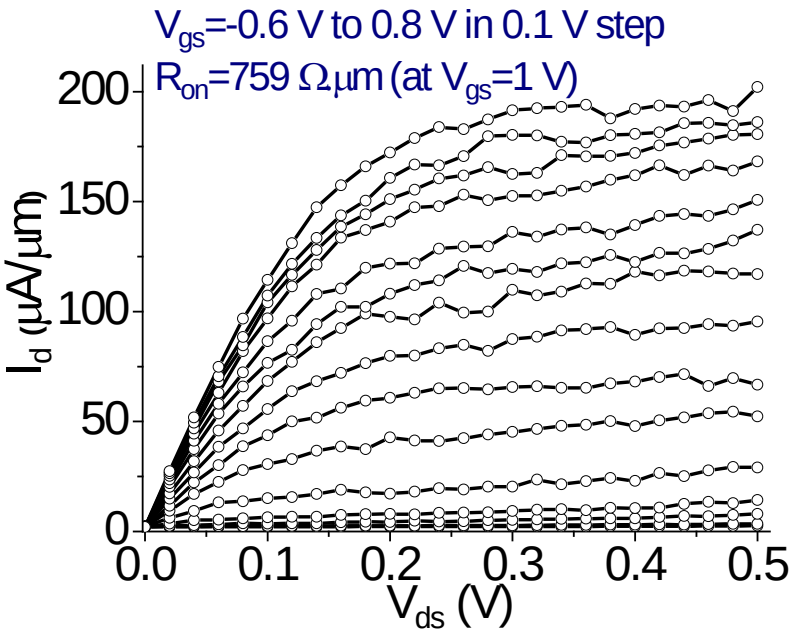


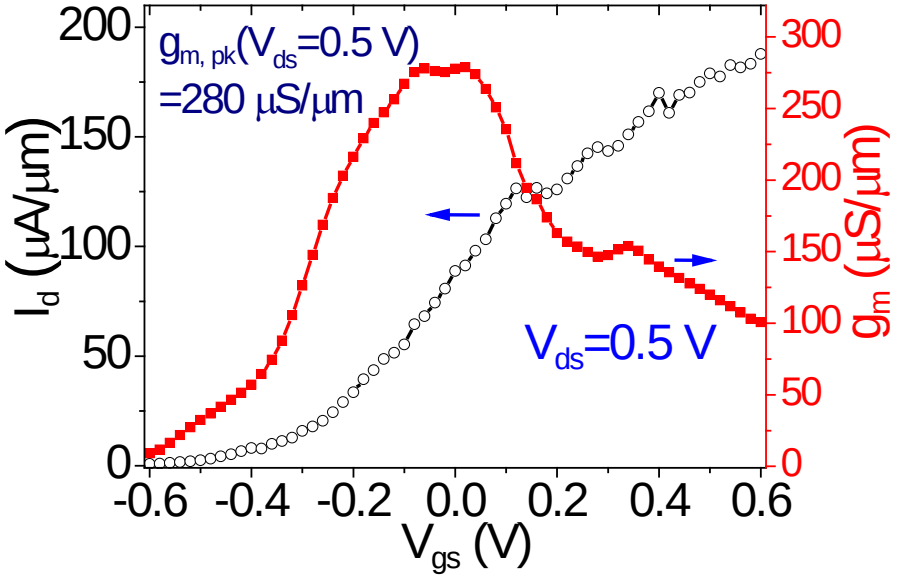
After 2nd planarization





NW-MOSFET I-V characteristics
D= 30 nm





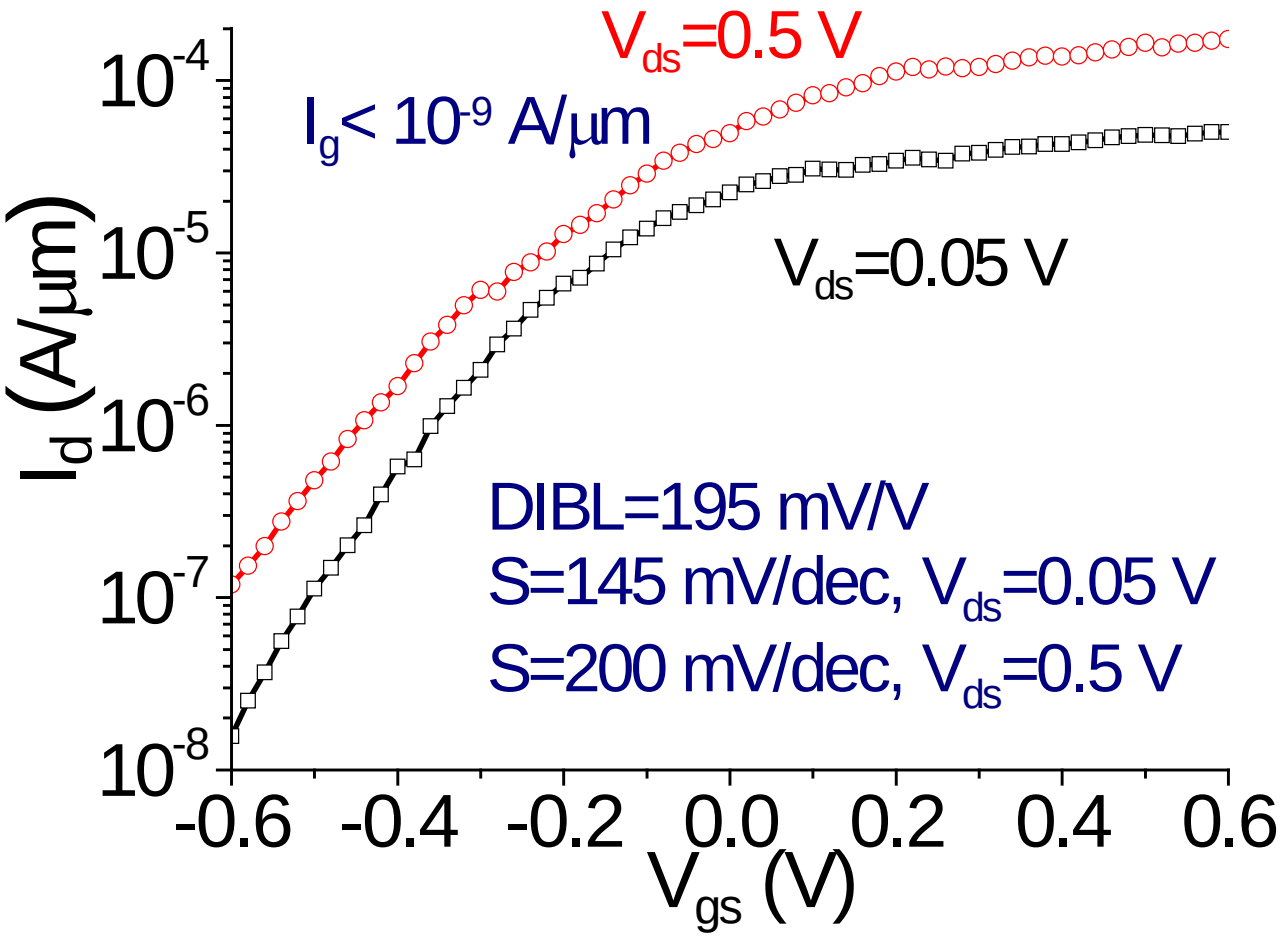
Single nanowire MOSFET:

- D= 30 nm
- L_{ch}= 80 nm
- 4.5 nm Al_2O_3 (EOT = 2.2 nm)

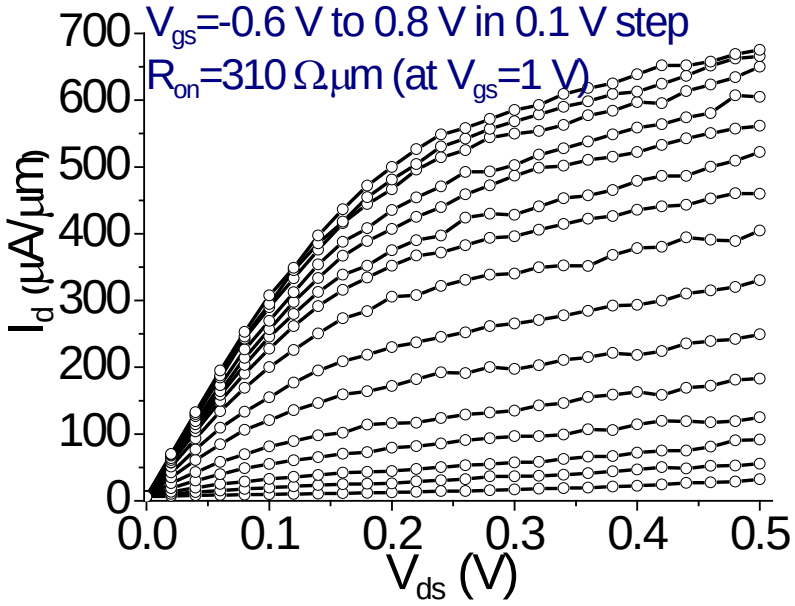
At V_{DS}=0.5 V (normalized by periphery):

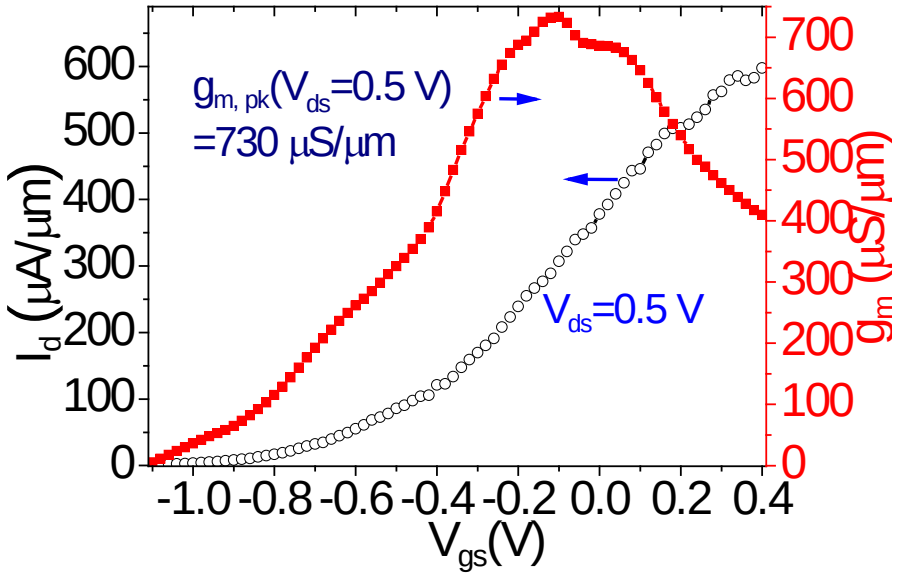
- $g_{m,pk}$=280 μS/μm
- R_{on}=759 Ω.μm

D=30 nm InGaAs NW-MOSFETs



D=50 nm InGaAs NW-MOSFET

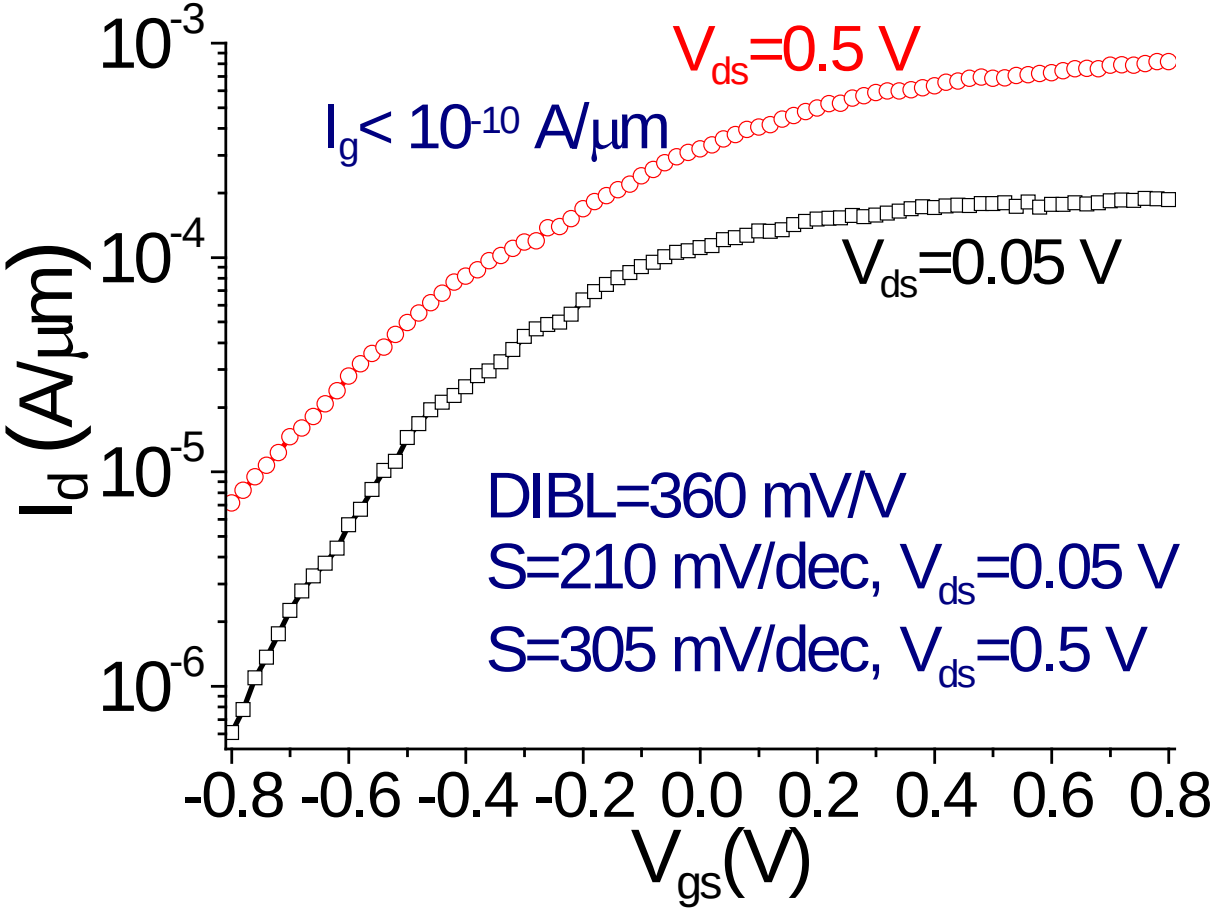




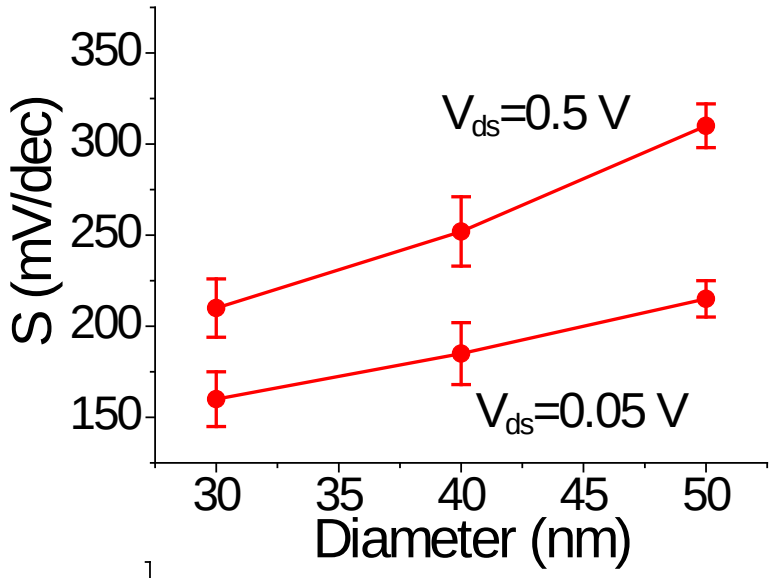
At V_{ds}=0.5 V:

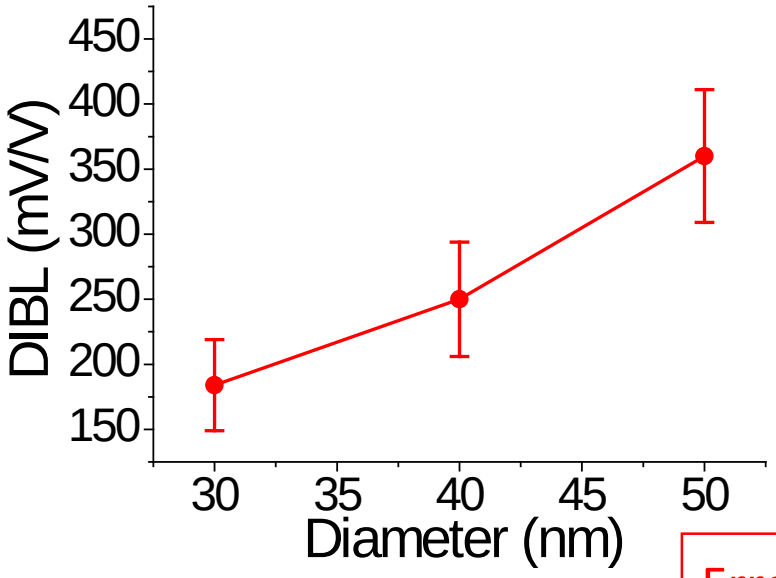
- $g_{m,pk}$=730 μS/μm
- R_{on}=310 Ω.μm

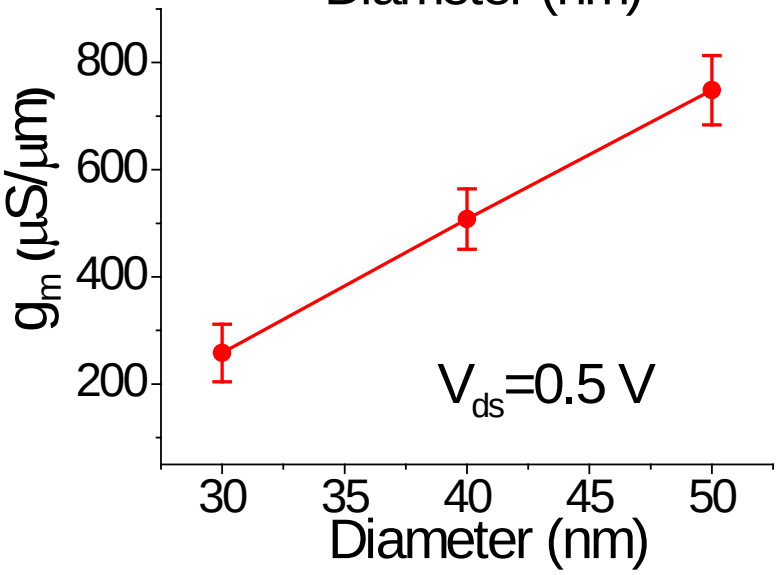
D=50 nm InGaAs NW-MOSFETs

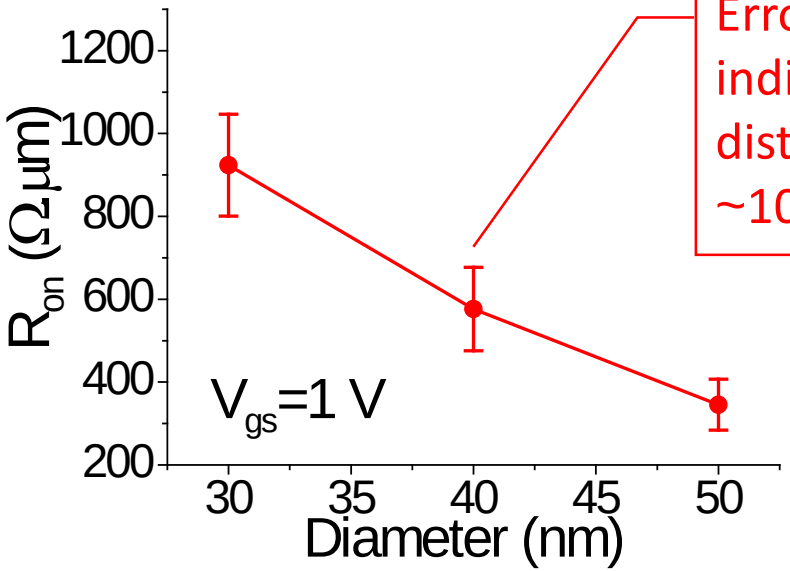


Impact of nanowire diameter









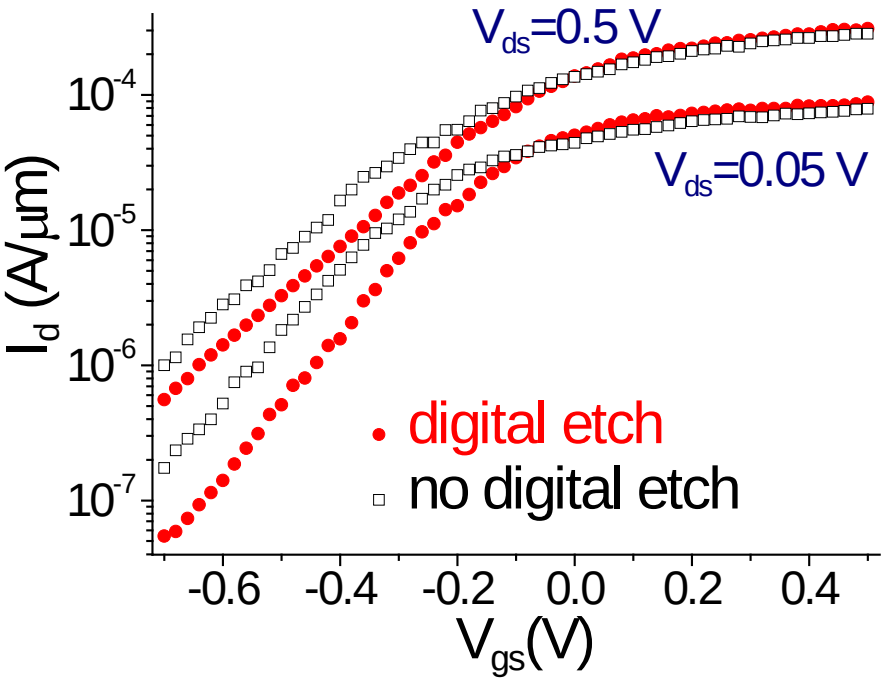
Error bars indicate distribution of ~10 devices

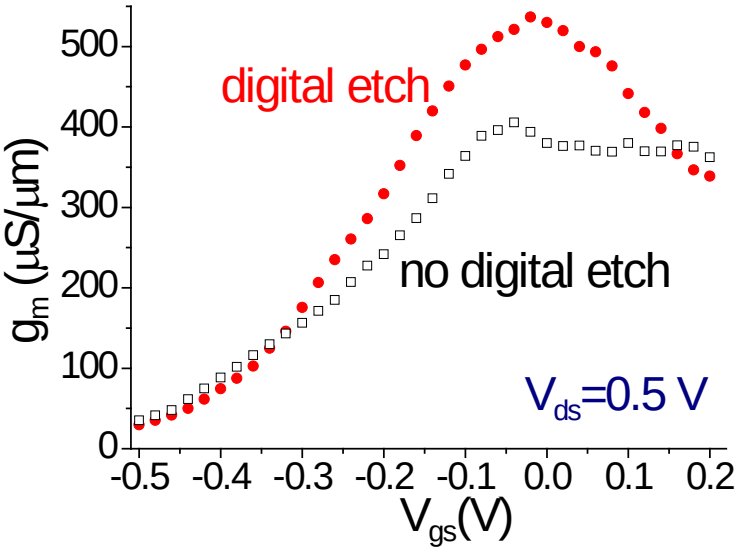
D↓ → S↓, DIBL↓, g_m↓, R_{on}↑

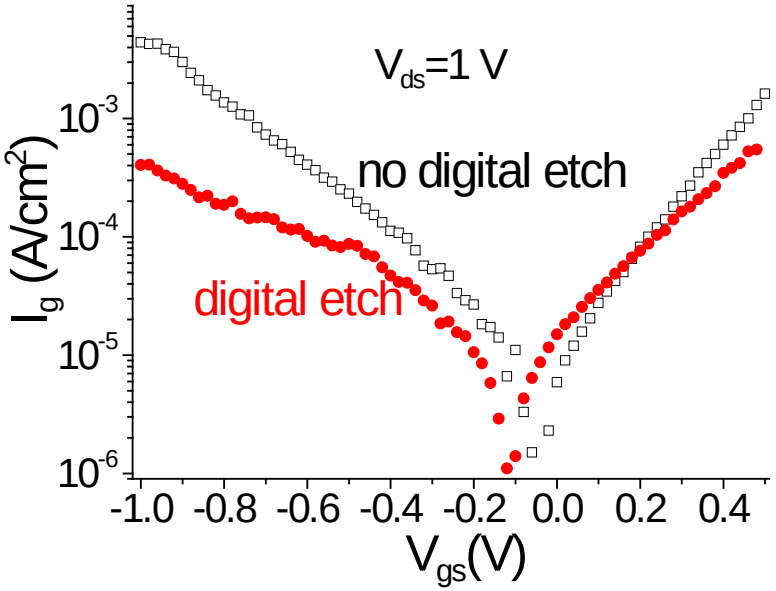
Impact of digital etch

Single nanowire MOSFET:

- D= 40 nm (final diameter)



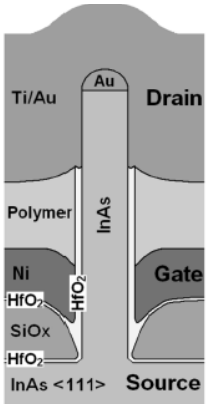




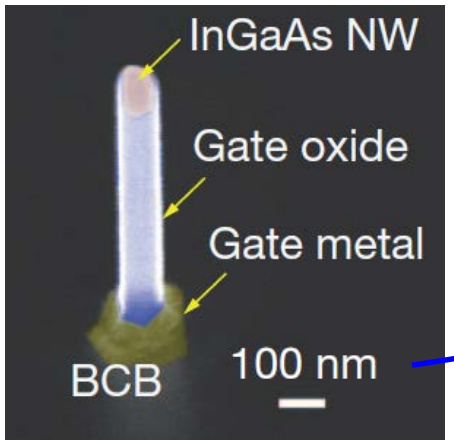
Digital etch → S↓, g_m↑, I_g↓

- Better sidewall interface
- R_{on} and DIBL unchanged

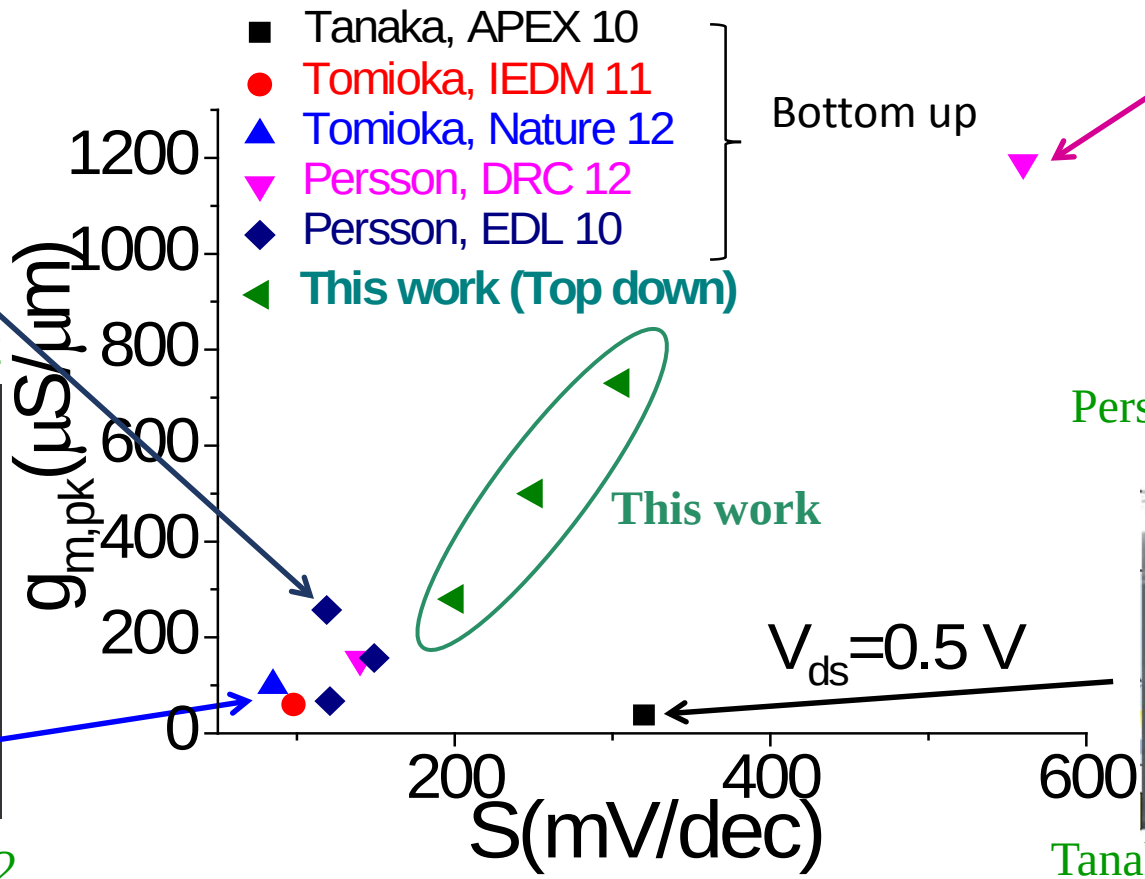
Benchmarking against bottom-up vertical InGaAs NW-MOSFETs

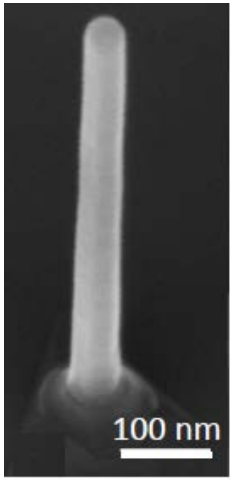


Persson, EDL 2012

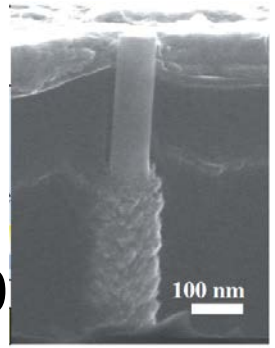


Tomioka, Nature 2012





Persson, DRC 2012



Tanaka, APEX 2010

- Fundamental trade-off between transport and short-channel effects
- Top-down NW-MOSFETs as good as bottom up devices

Conclusions

- First demonstration of top-down III-V GAA NW-MOSFET with vertical channel
  - Novel III-V RIE process with sub-20 nm resolution
  - 30 nm diameter NW MOSFET achieved
- Digital etch improves subthreshold and transport characteristics
- Device performance matches that of best bottom-up vertical NW III-V MOSFETs

Acknowledgement

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- E3S colleagues: A. Lakhani, S. Agarwal, M. Eggleston, E. Yablonovitch, M. Wu