Vertical Nanowire InGaAs MOSFETs Fabricated by a Top-down Approach

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Abstract

Vertical $In_{0.53}Ga_{0.47}As$ Gate-all around (GAA) nanowire (NW) MOSFETs fabricated by a top-down approach are demonstrated experimentally for the first time. The fabrication process features a new III-V dry etch process capable of sub-20 nm diameter NWs with an aspect ratio greater than 10. It also includes a digital etch technique to controllably reduce nanowire diameter and remove dry etch damage. With a channel length L_{ch}=80 nm and EOT=2.2 nm, we obtain a transconductance of 730 µS/µm at 0.5 V in a 50 nm diameter NW MOSFET. The digital etch increases the transconductance by 20% and improves the subthreshold characteristics of the devices. In terms of balance of transport and short-channel effects, our MOSFETs match the best vertical nanowire devices fabricated by bottom-up techniques.

Introduction

Recently, InGaAs has emerged as a promising channel material candidate for future CMOS applications [1]. The GAA nanowire MOSFET is the device architecture with ultimate scaling potential [2]. A vertical NW device structure uncouples gate length scaling and footprint scaling. As a result, device density goals can be reached with far better short-channel effects and performance than in planar MOSFETs, FinFETs or lateral NW-FETs [2]. To date, vertical channel III-V MOSFETs have only been demonstrated through bottom-up fabrication techniques [3-6]. This approach is not considered to be manufacturable as Au particles are used as seeds [4] or difficult to control epitaxial processes are utilized [3, 5]. In this work, we have developed a top-down fabrication process for $In_{0.53}Ga_{0.47}As$ vertical channel GAA NW-MOSFETs that is based on a novel III-V etching technology. We demonstrate NW MOSFETs with diameter (D) down to 30 nm and a performance comparable to the best devices fabricated by bottom-up techniques.

Fabrication Process

Fig. 1 shows a schematic view of the InGaAs NW MOSFETs fabricated here. The process flow is described in Fig. 2. The starting heterostructure (shown in Fig. 1) is grown by MOCVD on an InP wafer. The active channel consists of 80 nm undoped $In_{0.53}Ga_{0.47}As$ sandwiched between two n^+-$In_{0.53}Ga_{0.47}As$ contact regions.

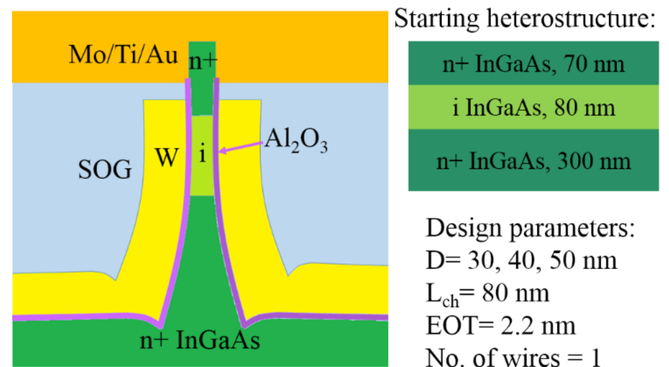

Fig. 1 Schematic of device structure listing design parameters and starting heterostructure.

- HSQ mask definition by EBL
- Nanowire formation by dry etch
- Digital etch
- ALD 4.5 nm Al_2O_3 gate dielectric
- Sputter 40 nm W gate metal
- Gate metal patterning
- Gate/top electrode isolation by planarization and etch back (2 times)
- Contact via opening by dry etch
- Sputter Mo as contact metal
- S/G/D pad formation

Fig. 2 Process flow for vertical GAA InGaAs NW MOSFET.

Device fabrication begins with mask definition for NW formation by e-beam lithography using HSQ. A novel ICP RIE process utilizing $BCl_3/SiCl_4/Ar$ has been developed for Indium-containing compounds which are notoriously difficult to etch [7]. This chemistry has been used for optical devices [7, 8] but its potential for nm-scale feature formation with high aspect ratio has not been recognized before. Fig. 3 (a) shows a D=20 nm NW with an aspect ratio of 10 defined by this technique. It features a smooth sidewall that is very vertical in the top ~50 nm. The footing and trenching that is commonly observed in InGaAs dry etch [9] is also present here. This can be improved through further process

optimization. The devices fabricated in this work are etched to a depth of 290 nm so as to ensure a uniform cross section over the intrinsic channel region. Although only InGaAs is used, this dry etch process can be applied to III-V heterostructures. Fig. 3(b) shows a 20 nm fin profile in an InGaAs/InAlAs/InP heterostructure with no notching.

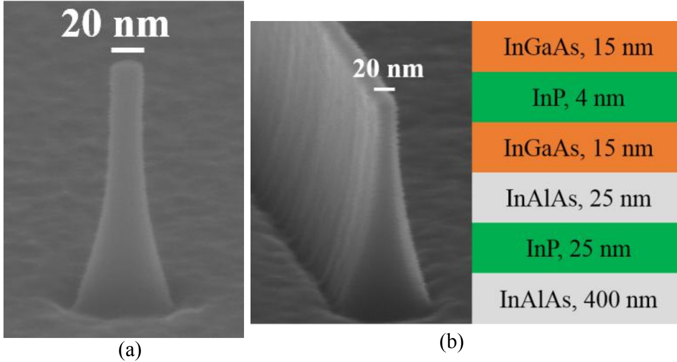

Fig. 3 (a) 20 nm diameter nanowire with an aspect ratio greater than 10 fabricated by RIE. (b) Dry etched 20 nm fin structure (left) in a III-V heterostructure containing InGaAs/InAlAs/InP (right).

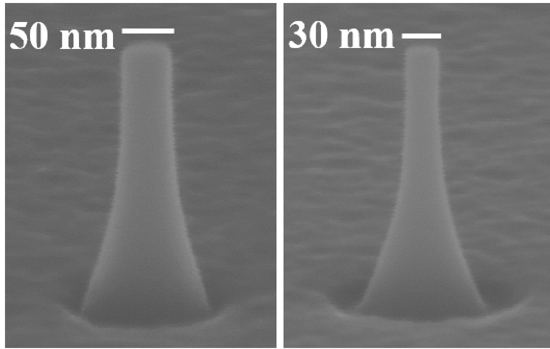

Fig. 4 D=50 nm InGaAs nanowire (left) reduced to D=30 nm (right) after 10 cycles of digital etch.

Our process proceeds with a digital etch (DE) to smooth the NW sidewalls. This consists of a self-limiting O_2 plasma oxidation/diluted H_2SO_4 sequence that reduces the InGaAs nanowire diameter by about 2 nm per cycle. Fig. 4 shows an InGaAs NW before and after 10 cycles of digital etch. The shape is almost unchanged and the sidewall roughness is decreased. After H_2SO_4 cleaning, 4.5 nm ALD Al_2O_3 (EOT=2.2 nm) is deposited on the sidewalls. A 40 nm thick W gate is immediately sputtered. Spin-on glass (SOG) is applied (1 hr baking at 350°C) and etched back until the overlap between the gate and the top n^+ region is reduced to 10 nm. Fig. 5 shows a SEM image of a device at this stage in the process (SOG removed). A second etch back process is used to isolate the gate metal from the top contact metal. After vias are opened, 40 nm Mo is sputtered as top contact metal. The process ends with lift-off of Ti/Au S/G/D pads.

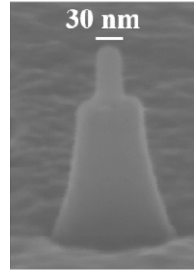

Fig. 5 SEM image of a D=30 nm device after 1st planarization and etch back (SOG and dielectric removed in BOE). The intrinsic region and the bottom n^+ region of the nanowire are wrapped around by W. The top n^+ region is exposed for ohmic contact. The roughness on the ground plane is caused by the erosion of W in BOE.

Results and Discussion

All devices have a channel length of 80 nm. This is set by the undoped InGaAs layer thickness. Figs. 6-8 show the electrical characteristics of a single D=30 nm NW MOSFET. As is common, I_d and g_m are normalized by the nanowire circumference (πD). The output characteristics demonstrate excellent saturation at low V_{ds} with R_{on} = 759 Ω·μm (8062 Ω) at V_{gs}=1 V. A peak g_m of 280 μS/μm is extracted at V_{ds}=0.5 V. Subthreshold swing of 145 mV/dec at 0.05 V and 200 mV/dec at 0.5 V are obtained. This can be improved with further surface treatment and proper annealing [10]. DIBL is 195 mV/V. The gate leakage current is below 10^{-9} A throughout the measurement range. Fluctuations in the drain current measurement are observed that are attributed to the single nanowire nature of this device [11].

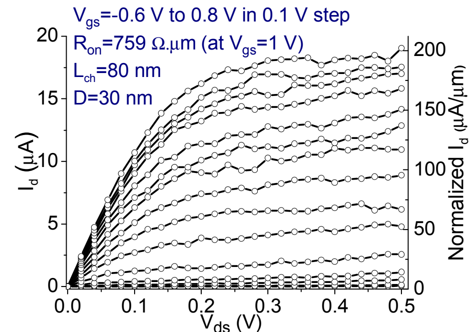

Fig. 6 Output characteristics of a D= 30 nm InGaAs single NW MOSFET.

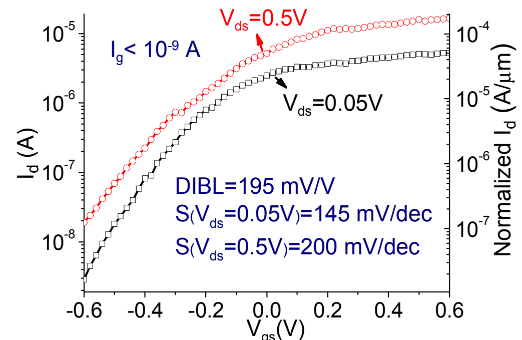

Fig. 7 Subthreshold characteristics of the device shown in Fig. 6.

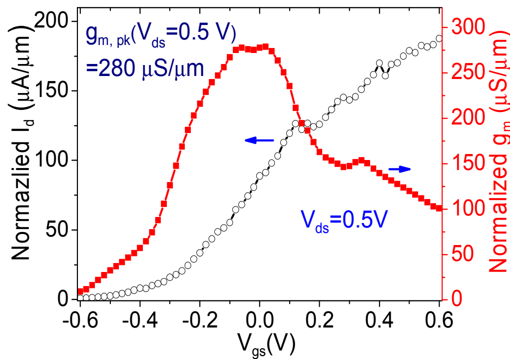

Fig. 8 Transfer and g_m characteristics at V_{ds}=0.5 V of the device shown in Figs. 6 and 7.

Electrical properties of a single nanowire device with D= 50 nm are shown in Figs. 9-11. The electrostatics are worse than D=30 nm device, as evidenced by increased S (210 mV/dec at V_{ds}=0.05 V) and DIBL (360 mV/V). However, R_{on} is reduced by a factor of 4 and a high $g_{m,pk}$ of 730 μS/μm at V_{ds}= 0.5 V is achieved. R_{on} is believed to be dominated by contact resistance of the top n^+ region due to the small contact area. The level of current fluctuation is also reduced as the nanowire diameter widens.

The impact of digital etch can be appreciated in Fig. 12

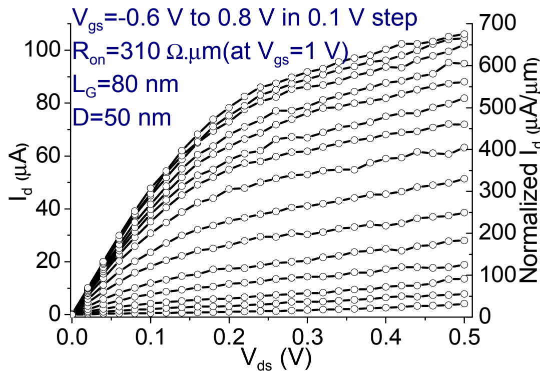

Fig. 9 Output characteristics of a D= 50 nm InGaAs single NW MOSFET.

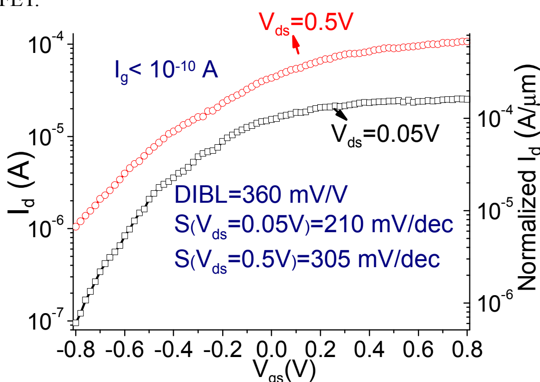

Fig. 10 Subthreshold characteristics of the device shown in Fig. 9.

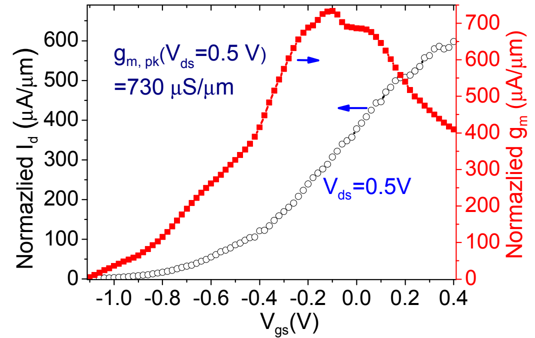

Fig. 11 Transfer and g_m characteristics at V_{ds}=0.5 V of the device shown in Figs. 9 and 10.

that shows the subthreshold characteristics of D=40 nm devices with and without digital etch (output characteristics of the device without digital etch shown in Fig. 13). The starting NW diameter is different so that after digital etch of one of them, both final diameters are identical. The digital etch improves the interface quality as evidenced by a reduction in S from 220 mV/dec to 180 mV/dec. Interestingly, DIBL is not affected. However, the threshold voltage V_t (defined at 1 μA/μm at V_{ds}=0.05 V) shifts positive by about 0.1 V as a result of digital etch. This could be due to the elimination of B^+ ions incorporated at the sidewalls during the RIE process [8]. The digital etch also improves transport, as evidenced by a 25% increase in the peak g_m (from 402 to 498 μS/μm at V_{ds}=0.5 V). Fig. 14 shows that gate leakage also significantly decreases by

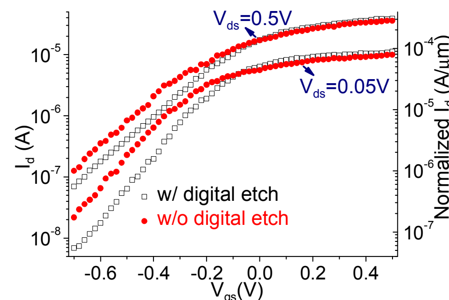

Fig. 12 Impact of digital etch on characteristics of D=40 nm devices. This is the final device diameter.

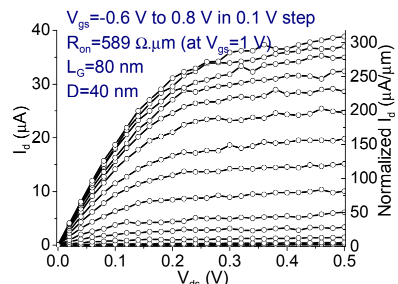

Fig. 13 Output characteristics of a D= 40 nm InGaAs single NW MOSFET fabricated without digital etch.

digital etch.

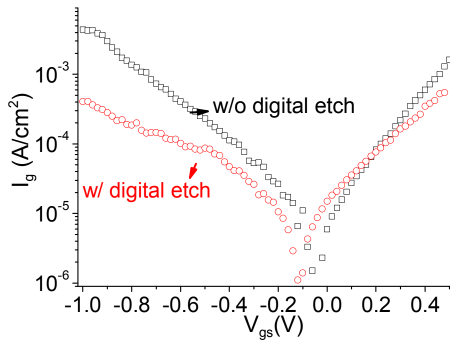

Fig. 14 Impact of digital etch on gate leakage current of D=40 nm single NW MOSFETs.

Figs. 15 show the evolution of key figures of merit as a function of final NW diameter for devices fabricated with and without digital etch. S and DIBL greatly improve as D is reduced, as expected. Peak normalized g_m is reduced as D is decreased. This is probably due to the strong dependence of series resistance on D that is evident in Fig. 15(d). Thus, a trade-off between transport (best indicated by $g_{m,pk}$) and electrostatics (measured by S) is observed in vertical

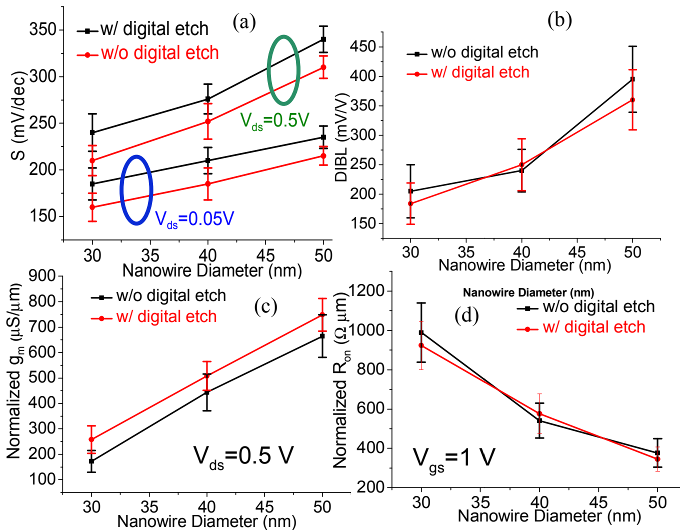

Fig. 15 Key device figures of merit vs. final nanowire diameter for devices fabricated with and without digital etch (over 10 devices for each nanowire diameter are measured): (a) Linear (V_{ds}=0.05 V) and saturated (V_{ds}=0.5 V) subthreshold swing, (b) DIBL, (c) Normalized g_m (V_{ds}=0.5 V), and (d) Normalized R_{on}.

InGaAs NW MOSFETs of different diameters. The digital etch improves S and g_m but does not affect DIBL and R_{on}.

Fig. 16 benchmarks the transport and electrostatics in recently published vertical III-V single NW MOSFETs by plotting $g_{m,pk}$ vs. S, both at V_{DS}=0.5 V. All but ours are fabricated through bottom-up techniques. It is clear that there is a trade-off between transport and short-channel effects in all NW MOSFETs and that our first-generation devices perform as well as the best vertical InGaAs and InAs NW transistors fabricated by bottom-up techniques.

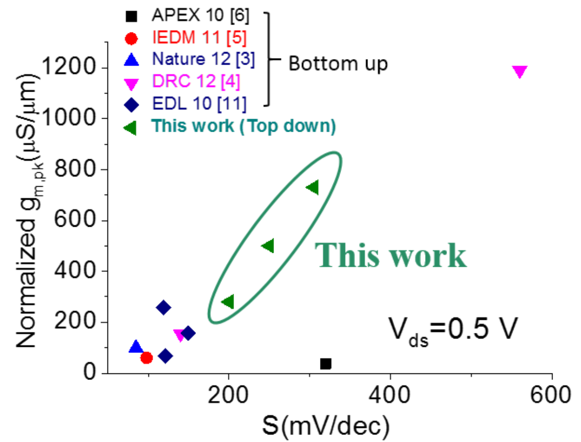

Fig. 16 $g_{m,pk}$ vs. S at V_{ds}=0.5 V for individual vertical InGaAs and InAs NW MOSFETs. A trade-off is evident. All devices but ours are fabricated through bottom-up techniques.

Conclusions

We have demonstrated the first III-V GAA NW-MOSFET with a vertical channel fabricated by a top-down approach. Utilizing a novel III-V RIE process and a digital etch technique, we have obtained a peak g_m=730 μS/μm at V_{ds}=0.5 V, despite a thick EOT=2.2 nm on a device with D=50 nm. Digital etch improves both the subthreshold characteristics and the transport properties. An enhancement of 20% in the peak g_m is observed. Our devices demonstrate a performance in terms of the balance between short-channel effects and transport that matches that of the best vertical NW III-V MOSFETs fabricated by bottom-up techniques.

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