A New Self-aligned Quantum-Well MOSFET Architecture Fabricated by a Scalable Tight-Pitch Process

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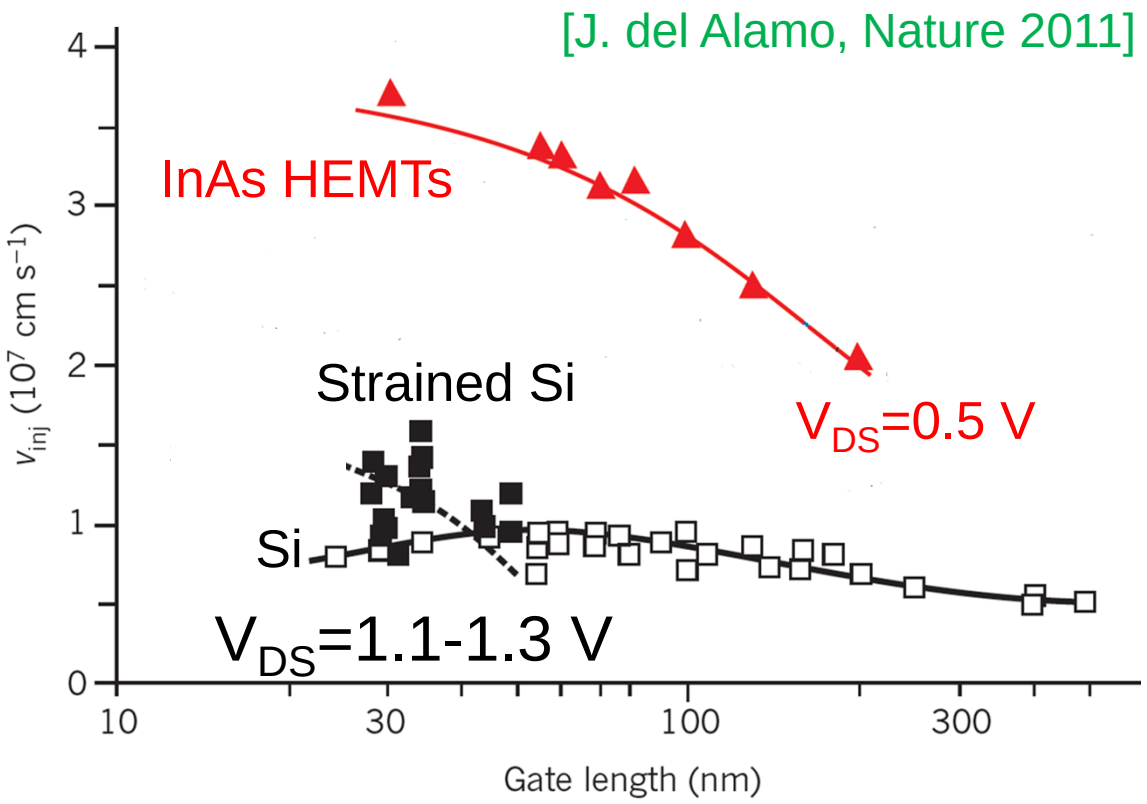
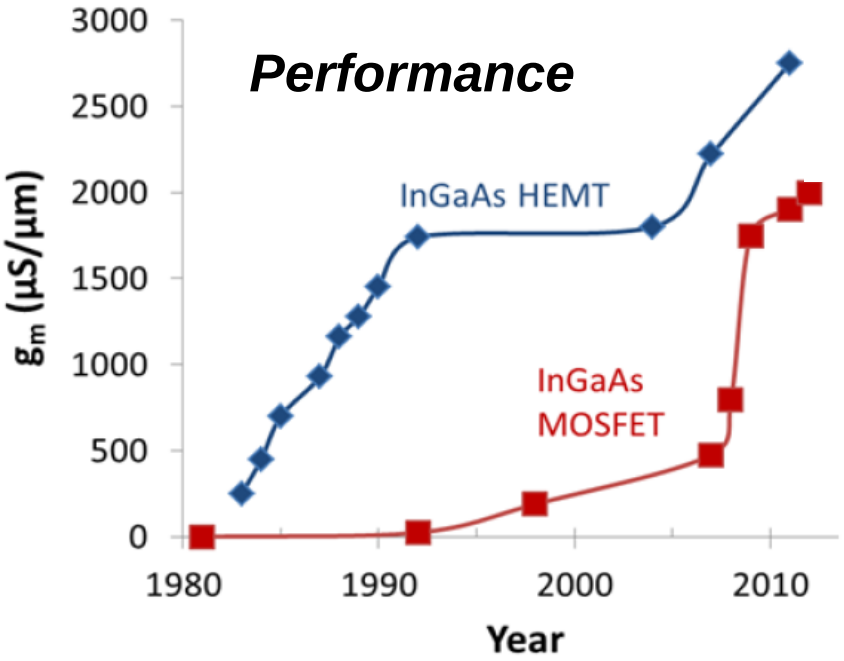
Sponsors: FCRP-MSD Center, Intel,
E3S STC, MIT SMA and SMART

Motivation

- Superior electron transport properties in InAs channel



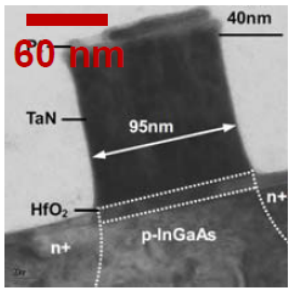
InGaAs MOSFET evolution



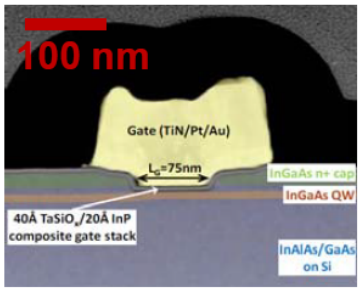
(Kim, IEDM 2012)

[del Alamo, ESSDERC 2013]

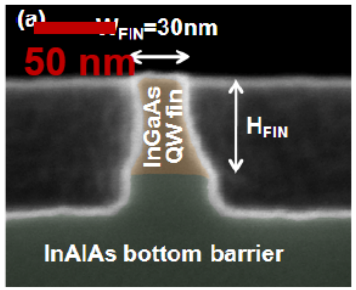
Fabrication and Scaling



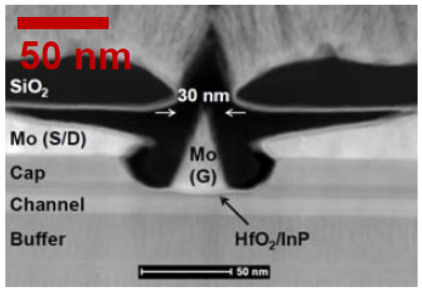
2008 (Lin)



2009 (Radosavljevic)

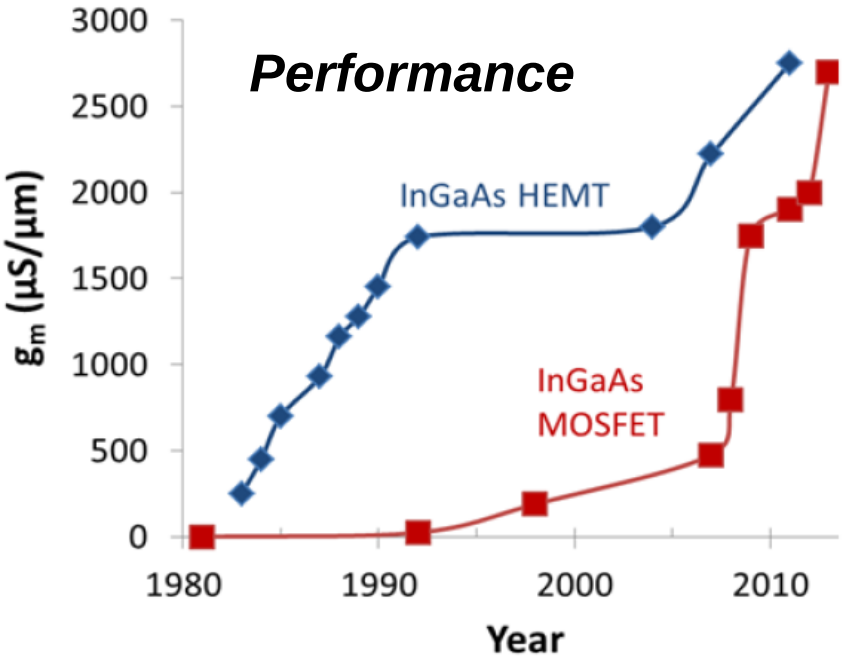


2010 (Radosavljevic)



2012 (Lin)

InGaAs MOSFET evolution



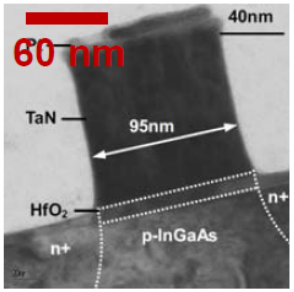
(This work)

(Kim, IEDM 2012)

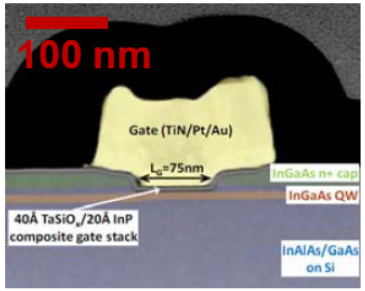
[del Alamo, ESSDERC 2013]

Fabrication and Scaling

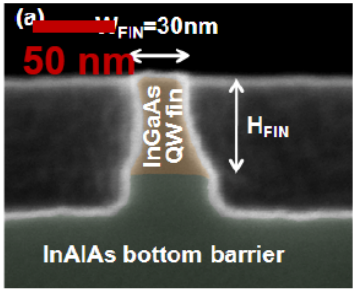
2000s → 2013



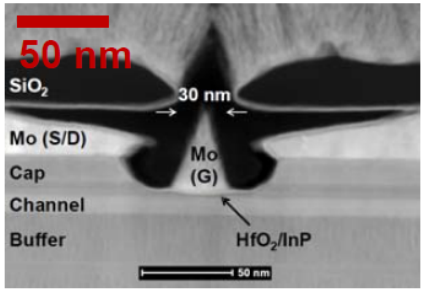
2008 (Lin)



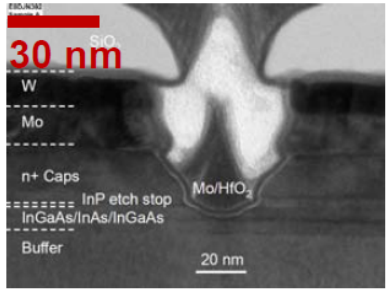
2009 (Radosavljevic)



2010 (Radosavljevic)



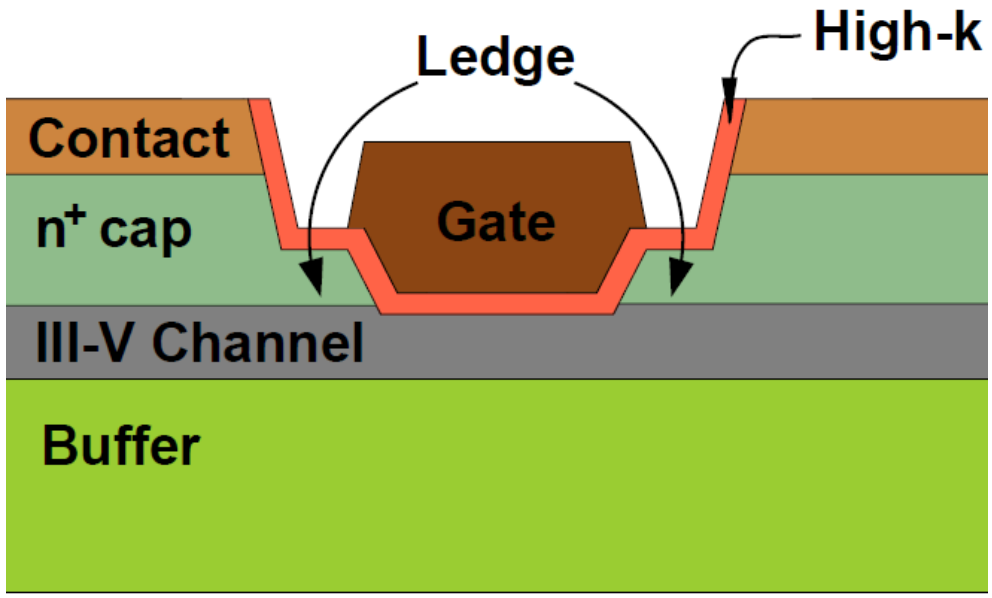
2012 (Lin)



2013 (This work)

New InGaAs MOSFET with self-aligned LEDGE

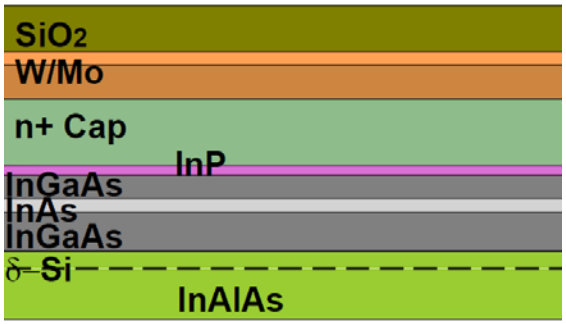
- Bottleneck to ON current is R_{sd}
- Introduction of highly conductive **"LEDGE"**
  - n^+ region linking metal contact and channel



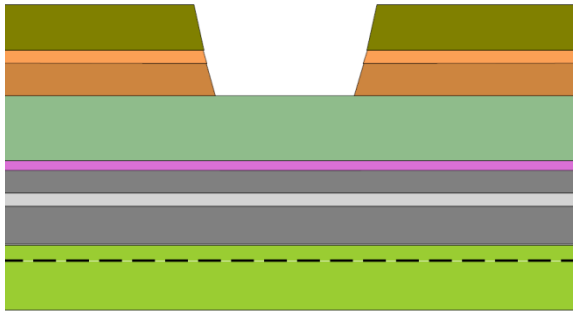
Process integration

Key features: Wet-etch free / Lift-off free / Au free

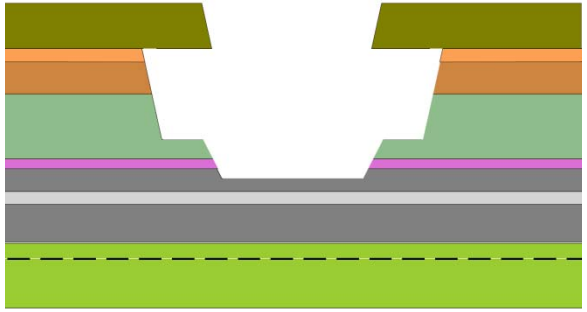
Ohmic/Oxide deposition*



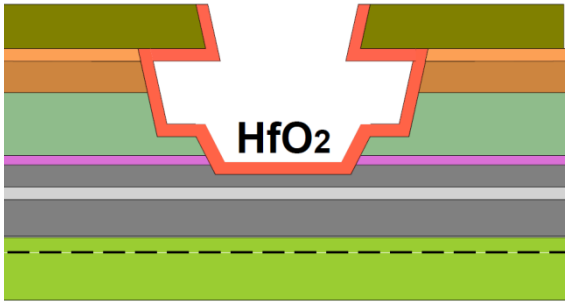
Gate opening



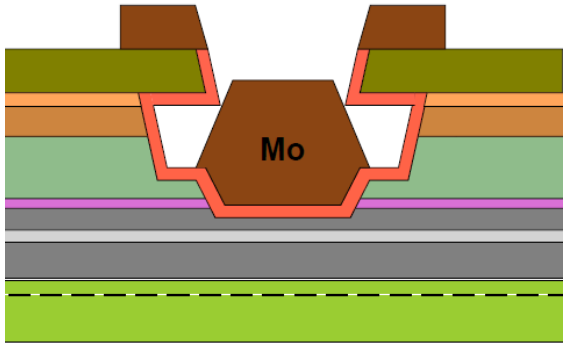
3-step gate recess



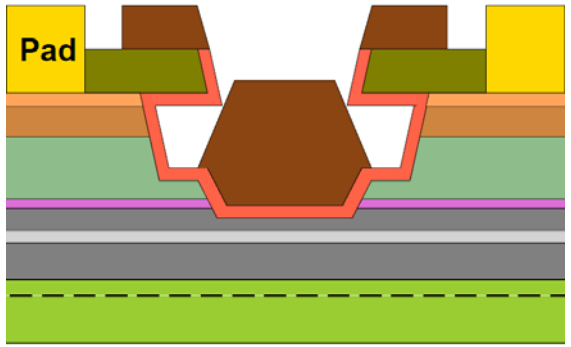
ALD deposition



Gate metal

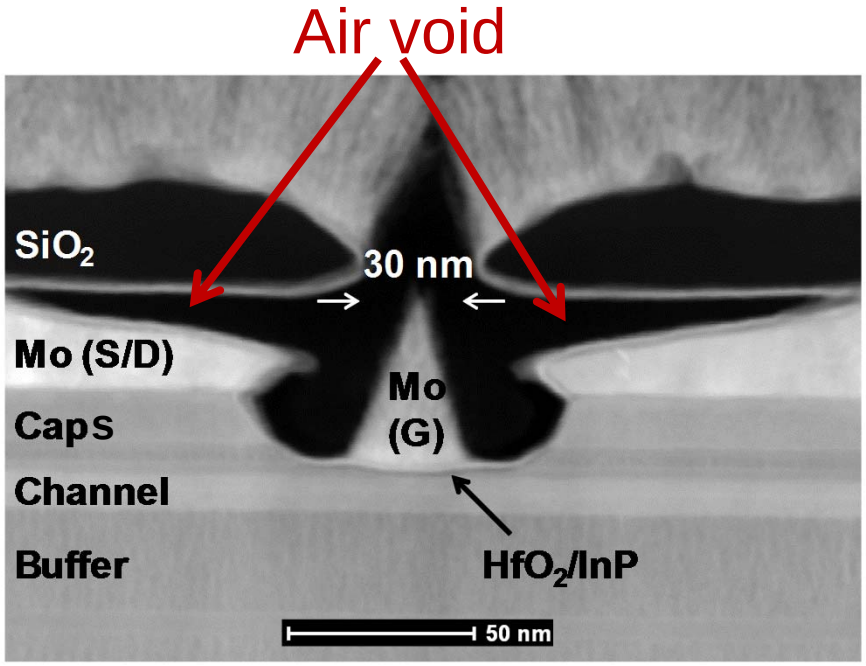


Pad formation

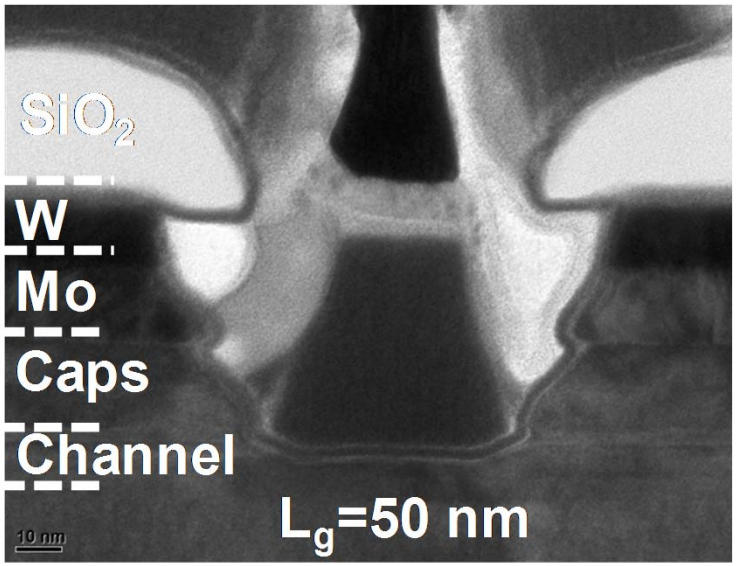


Composite W/Mo contact

- Without W: Long undercut of Mo due to oxidation
  - Limits S/D metal spacing
- With W: No Mo oxidation



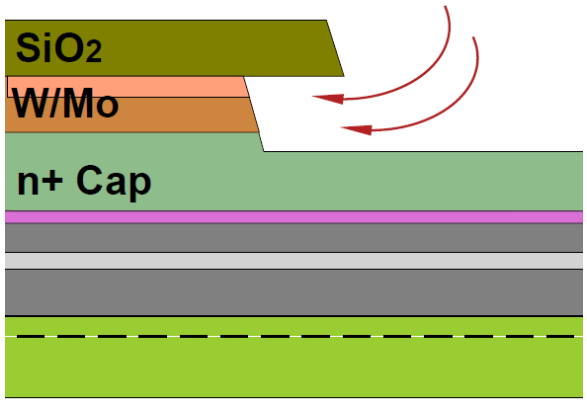
[Lin, IEDM 2012]



This work

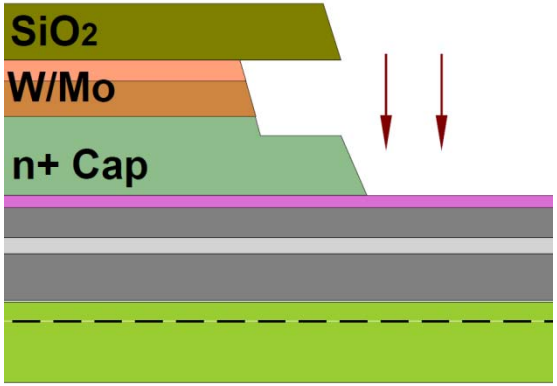
3-step gate recess process

CF_4+O_2 RIE *



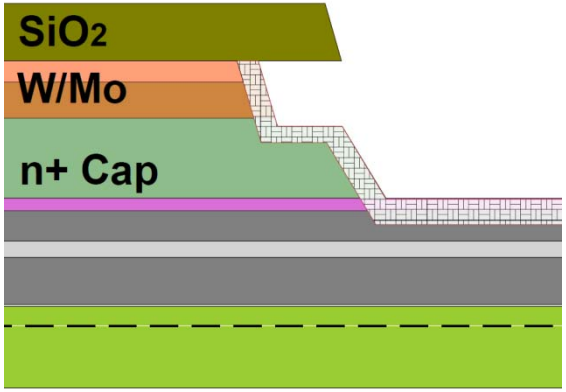
*[Waldron, IEDM 2007]

Cl-based RIE



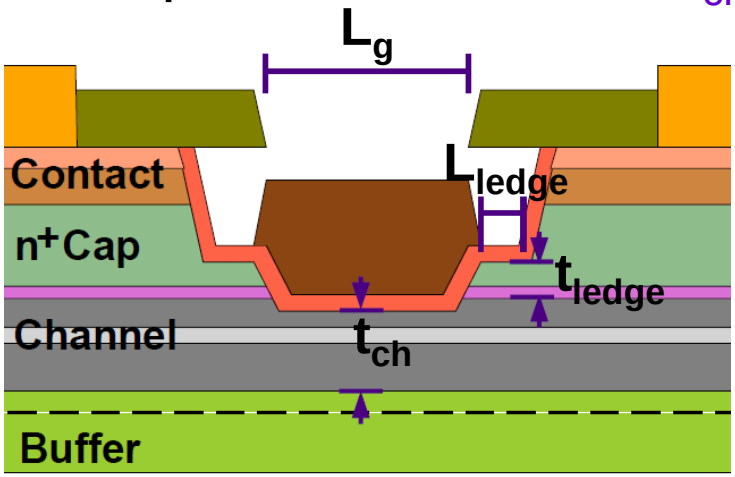
Digital etch*:

O_2 plasma + H_2SO_4



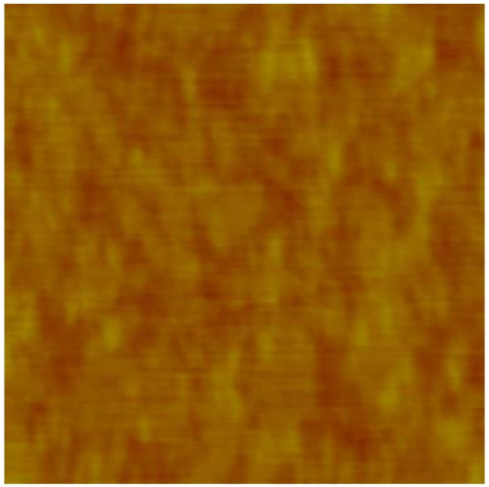
*[Lin, EDL submitted]

Process enables precise control of: t_{ch} / L_{ledge} / t_{ledge}



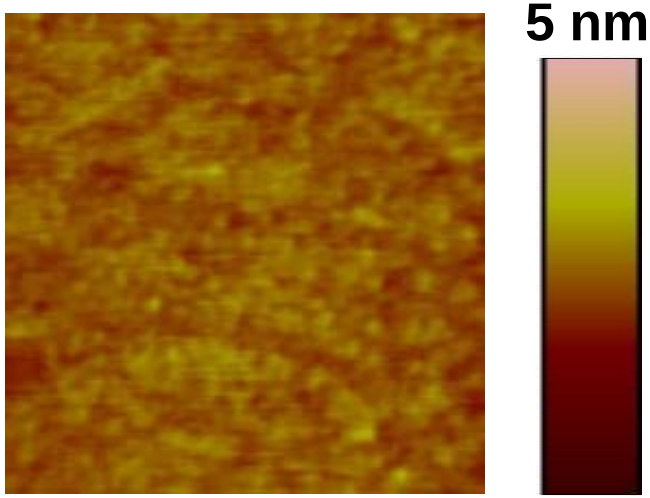
Semiconductor surface after recess

Only wet cleaning (no etching)



RMS = 0.12 nm

Additional cap dry etch (~ 20 nm) + 4 cycle digital etch

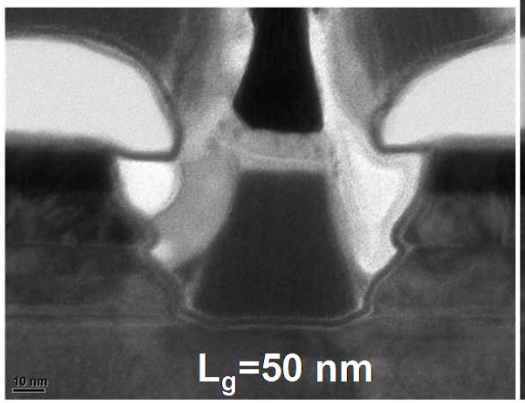


RMS = 0.21 nm

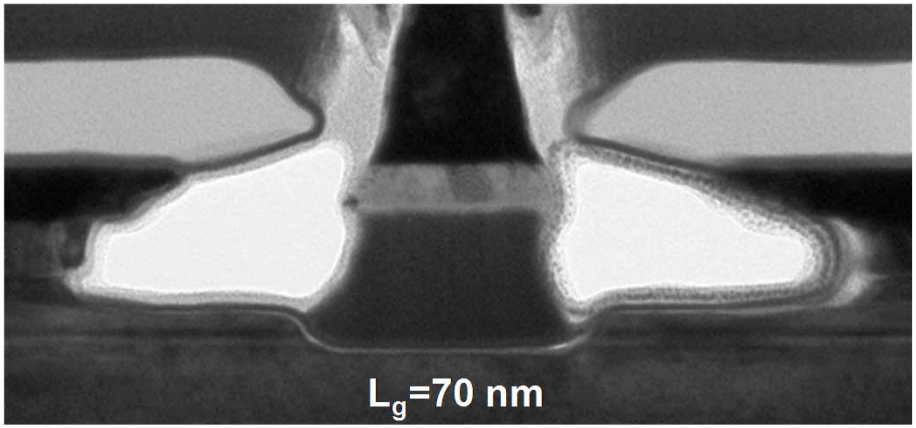
Scanning area: 2x2 μm^2

Structure design: Ledge

Short Ledge

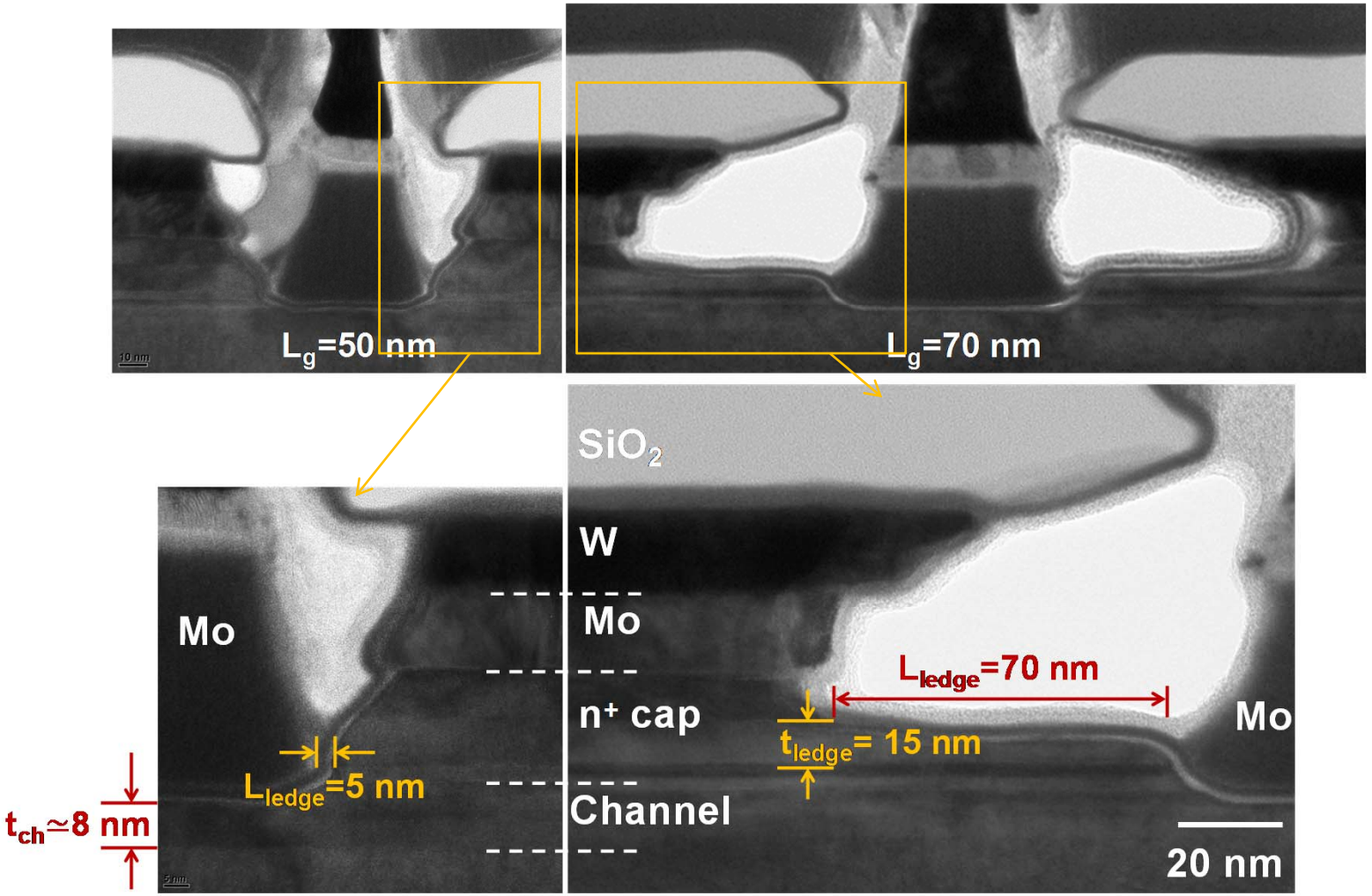


Long Ledge



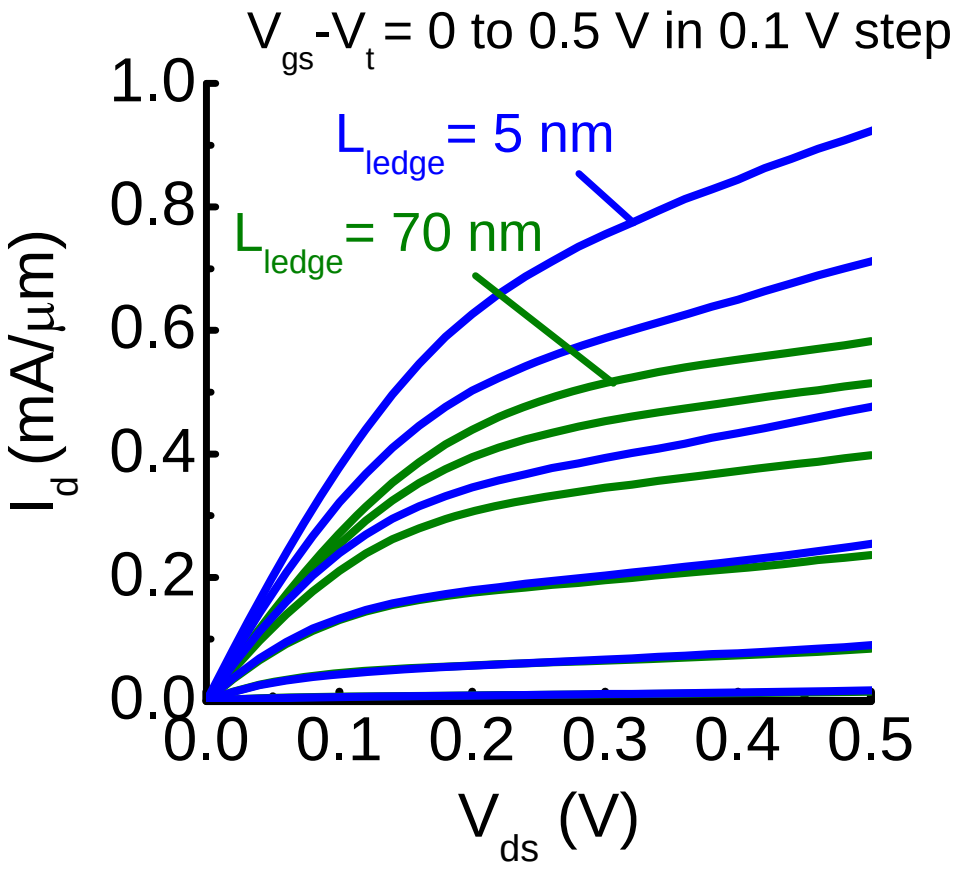
Structure design: Ledge

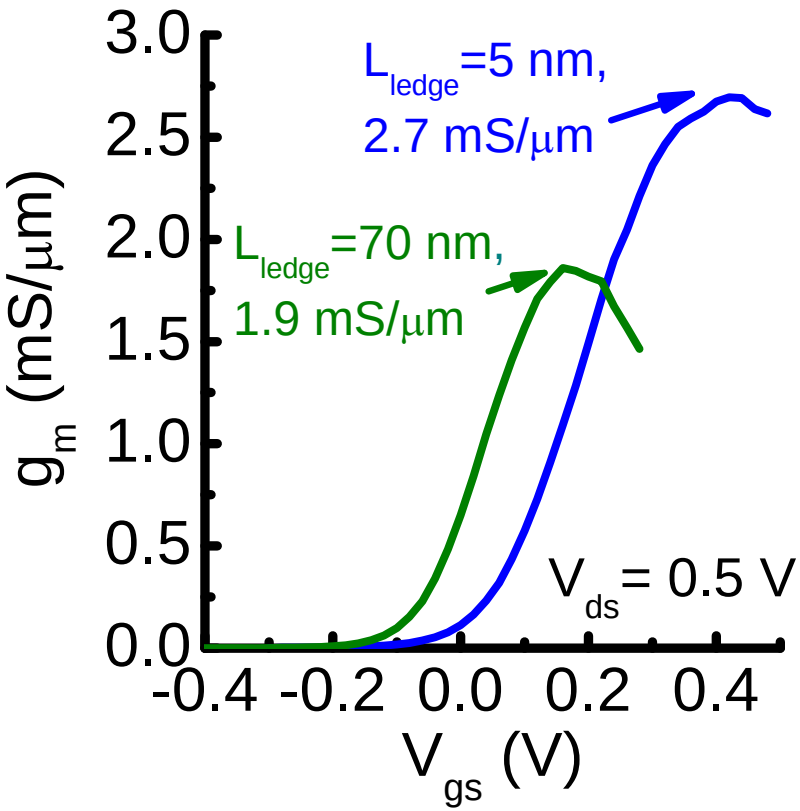
Short Ledge *Long Ledge*



- Surface channel: $In_{0.7}Ga_{0.3}As$ / InAs / $In_{0.7}Ga_{0.3}As$ = 1/2/5 nm
- High-k: HfO_2 , thickness =2.5 nm (EOT~0.5 nm)

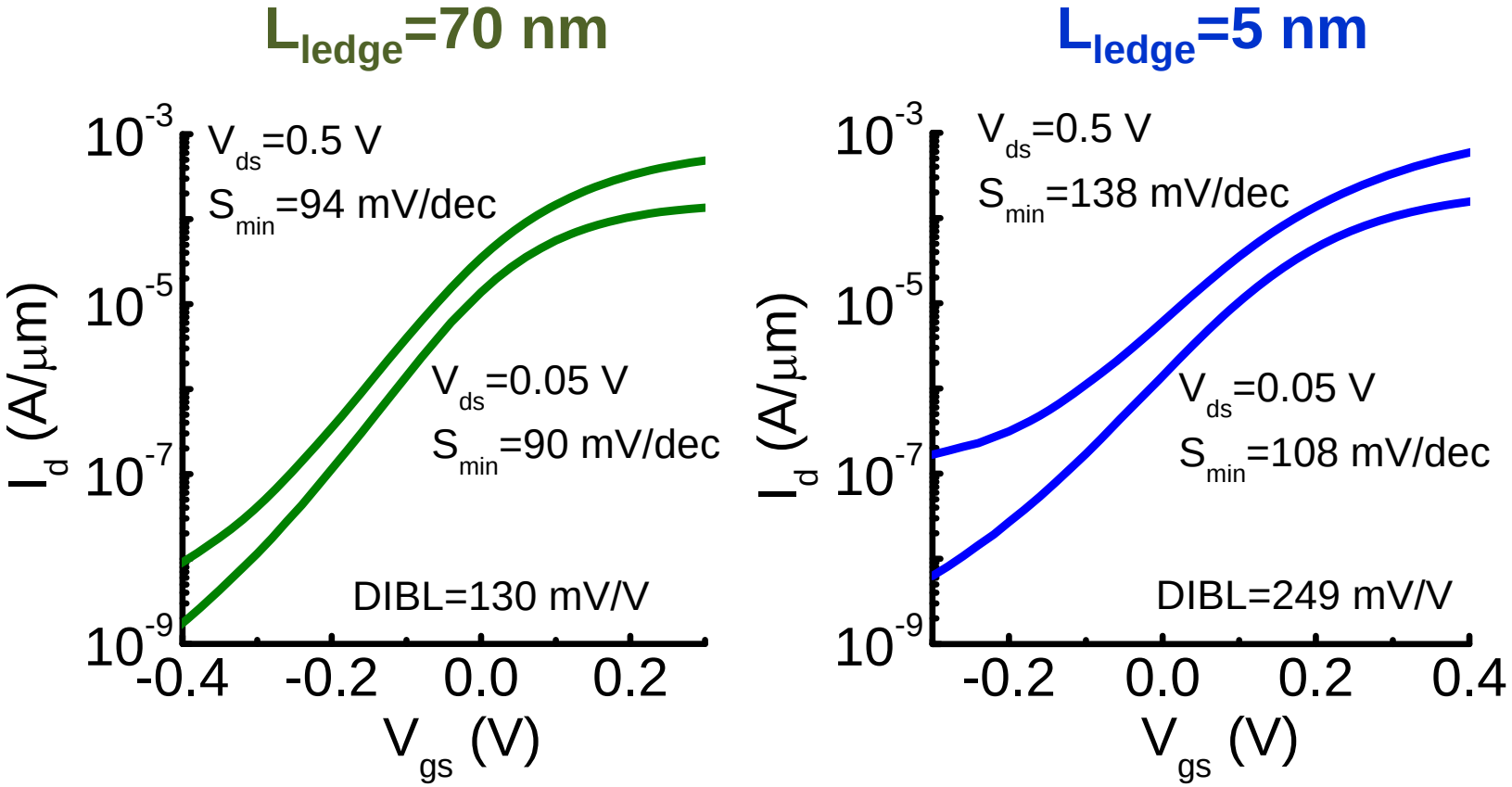
Output and g_m characteristics for L_g = 70 nm





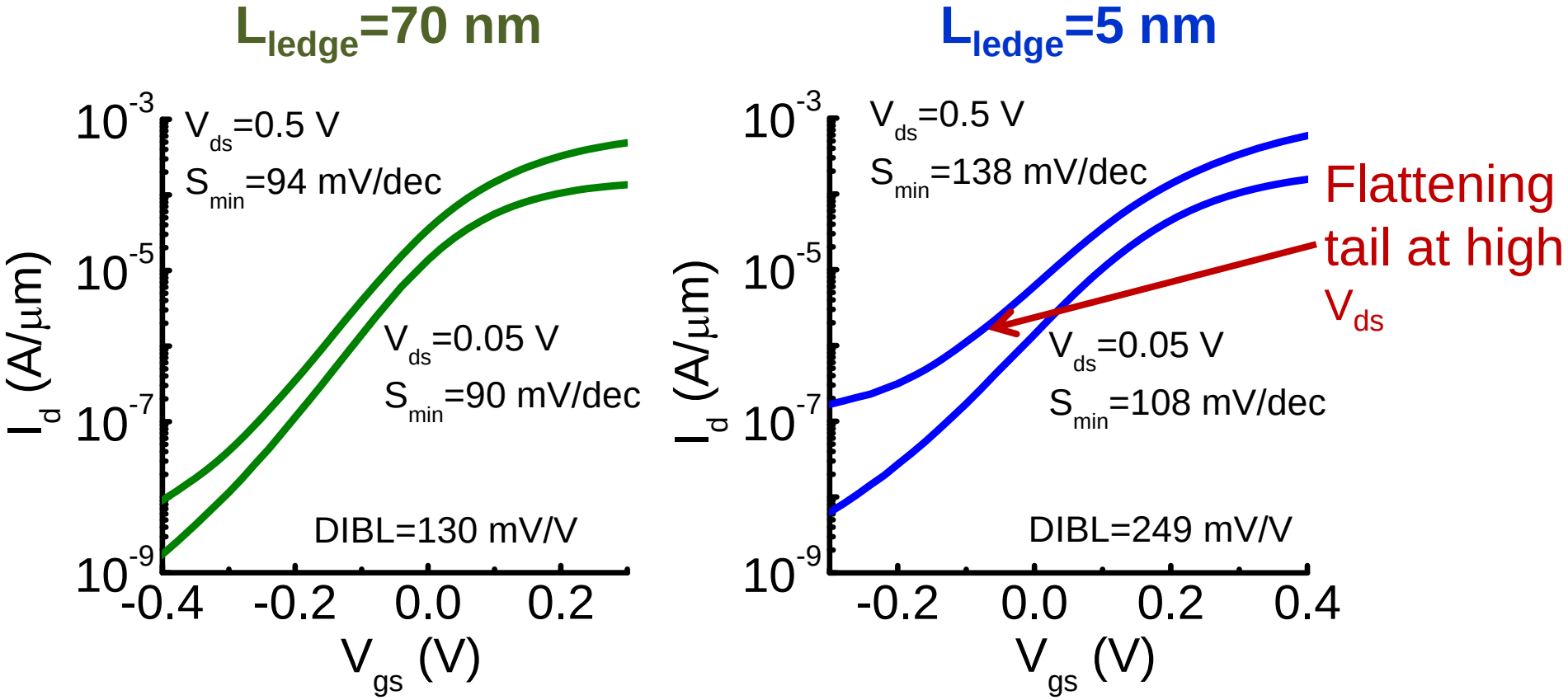
- R_{on} = 220 Ω.μm for L_{ledge}= 5 nm
- Record $g_{m,max}$ = 2.7 mS/μm at V_{ds}= 0.5 V for L_{ledge}= 5 nm

Subthreshold characteristics



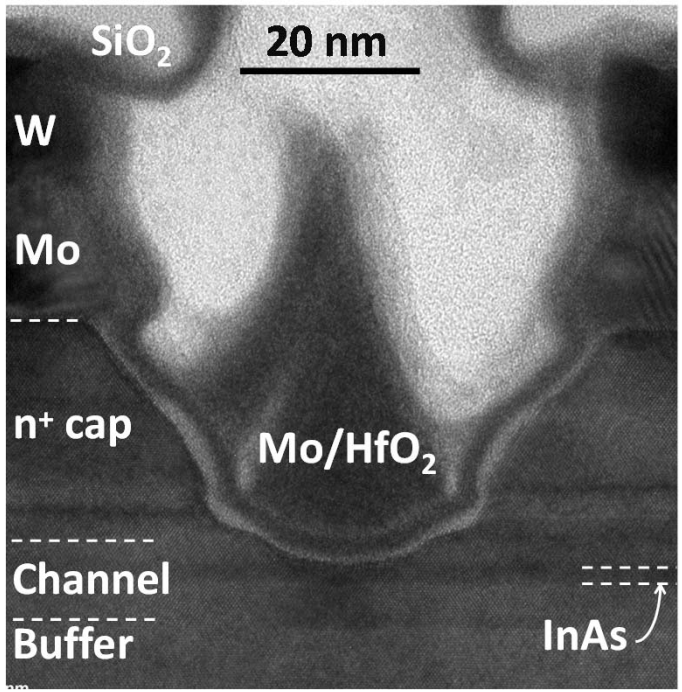
- I_g < 10 pA/μm over entire voltage range
  - Further EOT scaling possible

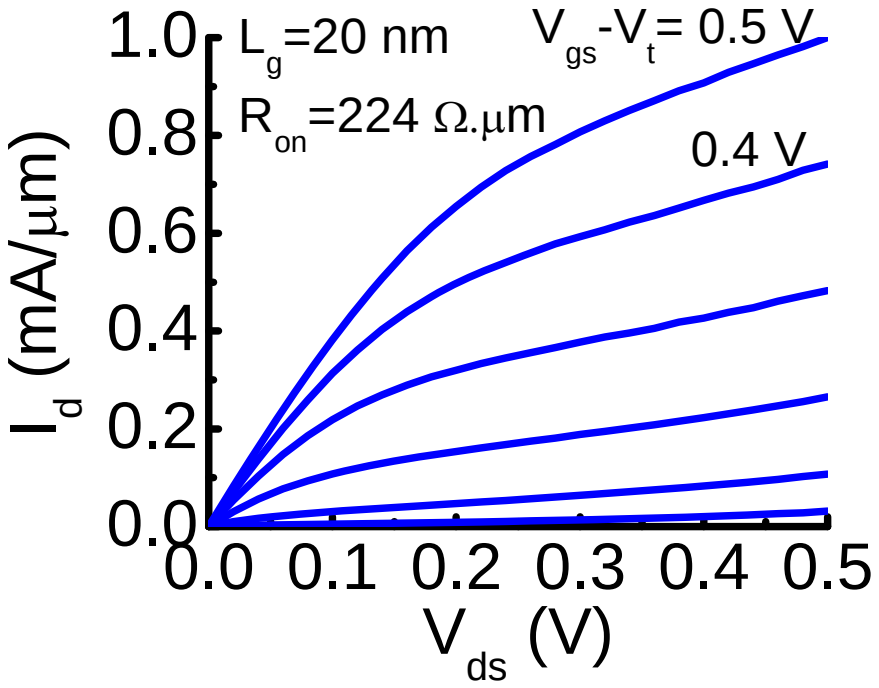
Subthreshold characteristics



- I_g < 10 pA/μm over entire voltage range
  - Further EOT scaling possible

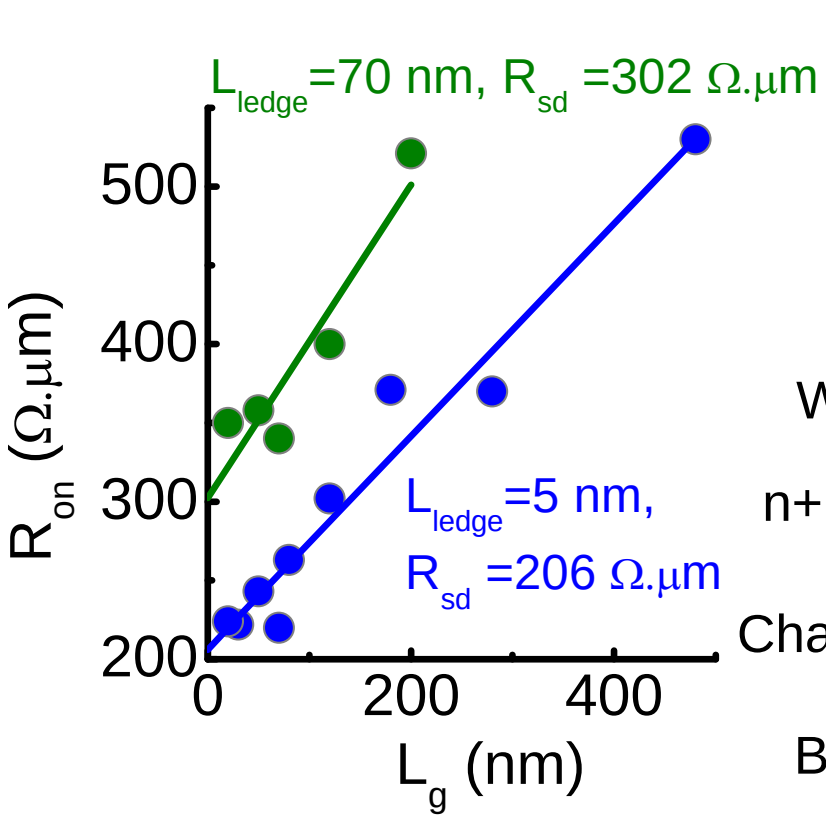
L_g= 20 nm InAs QW-MOSFET with L_{ledge}= 5 nm

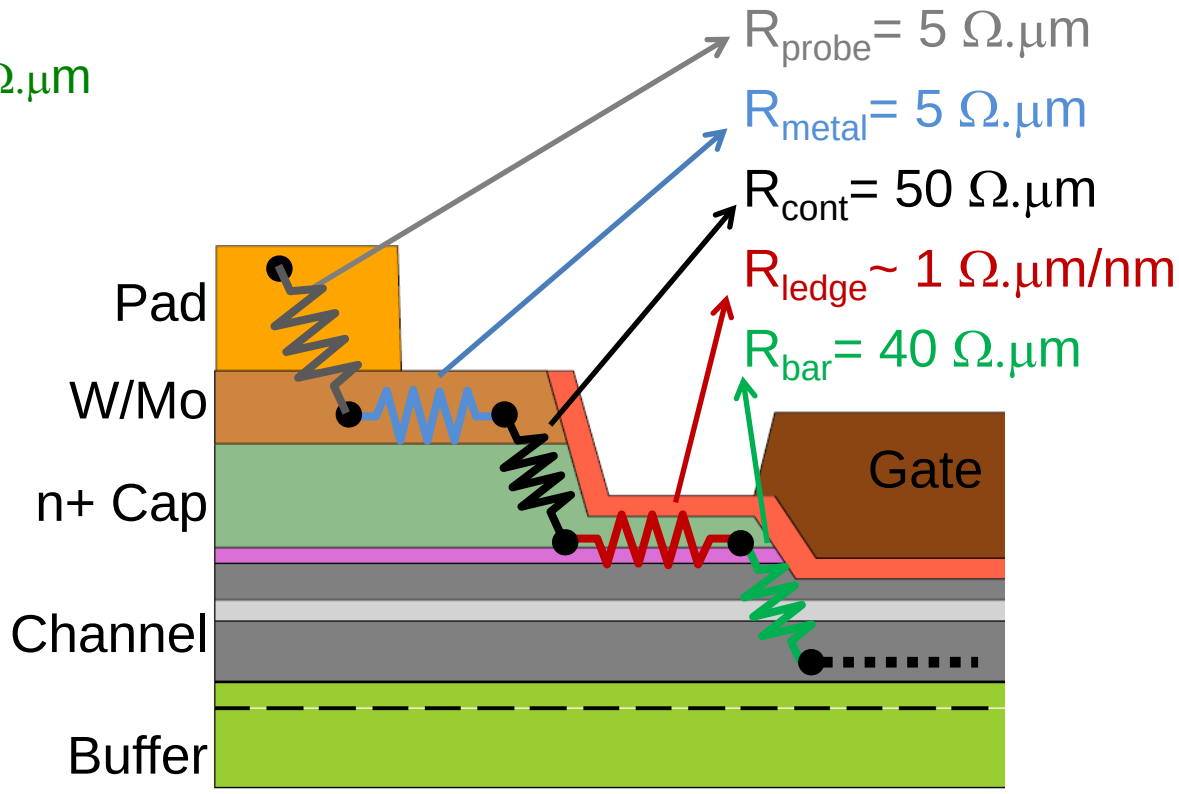




- Smallest functional III-V MOSFET with tight contact spacing

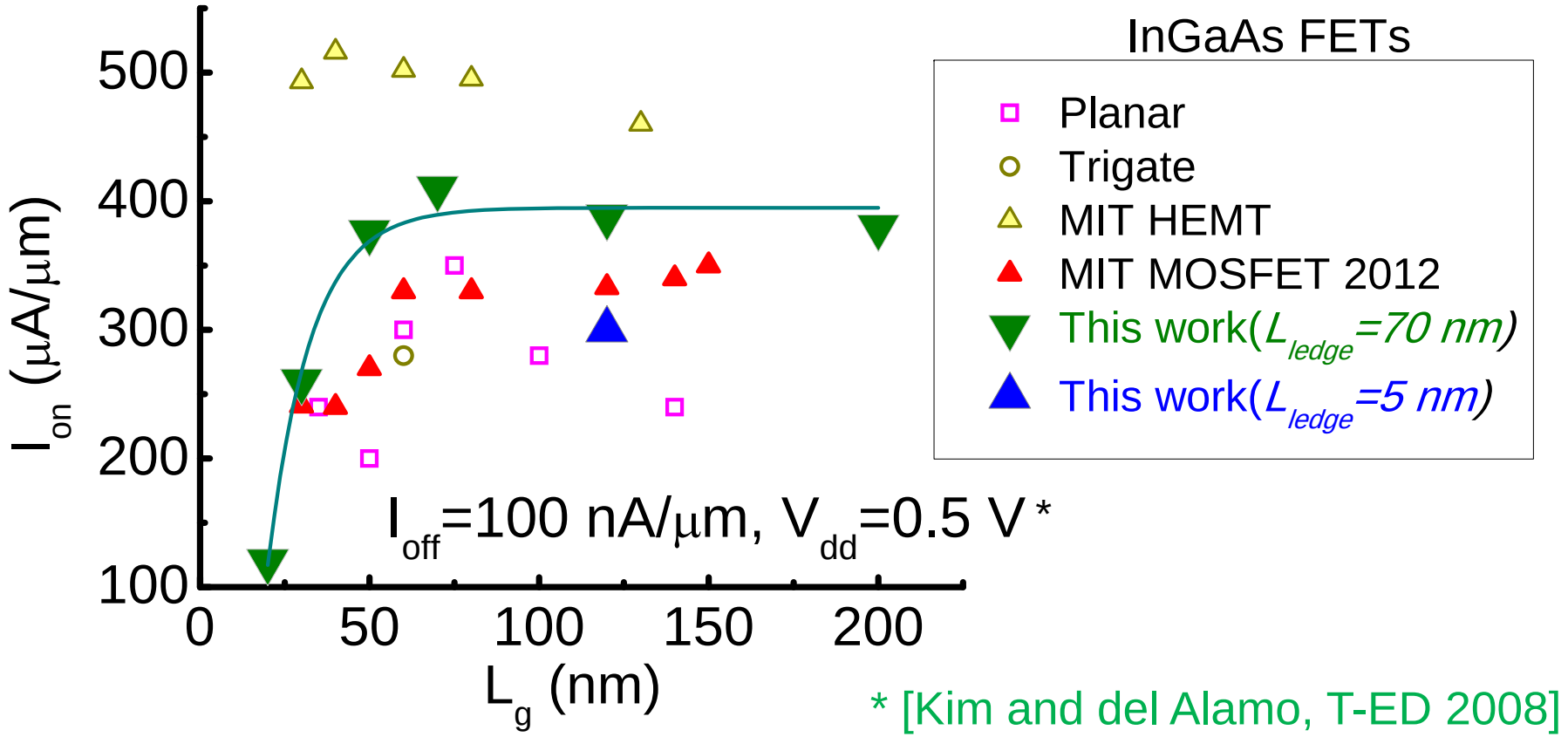
Parasitic resistance analysis





- For short ledge devices, major R_{sd} contribution from R_{cont} and R_{bar}

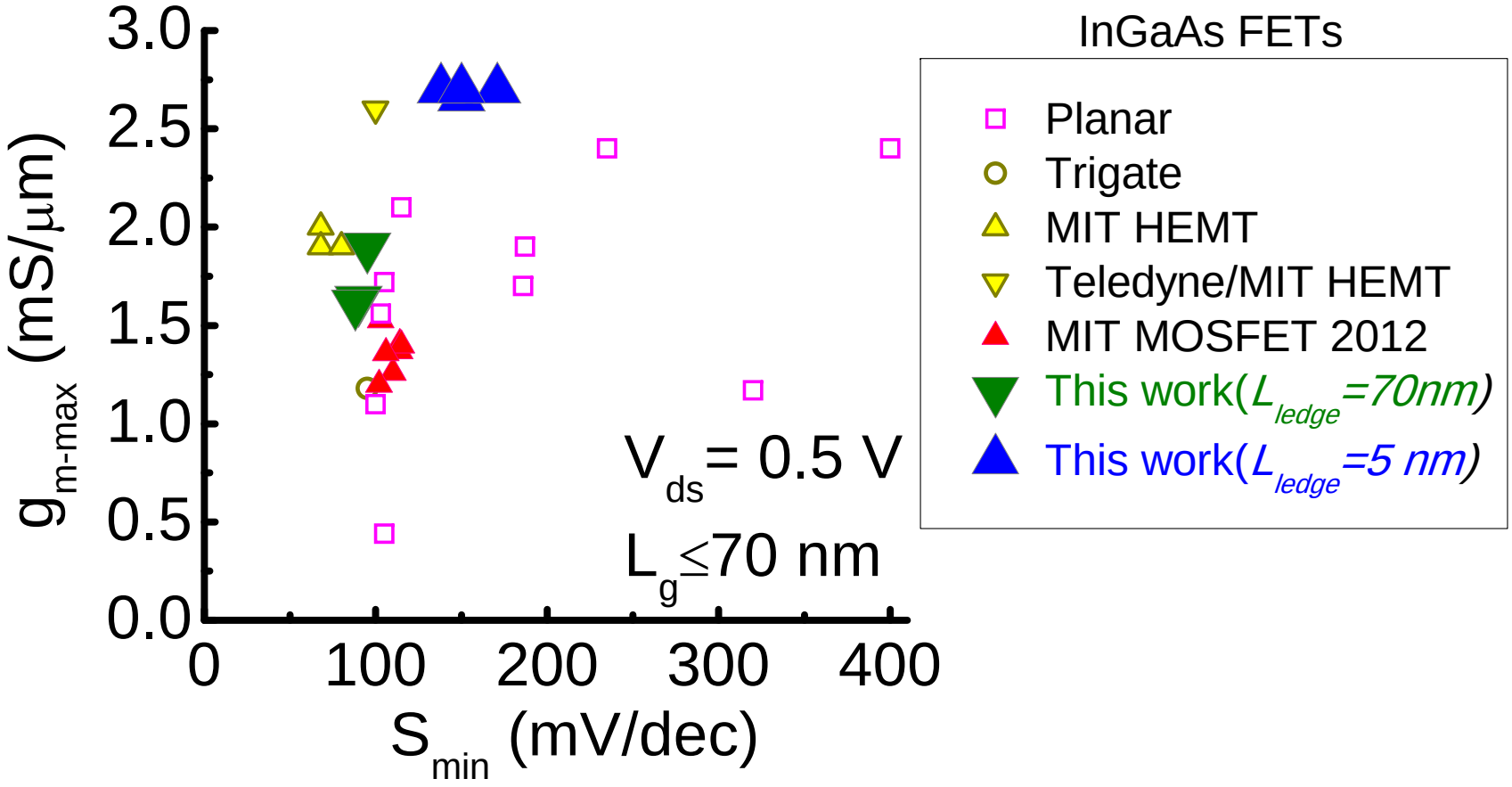
Benchmark: I_{on}



* [Kim and del Alamo, T-ED 2008]

- Record I_{on} = 410 μA/μm at L_g=70 nm for L_{ledge}=70 nm

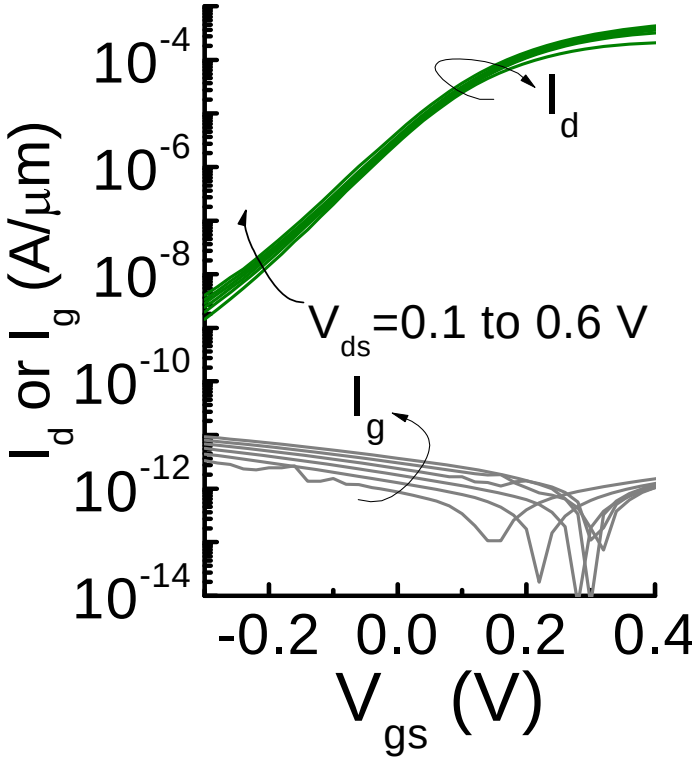
Benchmark: $g_{m,max}$ *vs.* S



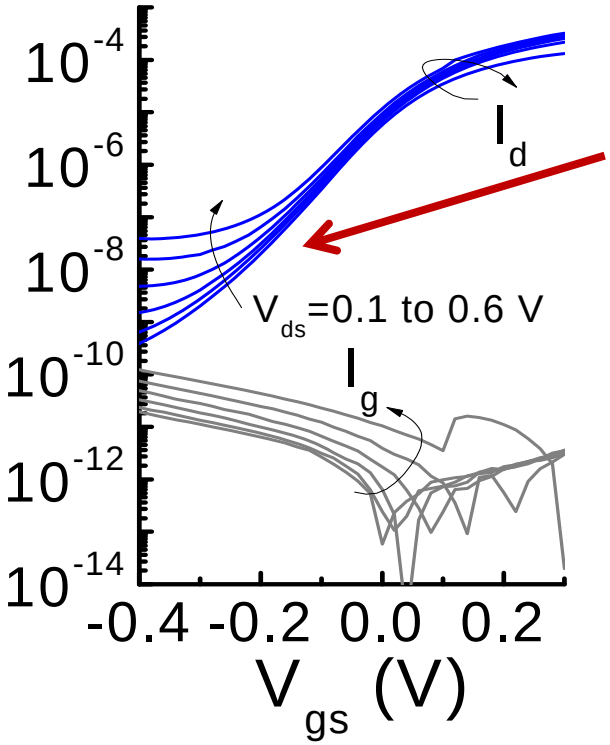
- Short ledge MOSFETs show record $g_{m,max}$
- Long ledge MOSFETs match record S
  [Radosavljevic, IEDM 2011]

Impact of ledge on off-state leakage (Long MOSFETs)

L_g= 200 nm, L_{ledge} = 70 nm



L_g= 500 nm, L_{ledge} = 5 nm

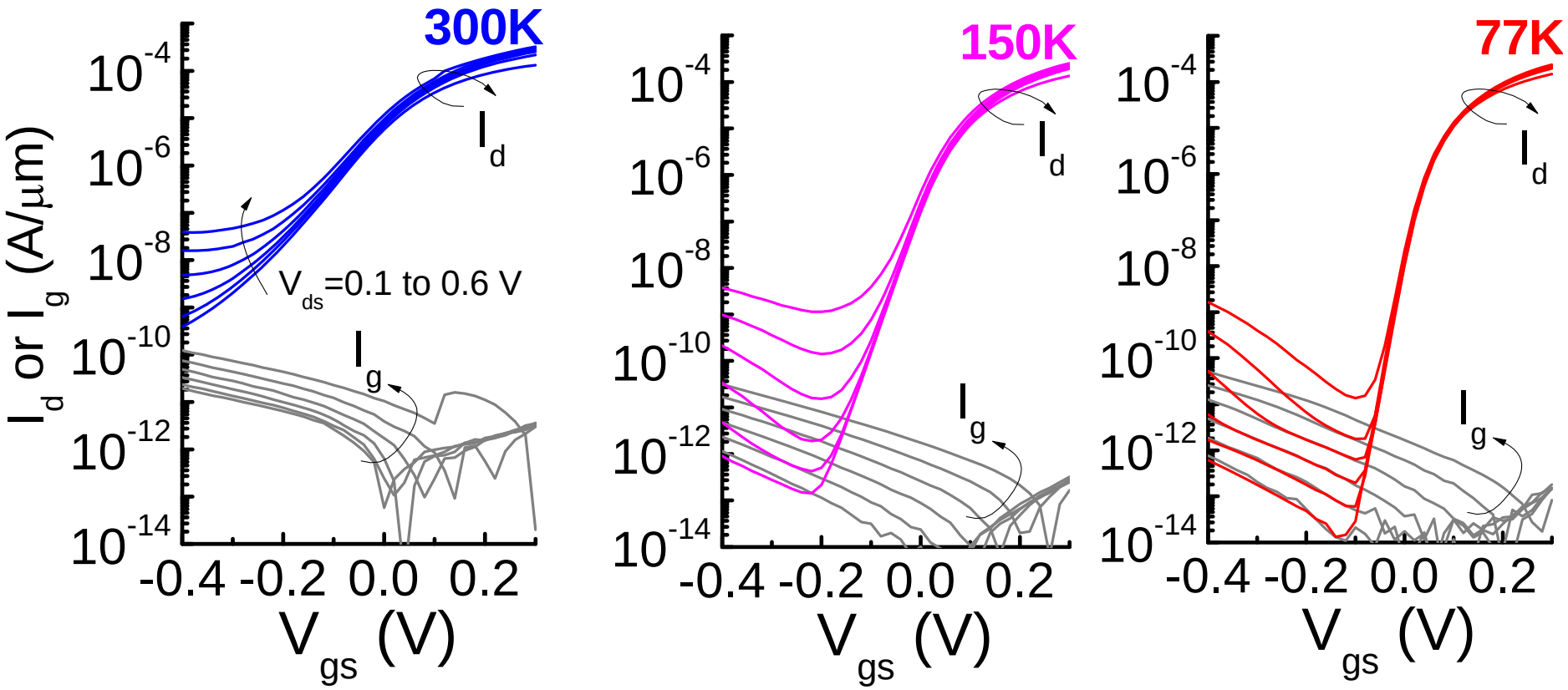


Flattening tail at high V_{ds}

- Short ledge leads to high I_{off}
- Strong V_{ds} dependence

Off-state leakage: Temperature dependence

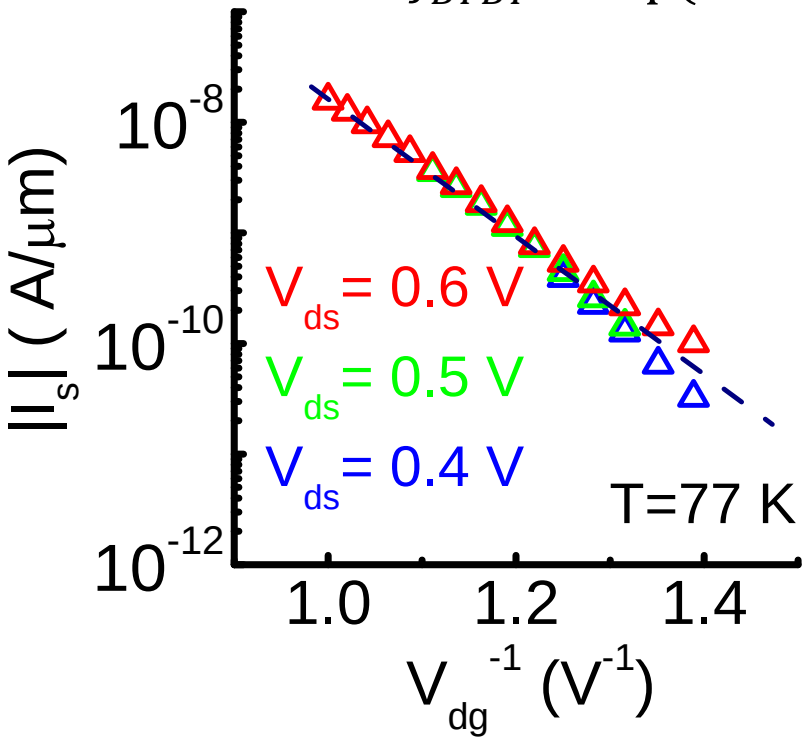
L_g= 500 nm, L_{ledge} = 5 nm

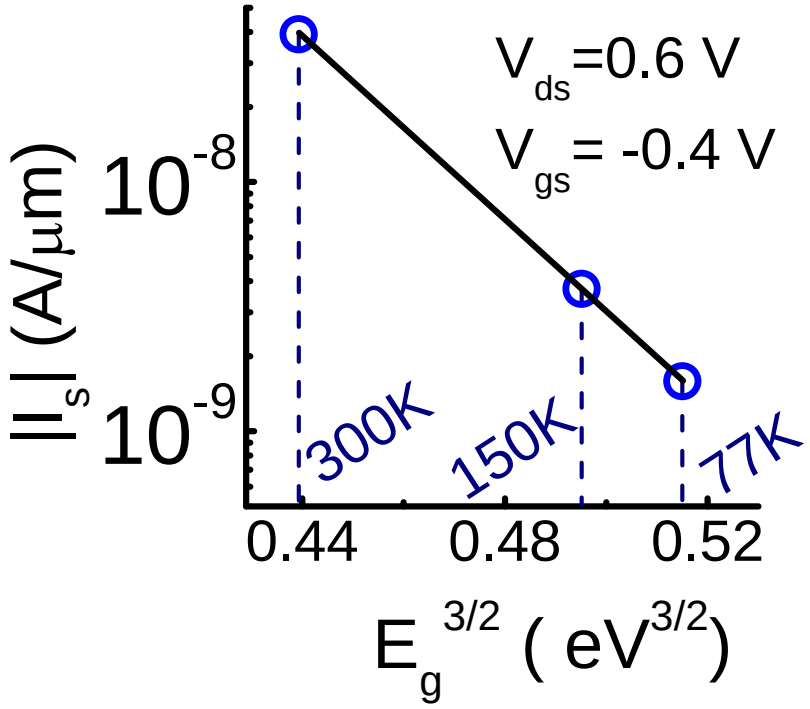


- GIDL (gate-induced drain leakage) signature

Off-state leakage follows BTBT signature

$$J_{BTBT} \sim \exp\left(-A\frac{\sqrt{E_g{}^3}}{V_{dg}}\right)$$

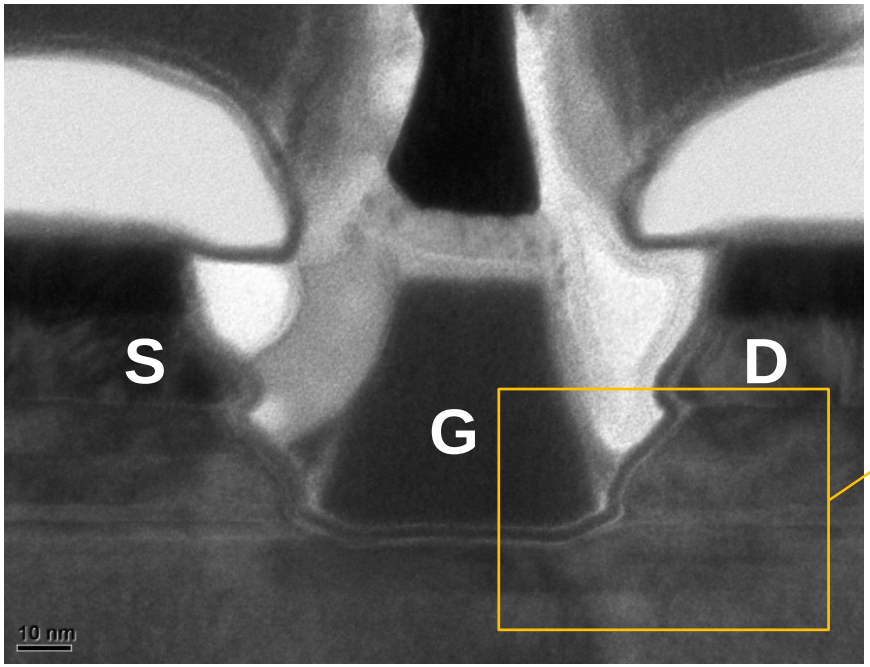


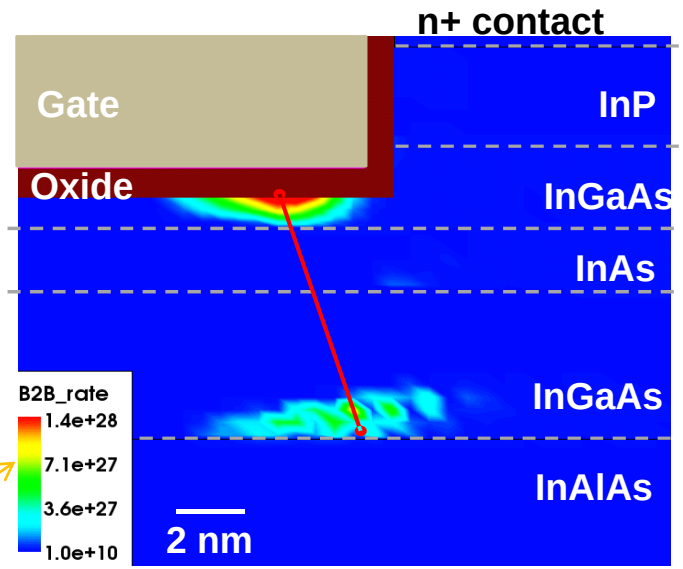


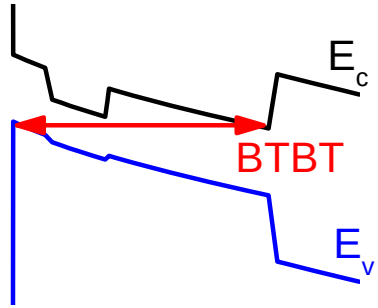
- I_s follows BTBT dependence on V_{dg} and E_g

GIDL simulations

TCAD simulation of BTBT rate based on nonlocal path BTBT model:







Conclusions

- Novel self-aligned III-V QW-MOSFETs:
  - Lift-off free, wet-etch free, and Au free in front end process
  - Design and fabrication of critical S/D ledge
  - Tight metal contact spacing
  - Scaled channel thickness, barrier thickness and gate length
- Record results demonstrated:
  - $g_{m,max}$ = 2.7 mS/μm in L_{ledge} = 5 nm
  - I_{on} = 410 μA/μm in L_{ledge} = 70 nm
- Characteristic GIDL signature observed