Total current collapse in High-Voltage GaN MIS-HEMTs induced by Zener trapping

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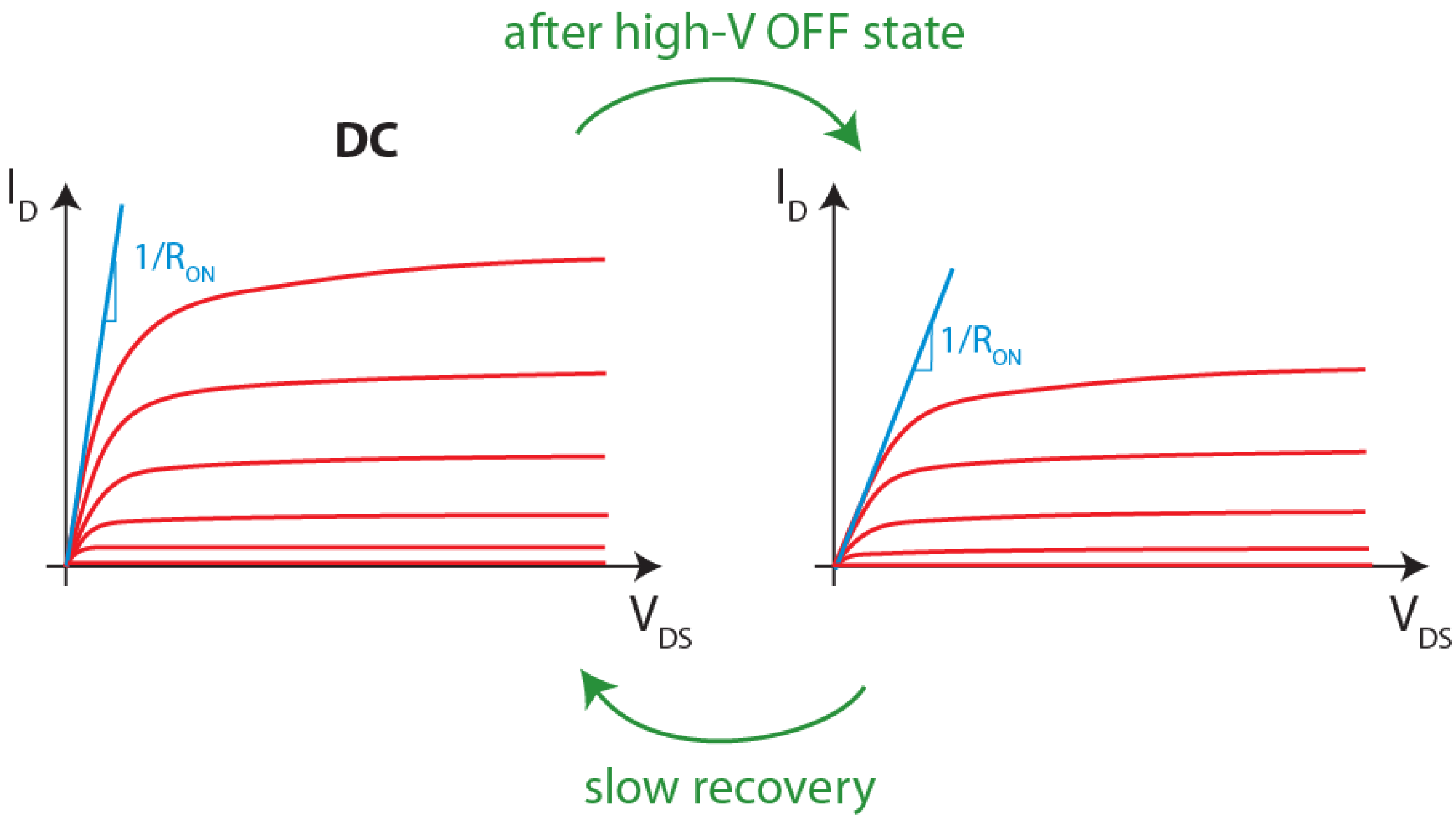
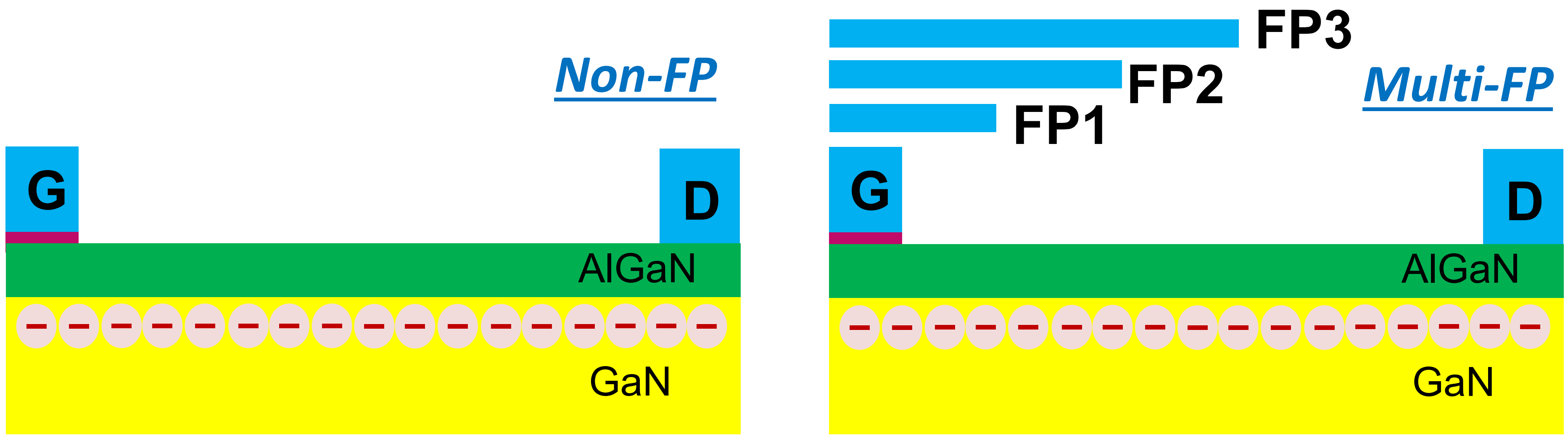
Current collapse or dynamic ON-resistance in GaN FETs



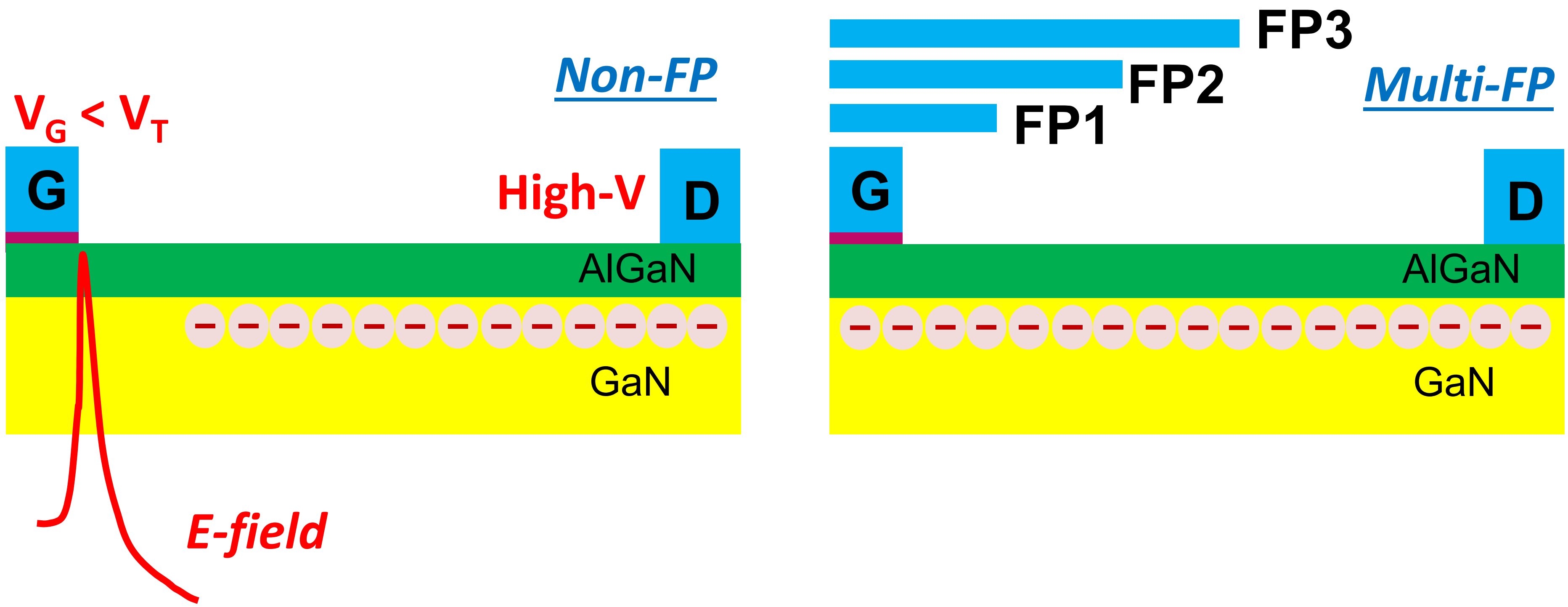
- R_{ON} depends on device history → After high V_{OFF}, R_{ON} ↑↑
- Big problem in power switching applications

Multi field-plate (FP) technology



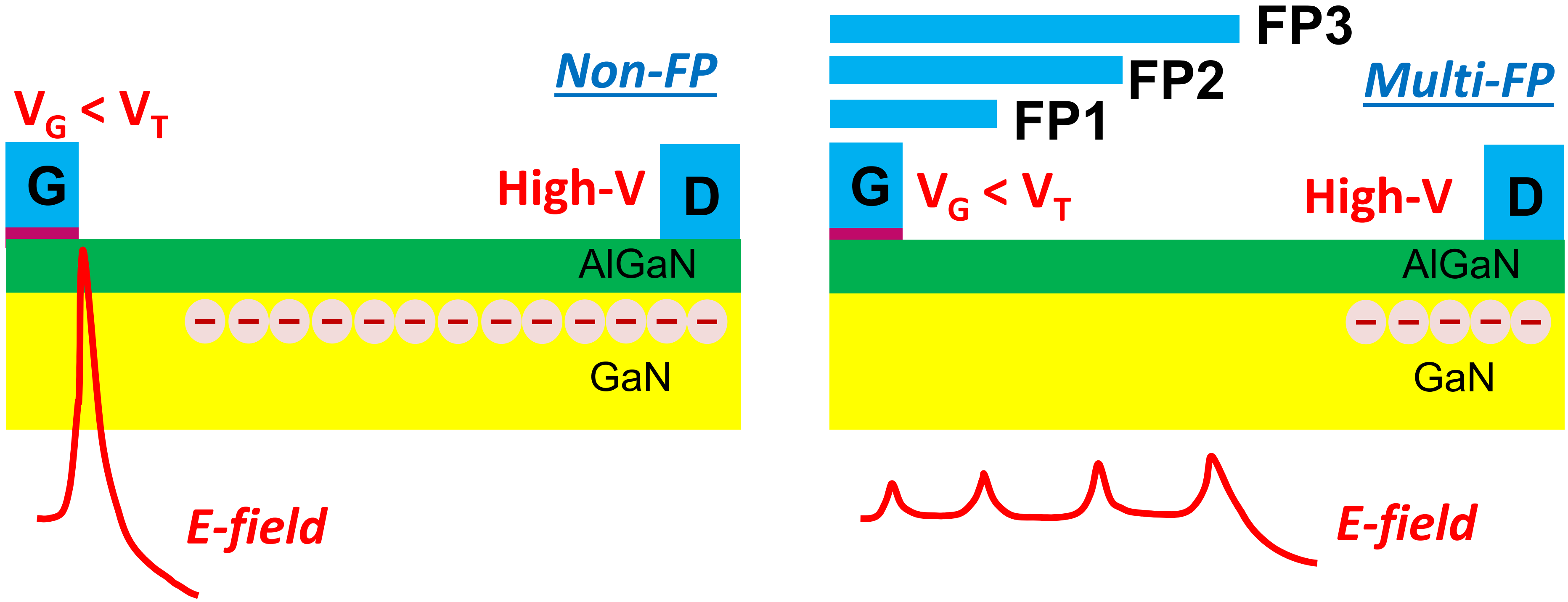
- **Key challenge for current collapse↓↓:**
  Engineering electric-field profile at high-V in the gate-to-drain gap of **GaN MIS-HEMTs** (Metal-Insulator-Semiconductor High-Electron-Mobility Transistors)
  → ***Multi field-plate technology developed***

Multi field-plate (FP) technology



- In high-V OFF-state,
  Non-FP → intense E-field peak → ***current collapse*** ↑↑

Multi field-plate (FP) technology



- In high-V OFF-state,

  Non-FP → intense E-field peak → ***current collapse* ↑↑**

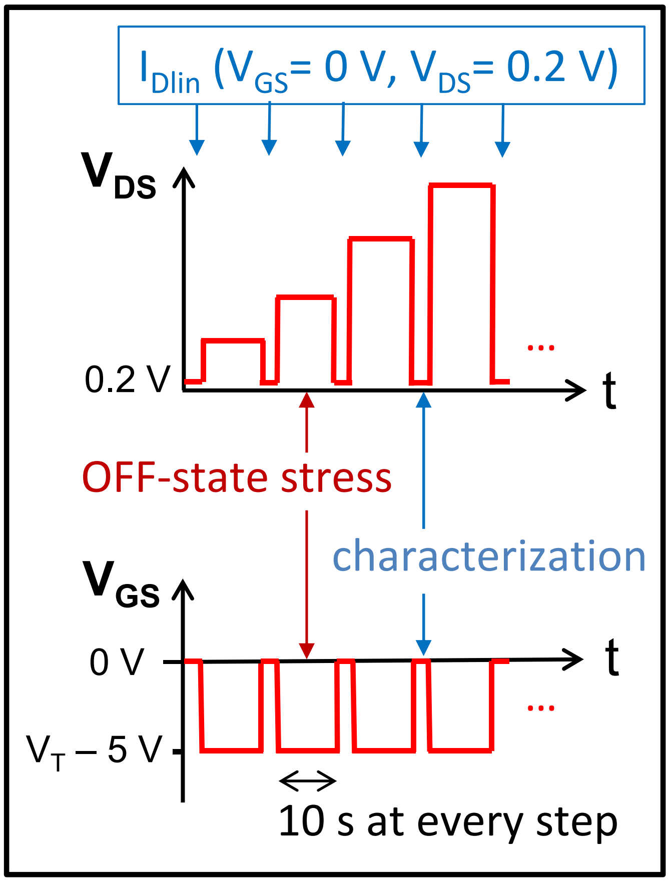
  Multi-FP → depletion region extension and E-field peak ↓↓

  → ***Effectiveness in current collapse?***

Current collapse at high V_{OFF}

GaN MIS-HEMTs with multi-FP (FP1,2,3):

- OFF-state step-stress with $V_{DS}\uparrow$
- Monitor I_{Dlin} (equivalent to R_{ON})



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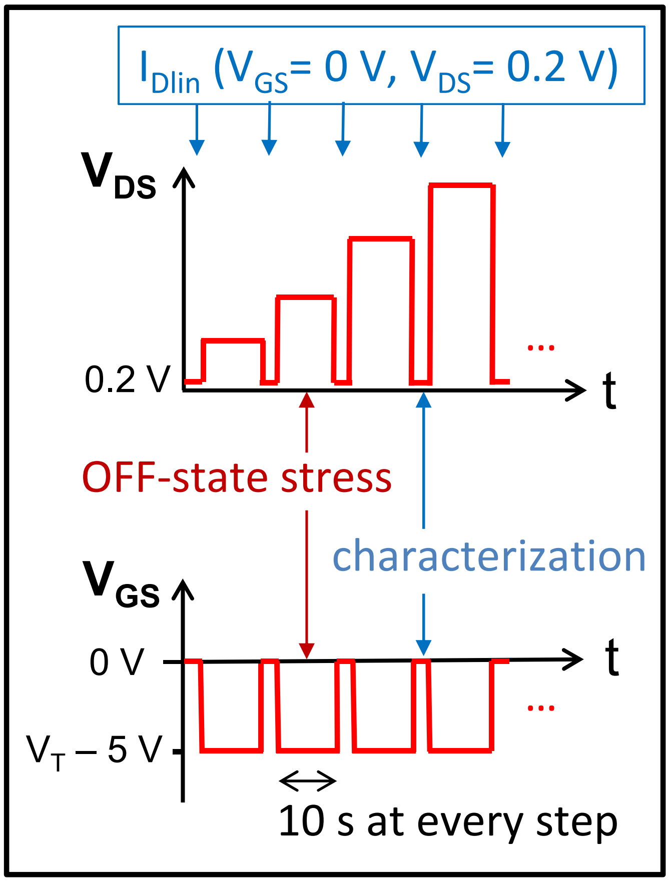
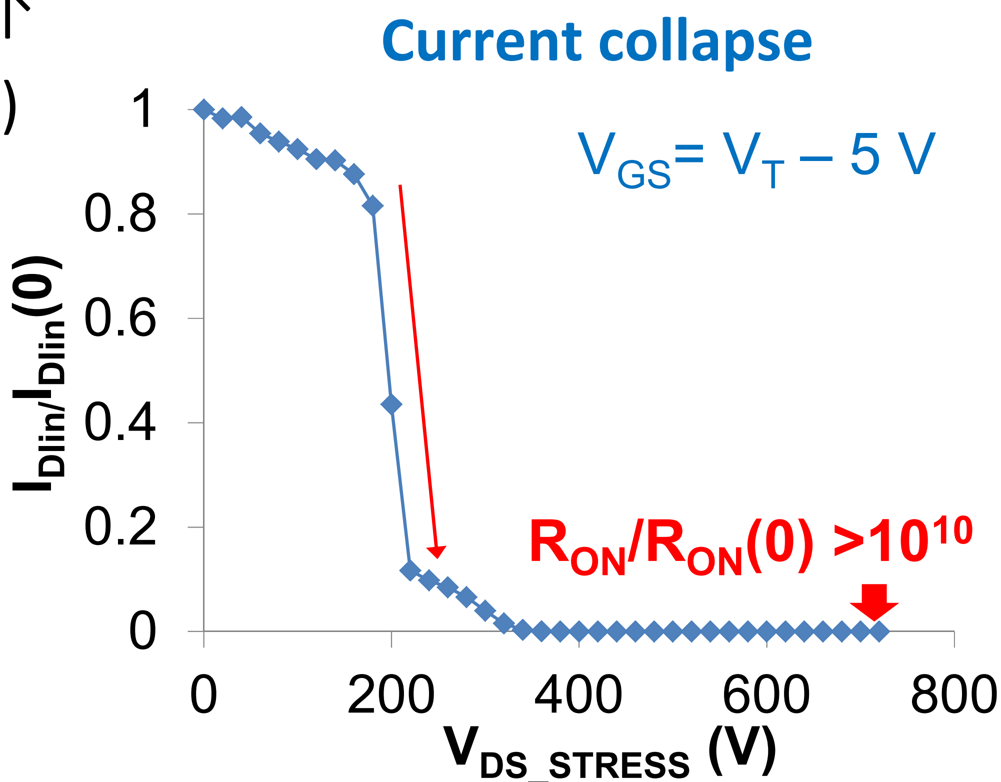
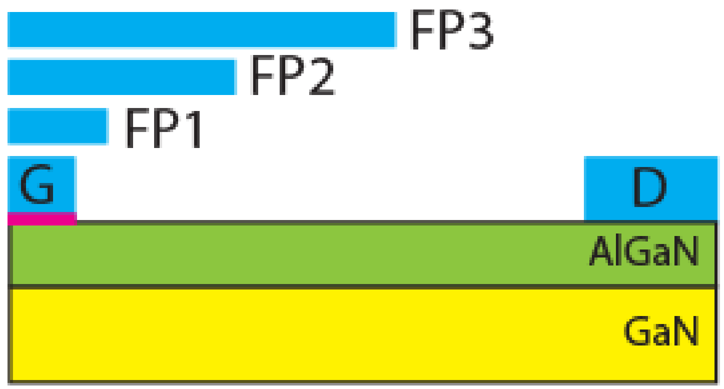




- ***Total current collapse*** for V_{DS} > 300 V
- **R_{ON} ↑↑ by > 10^{10}** by V_{DS}= 720 V

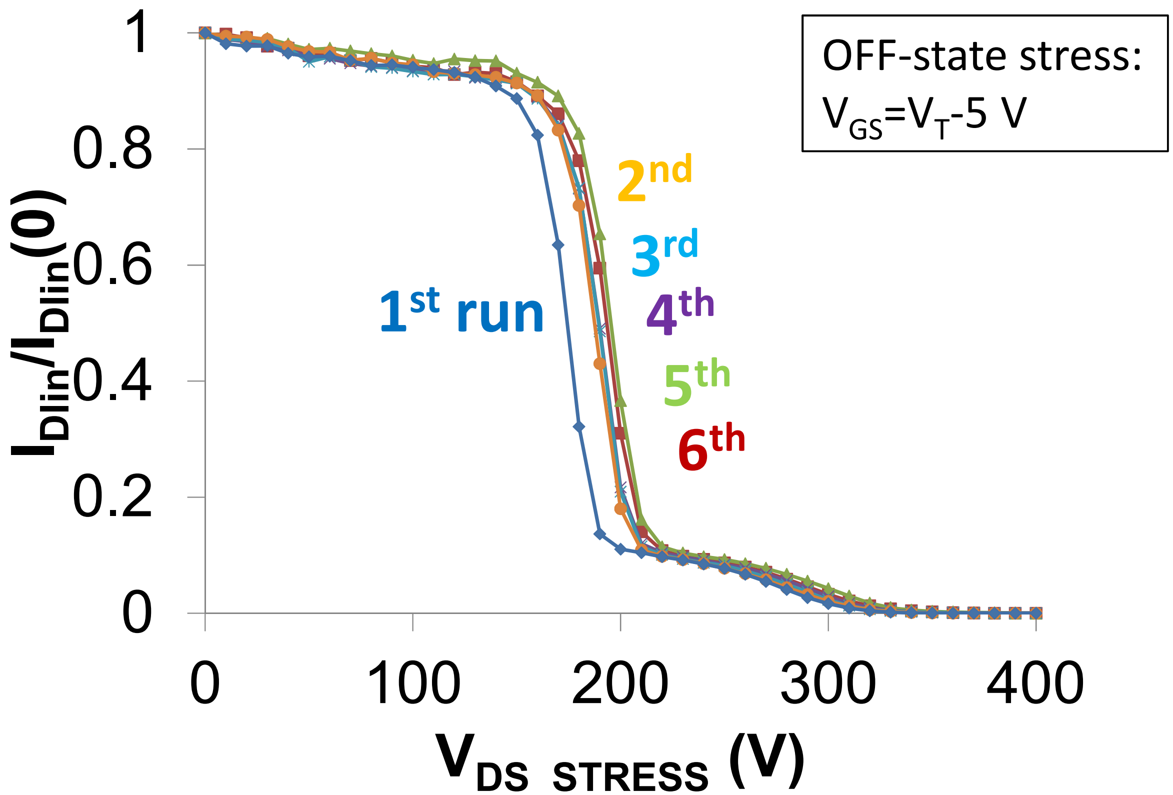
Questions to answer

- Is current collapse recoverable?
- Where in the device does this happen?
- What are the dynamics of this process?
- What is the mechanism responsible?
- How to mitigate/eliminate?



Current collapse recovery?

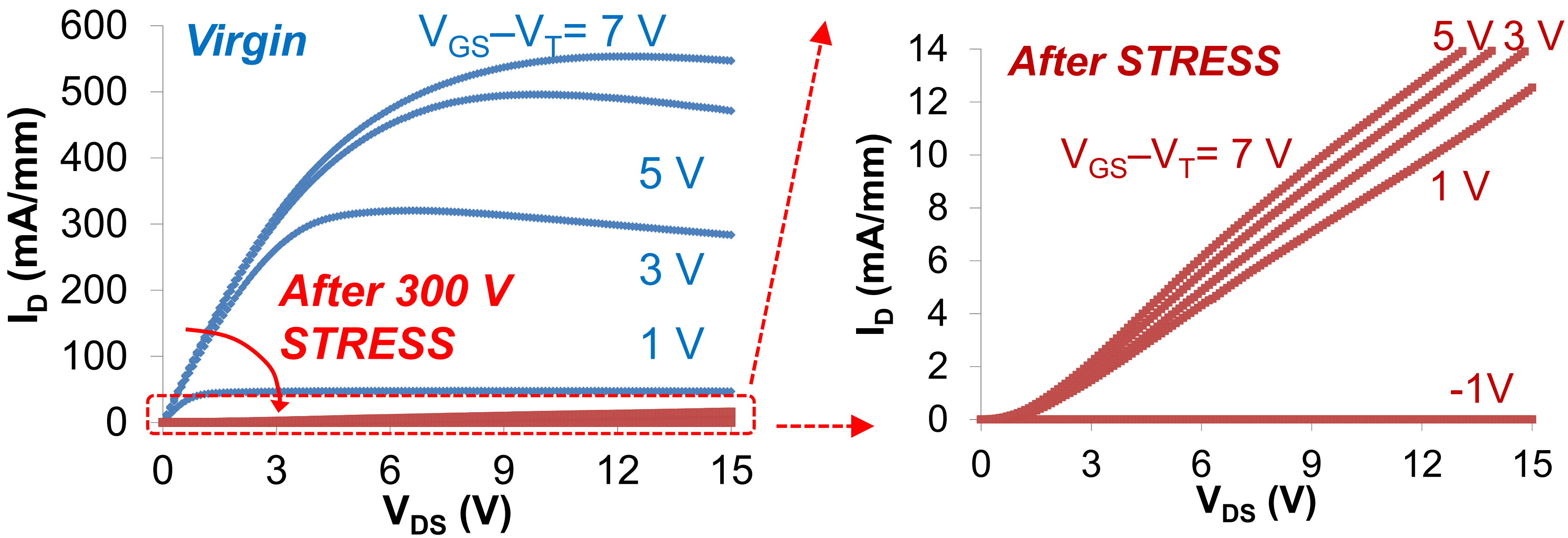
- 6 consecutive measurements
- UV exposure + thermal treatment (180 min at 200^{o}C) in between



Current collapse fully recoverable → **trapping!**

Lateral extent of current blockage?

Change in output characteristics after V_{DS}=300 V stress for 300 s:



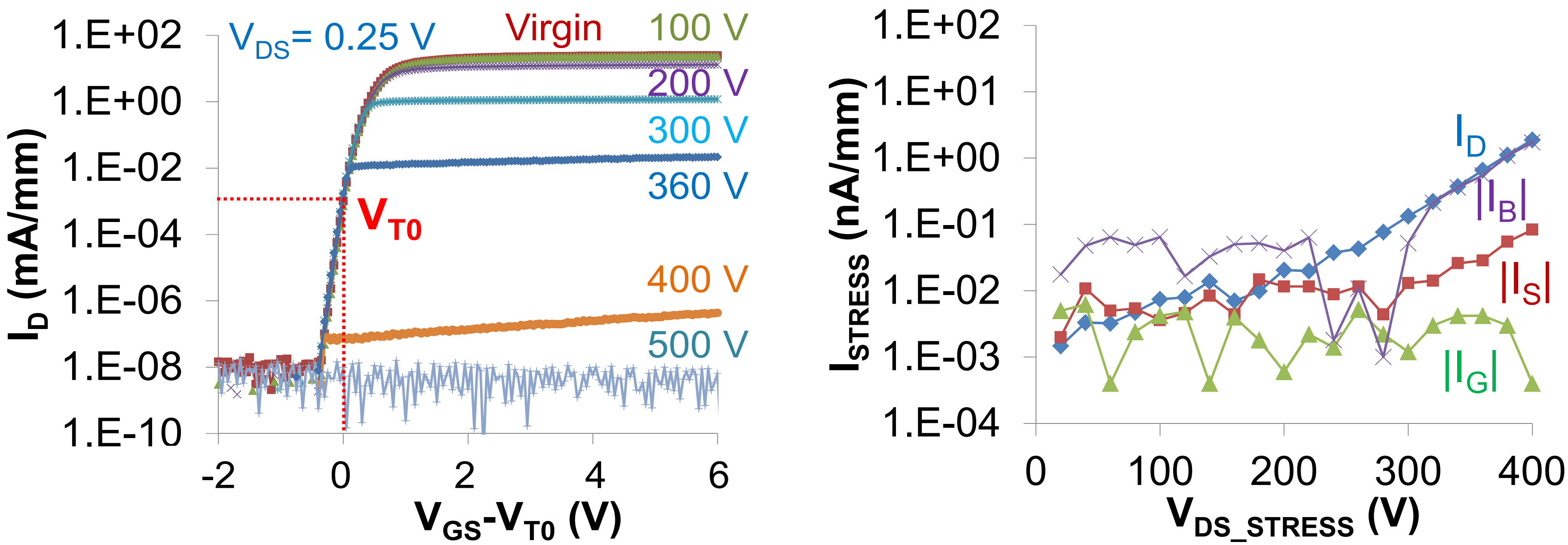
Current collapse for low V_{DS} but I_D flows again at high V_{DS}

→ punchthrough-like characteristics

→ current blockage is short along channel direction

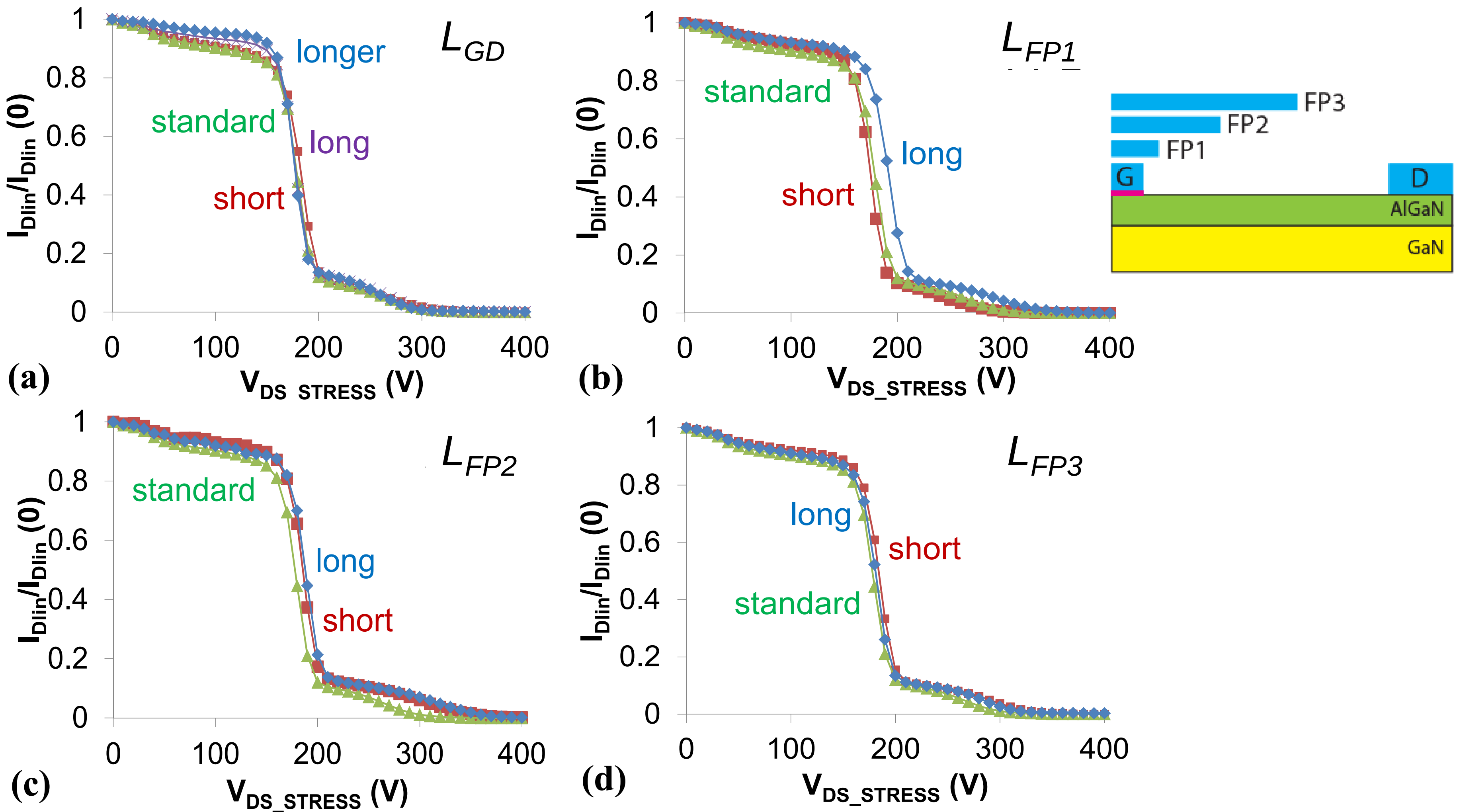
Change in V_T and terminal currents?

Evolution of subthreshold characteristics and 4 terminal currents:



- No change in V_T → current blockage in extrinsic device region
- At the onset of severe trapping, all currents are negligible

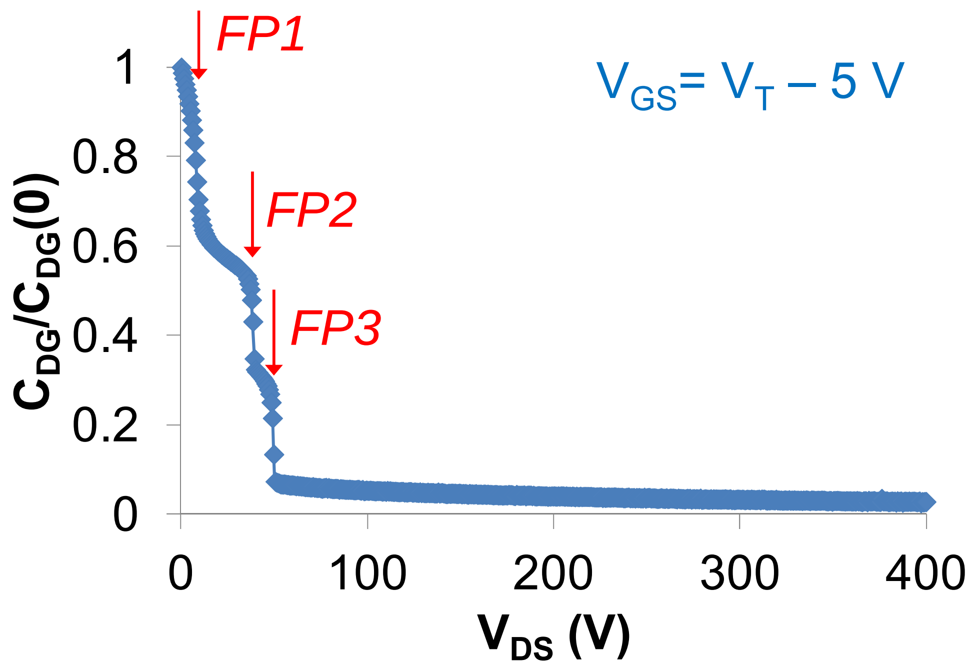
Impact of device geometry?

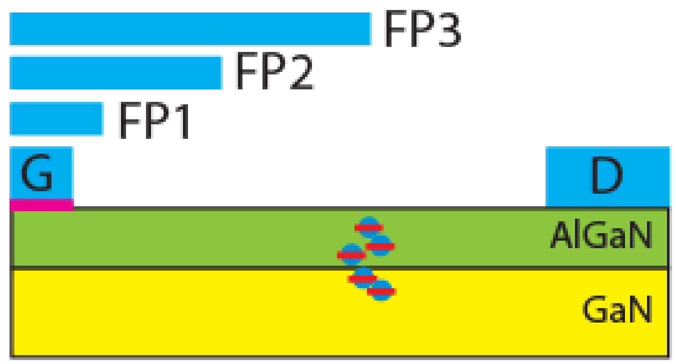


Current collapse independent of L_{GD} and geometry of field-plates

Current blockage location?

Capacitance-voltage characteristics of virgin device:





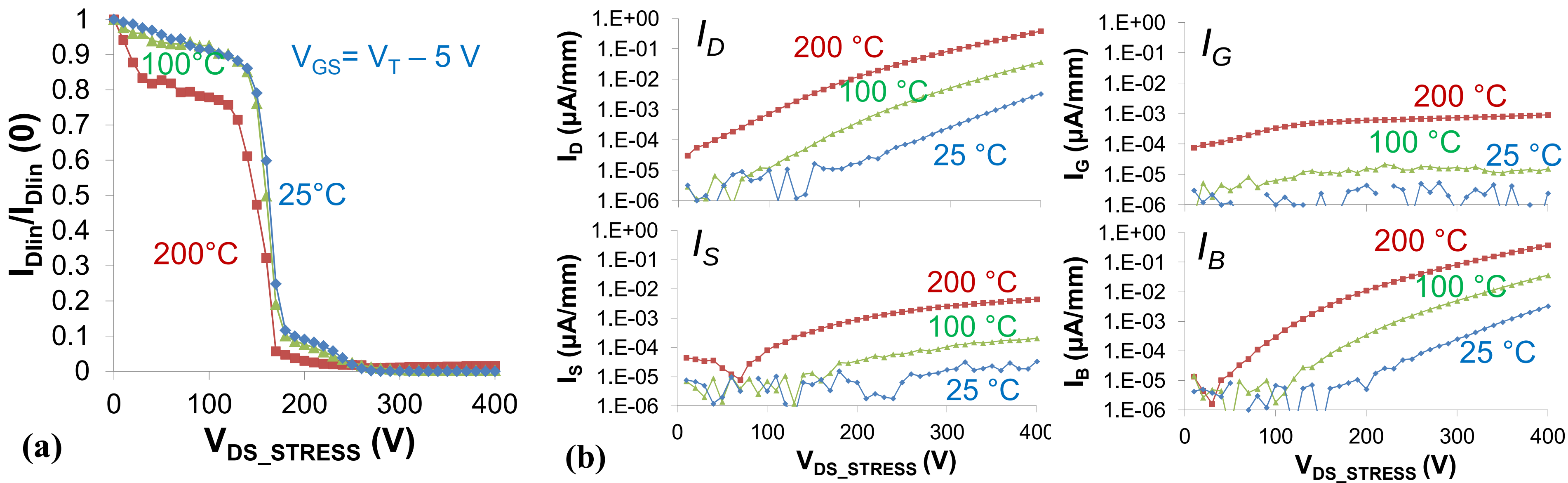
Channel under field plates fully depleted by V_{DS}=50 V

→ For V_{DS}>50 V, electric field peaks in channel under edge of FP3

→ Current blockage under edge of FP3

Role of temperature?

OFF-state step-stress at different T:

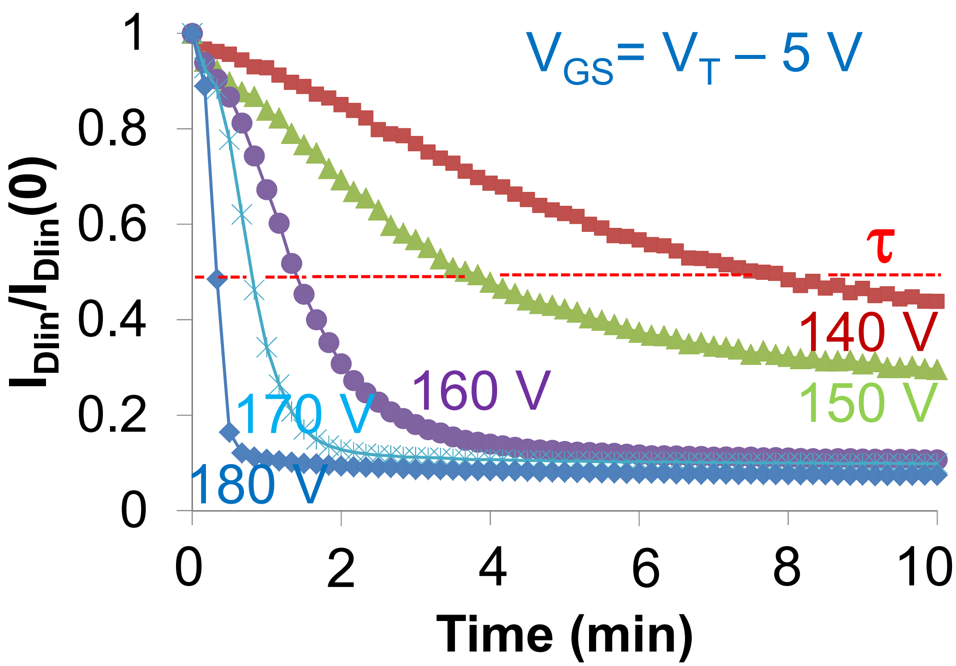


- Terminal currents ↑↑ as T↑ → <u>Not source of trapping</u>
- Total current collapse independent of T

  → <u>Trapping through **tunneling process**</u>

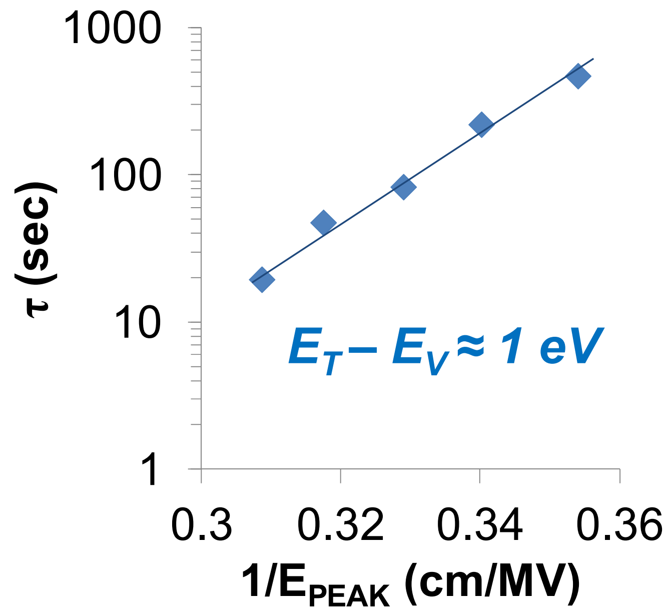
Dynamics of trapping

Evolution of I_{Dlin} during trapping process:



Zener tunneling law:

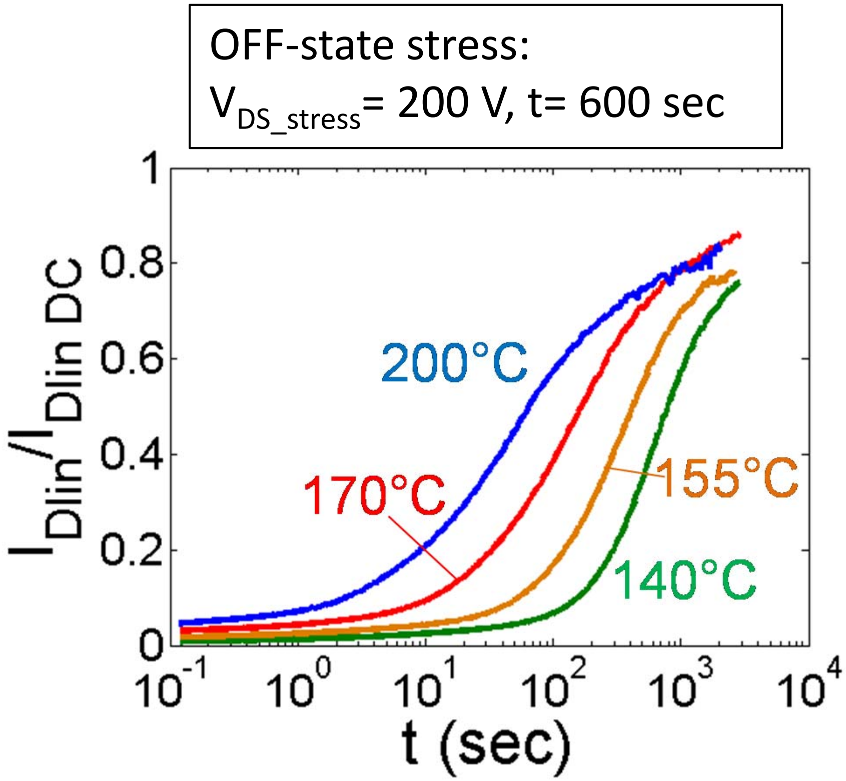
$$\ln(\tau) = A\frac{(E_T - E_V)^{3/2}}{E_{PEAK}} + B$$

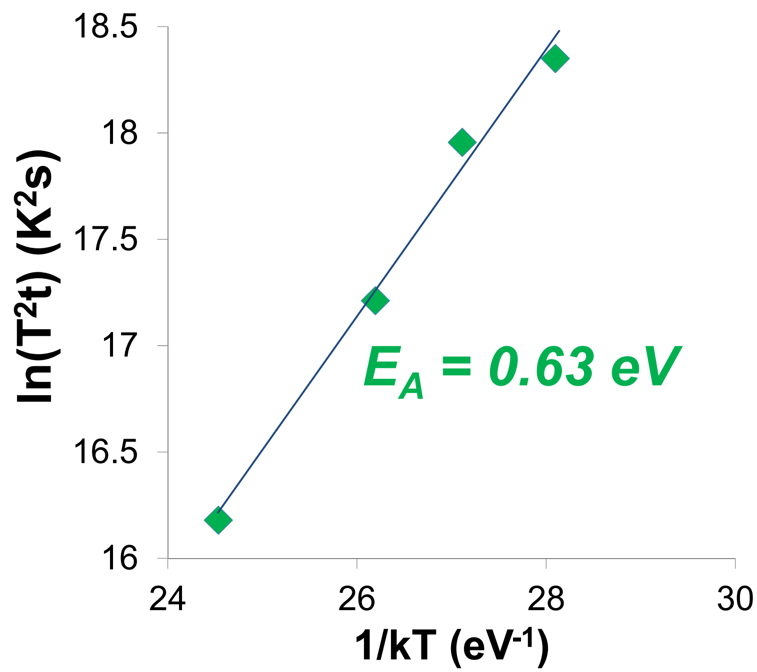


- Trapping accelerated as V_{DS_stress}↑
- Characteristic trapping time exhibits Zener-like dependence on peak electric field under FP3 edge (from simulations)

Dynamics of thermal detrapping

Evolution of I_{Dlin} during detrapping at different temperatures:



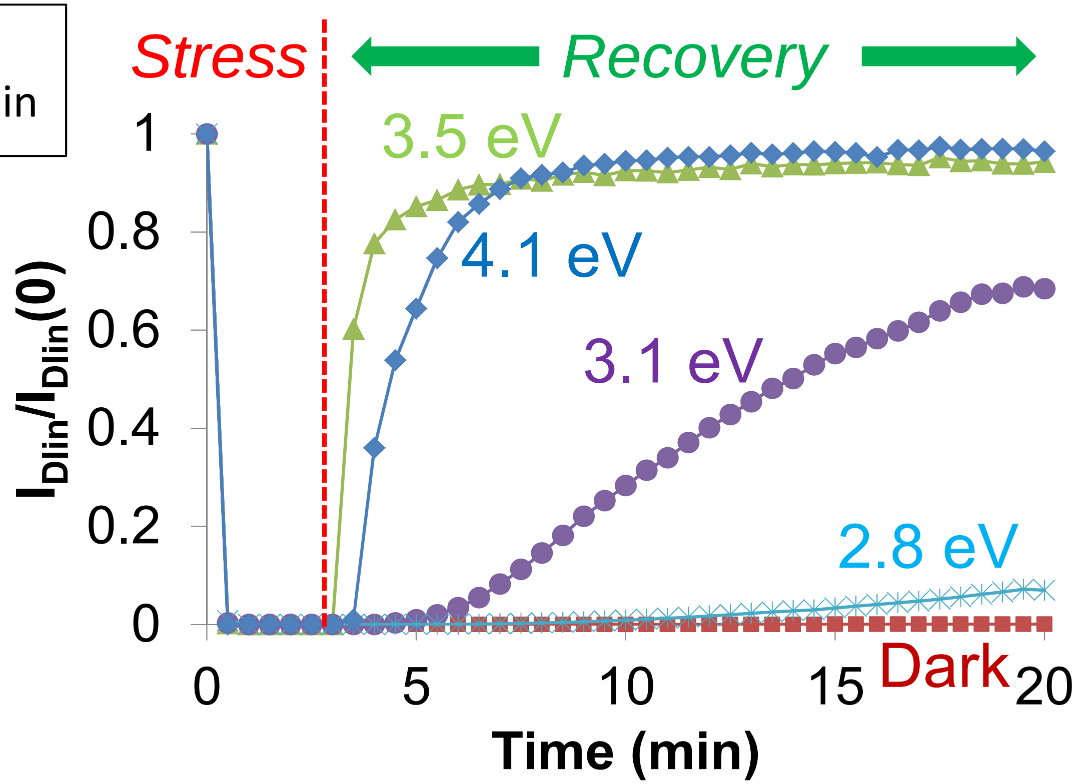


- Detrapping accelerated as T↑
- Activation energy: E_A= 0.63 eV

Dynamics of UV-enhanced detrapping

Evolution of I_{Dlin} during detrapping under UV exposure (300K):

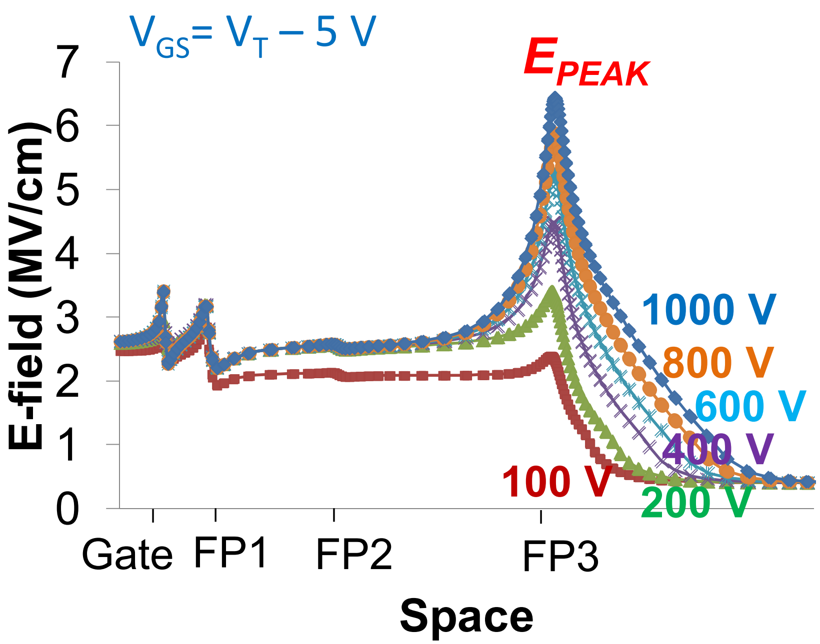
OFF-state stress:
V_{DS_stress}=300 V, t=3 min

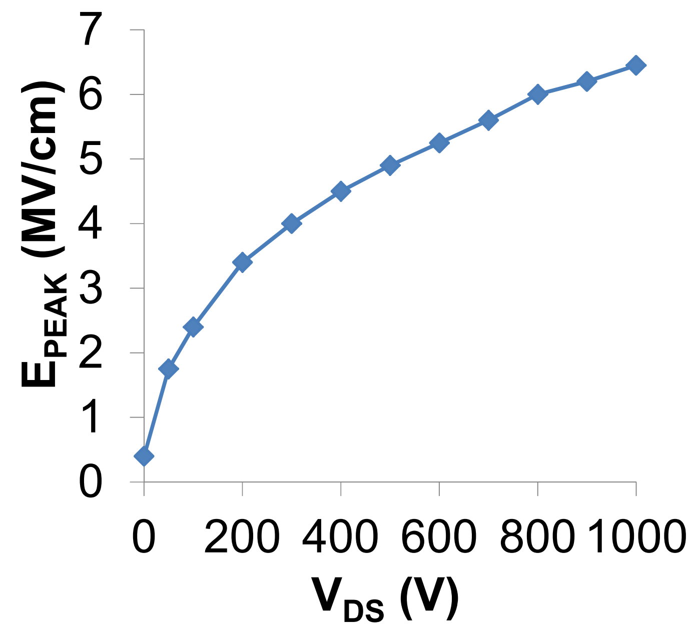


Detrapping accelerated by UV with $E_{h\nu}$> 2.8 eV

Electric field simulations

Silvaco simulations of electric field at top surface of AlGaN barrier from gate to drain:





- In OFF-state for V_{DS}> 100 V, field peaks under edge of FP3
- E_{PEAK} increases with V_{DS}
- At V_{DS}=200 V, E_{PEAK}= 3.4 MV/cm

Summary of key findings

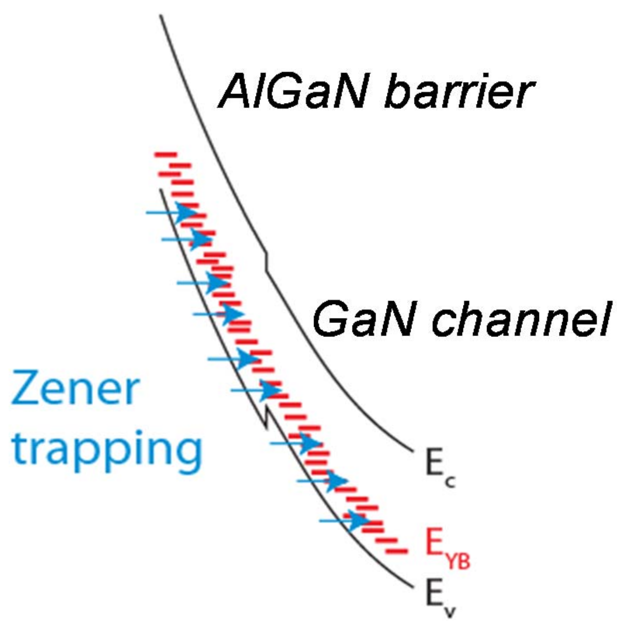
- Total current collapse after high V_{OFF} bias:
  - Fully recoverable
  - Triggered and accelerated by electric field
  - Follows Zener-like dependence with $E_T – E_V = 1.0$ eV
  - Trapped region very short and located under FP3 edge
  - No effect from variations of L_{GD} and FPs lengths
  - Temperature independent trapping process
  - Detrapping enhanced by UV with $E_{h\nu} > 2.8$ eV
  - Detrapping enhanced by temperature with $E_A = 0.63$ eV

Mechanism for total current collapse

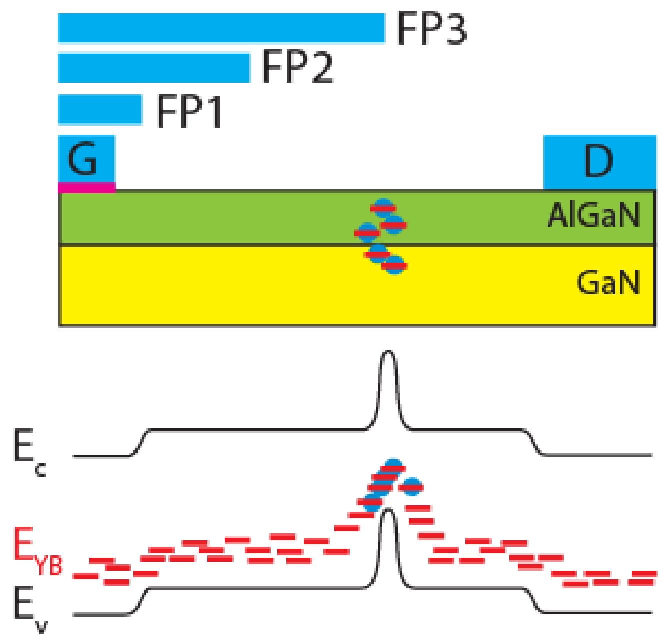
Observations consistent with:

- Field-induced trapping process → **Zener trapping**
- Takes place in narrow region under edge of FP3
- Electrons from valence band tunnel to traps
- Trapped electrons lift bands in ON state and create blockage

At high-V_{OFF}

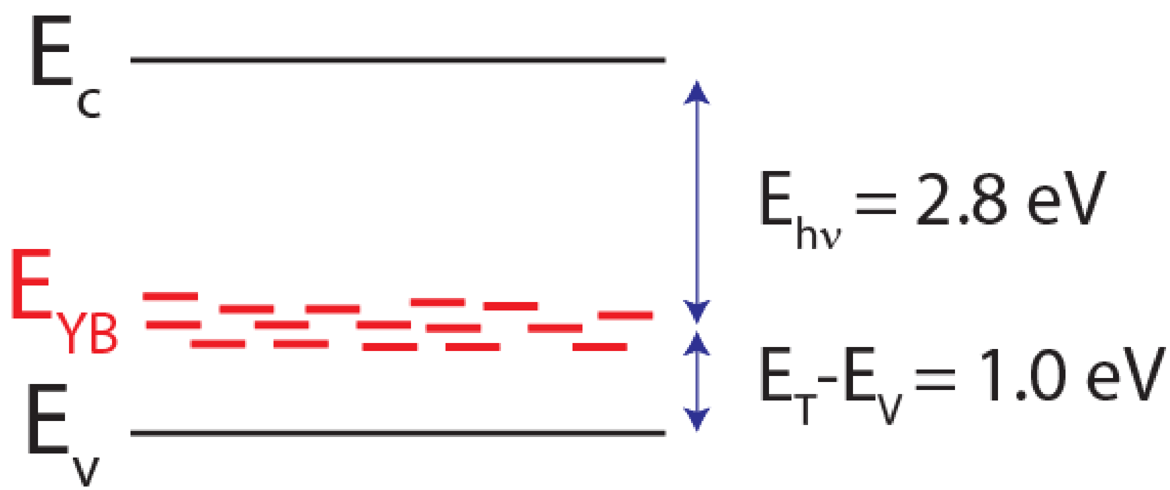


After high-V_{OFF}



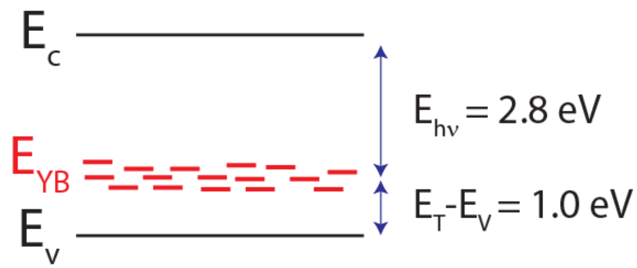
Energy location of traps?

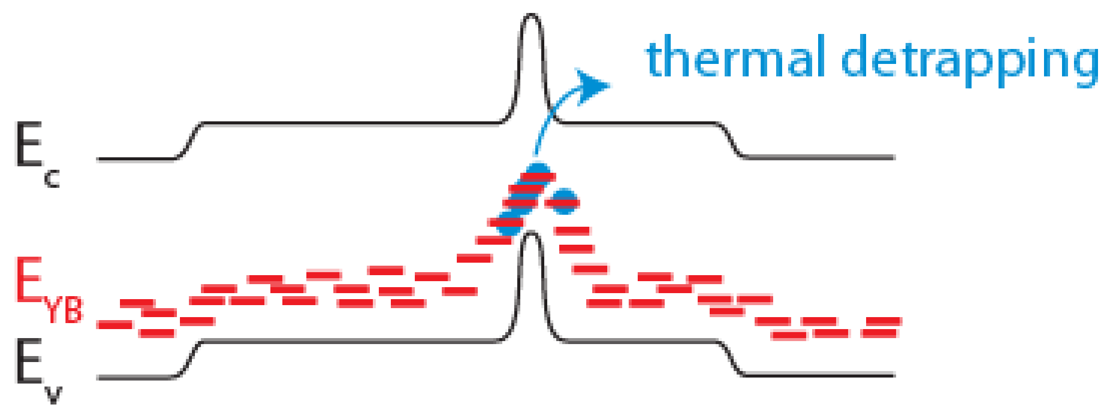
- From Zener trapping calculations: E_T-$E_V \approx 1.0$ eV
- From UV detrapping experiments: $E_{h\nu} \approx 2.8$ eV
- For reference: E_g(GaN) = 3.4 eV, E_g ($Al_{0.2}Ga_{0.8}N$) = 3.8 eV



Thermal detrapping with E_A=0.63 eV?

Thermal detrapping E_a=0.63 eV seems inconsistent with energy picture…

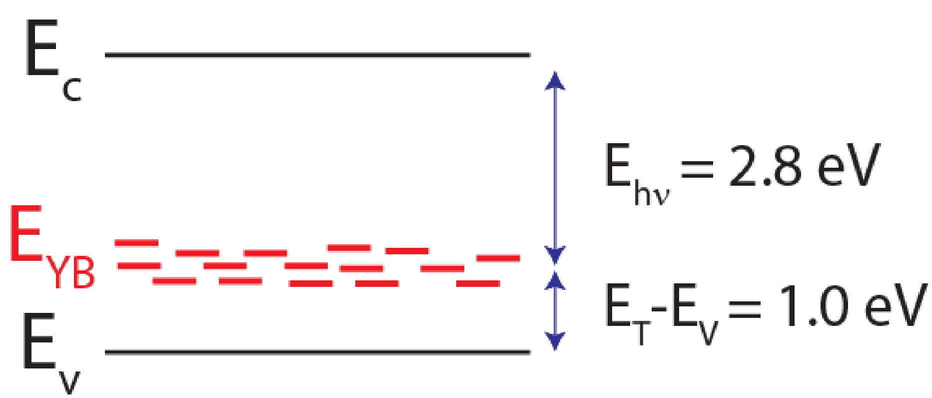




If blockage region is short, thermal detrapping possible with $E < E_C$-E_T

Physical origin of traps?

- Trap energy consistent with traps responsible for yellow luminescence in AlGaN and GaN.
- In GaN: E_C-E_{YB} = 2.5 eV (Calleja, PRB 1997)
- In $Al_{0.2}Ga_{0.8}N$: E_C-E_{YB} = 2.8 eV (Hang, JAP 2001)
- Yellow luminescence traps attributed to C in N site (Lyons, APL 2010)



Mitigation: carefully manage C doping in buffer and migration to AlGaN barrier

Conclusions

- Total current collapse in high-voltage GaN MIS-HEMTs
  - Current collapse is recoverable
  - Attributed to Zener trapping in AlGaN barrier or GaN channel under edge of outermost field plate
  - Traps are consistent with those responsible for yellow luminescence in GaN and AlGaN
  - Main suspect: C

- Attention to defect control during epitaxial growth and appropriate design of multi field-plate structures