# Total current collapse in High-Voltage GaN MIS-HEMTs induced by Zener trapping

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## Abstract

We investigate current collapse in GaN MIS-HEMTs for >600 V operation. Extreme trapping leading to total current collapse has been observed after OFF-state stress at high voltage. We attribute this to high-field tunneling-induced electron trapping ("Zener trapping") inside the AlGaN barrier or the GaN channel layers. The trapping takes place in a narrow region right under the edge of the outermost field plate in the drain portion of the device. The trapping characteristics are consistent with those responsible for the yellow luminescence band in GaN or AlGaN. This finding gives urgency to defect control during epitaxial-growth and the design of appropriate field plate structures for the reliable high-voltage operation of MIS-HEMTs.

## Introduction

GaN Metal-Insulator-Semiconductor High-Electron-Mobility Transistors (MIS-HEMTs) fabricated on large-diameter Si substrates have emerged as promising candidates for high-voltage power management applications. A great concern with these devices is current collapse or dynamic ON-resistance ($R_{ON}$) phenomenon [1]. This is the temporary increase in $R_{ON}$ after high-voltage OFF-state biasing that arises from excessive trapping. To mitigate this problem and enhance the voltage handling ability of these devices, multi field-plate structures are used [2]. Their effectiveness to prevent current collapse is unclear, particularly at high voltage [3].

In this work, we have investigated current collapse in GaN MIS-HEMTs designed for > 600 V operation. In the OFF-state, when $V_{DS}$ exceeds around 200 V, we observe trapping that is so severe that leads to total current collapse and the device effectively behaves as an "open" when subsequently biased in the ON state. This phenomenon is fully recoverable and repeatable. The impact of device geometry and temperature on this anomaly has been investigated and the responsible activation energies for the trapping/detrapping dynamics have been extracted. All of our experimental results are consistent with electron trapping inside the AlGaN barrier or the GaN channel that takes place through a tunneling process under high-electric-field. We term this "Zener trapping".

## Total current collapse under OFF-state stress

The devices studied here are industrially prototyped AlGaN/GaN MIS-HEMTs fabricated on a 6-inch Si wafer. They feature three field plates placed in a stairway fashion along the gate-to-drain gap. The breakdown voltage is > 600 V and $R_{ON}$ and $I_{DMAX}$ are 10 Ω·mm and 550 mA/mm, respectively. To study the impact of high-V stress on $R_{ON}$, we perform OFF-state step-stress experiments. We gradually step $V_{DS\_STRESS}$ and periodically monitor the linear drain current ($I_{Dlin}$, defined at $V_{GS}$= 0 V, $V_{DS}$= 0.2 V) which is inversely proportional to $R_{ON}$. **Fig. 1** shows the evolution of normalized $I_{Dlin}$ in a typical experiment in which $V_{DS}$ increases by 20 V every 10 seconds up to 720 V. We find that up to $V_{DS\_STRESS}$= 200 V, $I_{Dlin}$ degrades slightly, about 10%. Around 200 V, $I_{Dlin}$ abruptly drops to around 10% of its initial value. For higher $V_{DS\_STRESS}$, $I_{Dlin}$ continues to degrade and eventually becomes negligible. Correspondingly, $R_{ON}$ increases by ~10 orders of magnitude! Strikingly, this degradation is completely recoverable under strong UV illumination or after moderate thermal treatment (~180 min at 100°C). These experiments are fully repeatable without inducing any permanent degradation in the device. This suggests that there is neither trap creation nor any kind of permanent damage. Consistent behavior is observed across the 6-inch wafer.

## Extension and location of current blockage

In order to understand this serious problem, we have carried out detailed characterization. **Fig. 2** shows the evolution of the 4 terminal currents during the stress of **Fig. 1**. As the stress voltage increases beyond 300 V, the drain-to-substrate current becomes dominant. However, at the onset of severe trapping, all currents are <1 nA/mm. The evolution of the subthreshold characteristics (**Fig. 3)** during the stress of **Fig. 1** shows that $V_T$ is unaffected suggesting that the channel current blockage responsible for current collapse is located in the extrinsic region of the device.

**Fig. 4** shows the output characteristics before and after 300 sec of OFF-state stress at 300 V. After high-voltage stress, we observe nearly complete current collapse at low $V_{DS}$. However, for higher $V_{DS}$, the drain current starts flowing again. This behavior is characteristic of channel punch-through suggesting that the blockage region where trapping takes place is relatively short along the channel direction.

To pinpoint its location, we have examined the impact of device geometry. **Fig. 5** shows that the gate-to-drain gap length, the 1st field plate (FP1) length, the 2nd field plate (FP2) length and the 3rd field-plate (FP3) length do not affect the trapping characteristics at all. In addition, **Fig. 6** graphs the drain-to-gate capacitance in the OFF state as a function of $V_{DS}$. The three steps that are observed indicate complete extension of the depletion region under each of the three field plates. We conclude that for voltages beyond $V_{DS}$=50 V, the electric field in the channel peaks under the edge of the third field-plate and increases with voltage. We then postulate that it is at this precise location, under the outer edge of the third field-plate, where the blockage to the channel current is induced.

### Trapping and detrapping dynamics

In **Fig. 7**, we show that the trapping behavior is rather insensitive to temperature from 25 to 200 °C. In addition, the evolution of the four terminal currents over this entire temperature range (not shown) confirms again that they are not the main source of electron trapping. The temperature insensitivity of the phenomenon suggests that trapping takes place through a tunneling process.

To probe this, we study the dynamics of trapping. **Fig. 8 (a)** shows the time evolution of normalized $I_{Dlin}$ under constant stress at different voltages. $I_{Dlin}$ degradation greatly speeds up with voltage. We define a characteristic trapping time $\tau$ at 50% degradation of $I_{Dlin}$. In **Fig. 8 (b)** we plot $\tau$ vs. $1/E_{PEAK}$ where $E_{PEAK}$ is the peak value of electric field inside the AlGaN barrier layer under the edge of FP3 estimated from field simulations by Silvaco (described below). This is the characteristic Zener tunneling law [4]. The excellent linearity that is obtained strongly suggests a valence-band-to-trap tunneling process. We call this "Zener trapping." A trap energy level of around 1 eV above the valence band edge is estimated from the Zener tunneling law.

To gain greater insight into this problem, we have also studied the recovery dynamics of fully trapped devices. At room temperature in the dark, the complete recovery can take many days. The recovery process can be accelerated at higher temperatures as shown in **Fig. 9** which shows $I_{Dlin}$ recovery transients after 600 sec OFF-state stress at $V_{DS}$= 200 V at different temperatures. We extract the dominant recovery time constant [5] and find that it has an activation energy of around 0.63 eV. The recovery is also accelerated under UV light. **Fig. 10** shows the UV light-induced recovery transients at room temperature of a device collapsed after 3 min at $V_{DS}$= 300 V. We use UV light of different wavelengths that are selected by a monochromator out of a broadband light source. Enhanced recovery is observed for light energies higher than 2.8 eV.

### Mechanism for total current collapse

All the observations reported here are consistent with a field-induced trapping process that takes place right under the edge of the outer-most field plate at high enough OFF-state voltage. Field simulations (**Fig. 11)** confirm that increasing $V_{DS}$ beyond the voltage that depletes the 2DEG under the outer-most field plate results in a sharply peaked electric field distribution with the peak located right under the third field plate edge. The magnitude of the electric field increases with $V_{DS}$. At this location close to the semiconductor surface, the electric field can be so intense that direct tunneling of electrons from the valence band to trap levels in the AlGaN barrier or the GaN channel can take place (**Fig. 12)**. This type of tunneling process is consistent with our temperature insensitive observations and the absence of geometrical dependencies. Our simulations indicate that at $V_{DS}$= 200 V just inside the AlGaN surface, $E_{PEAK}$ is around 3.4 MV/cm and it increases to 6.4 MV/cm at 1,000 V (**Fig. 11b**).

The traps involved in this process are likely to be those responsible for yellow luminescence in AlGaN and GaN. They are reported to be located at a depth from the conduction band of around 2.5 eV in GaN [6] and 2.8 eV in $Al_{0.2}Ga_{0.8}N$ [7]. These values are reasonably consistent with our UV light detrapping experiments (**Fig. 10**) and our estimate from the Zener law (**Fig. 8b**). Recent studies attribute yellow luminescence to substitutional C in the N site [8] though other hypotheses have been formulated. C is a common dopant in high-voltage GaN FET heterostructures. The much lower activation energy observed in the thermal detrapping process (**Fig. 9**) stems from the sharply localized nature of the trapping which allows thermal trap-to-conduction band transitions with significantly lower energies (**Fig. 13**).

### Conclusions

In summary, we report fully recoverable but total current collapse in high-voltage GaN MIS-HEMTs induced by Zener trapping at high voltage. The understanding derived here suggests that this effect can be mitigated through attention to defect control during epitaxial growth and appropriate design of the field plate structure of the device.


### Acknowledgements

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### References


[1] D. Jin *et al*, Power Semiconductor Devices and ICs (ISPSD), pp. 333-336, 2012.
[2] R. Chu *et al*, IEEE Electron Dev. Lett., vol.32, no.5, pp.632-634, 2011.
[3] W. Saito *et al*, IEEE Electron Dev. Lett., vol.31, no.7, pp.659-661, 2010.
[4] J. G. Fossum *et al*, IEEE Trans. Electron Devices, vol.32, no.9, pp.1878-1884, 1985.
[5] J. Joh *et al*, IEEE Trans. Electron Devices, vol.58, no.1, pp.132-140, 2011.
[6] E. Calleja *et al*, Phys. Rev. B, vol.55, no.7, pp.4689-4694, 1997
[7] D. R. Hang *et al*, J. Appl. Phys., vol.90, no.4, pp.1887-1890, 2001.
[8] J. L. Lyons *et al*, Appl. Phys. Lett., vol.97, no.15, pp.152108, 2010.

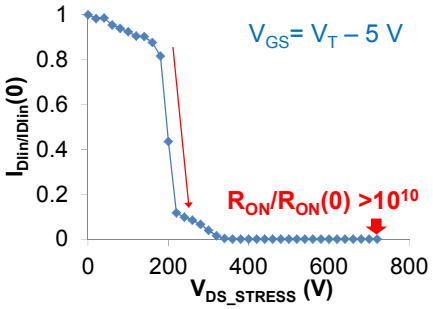


**Fig. 1.** Evolution of normalized $I_{Dlin}$ in an OFF-state step-stress experiment. $V_{GS}$ is biased at $V_T$ – 5 V and $V_{DS}$ is step-stressed by 20 V every 10 seconds up to 720 V. Total current collapse occurs for $V_{DS\_STRESS}$>300 V and $R_{ON}$ increases by ~10 orders of magnitude at the end of the experiment.

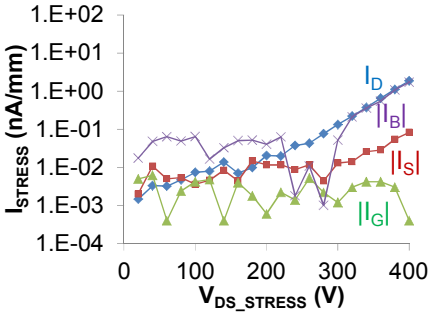


**Fig. 2.** Evolution of source ($I_S$), gate ($I_G$), drain ($I_D$), and substrate ($I_B$) currents during the stress periods of **Fig. 1** up to 400 V. As the OFF-state bias increases beyond 300 V, the drain-to-substrate current increases. At the onset of severe trapping, all currents are negligible.

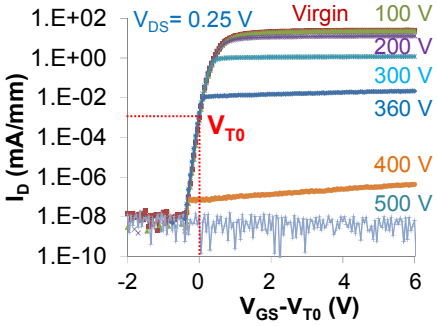


**Fig. 3.** Evolution of the linear subthreshold characteristics ($V_{DS}$= 0.25 V) during the stress of **Fig. 1.** $V_{T0}$ is the initial threshold voltage where $I_D$ is 1 µA/mm. $V_T$ does not change at all under total current collapse.

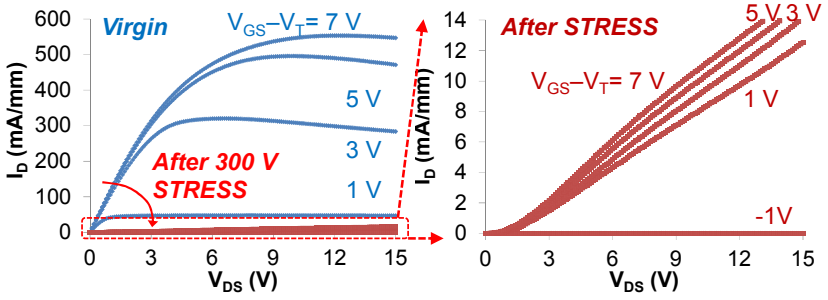


**Fig. 4.** Output characteristics before (blue) and after (red) 300 sec of OFF-state stress at $V_{DS\_STRESS}$= 300 V and $V_{GS}$= $V_T$ – 5 V. After stress, at low $V_{DS}$, nearly complete current collapse is observed. However, as $V_{DS}$ increases the drain current starts flowing again. The collapsed output characteristics resemble a punchthrough device.

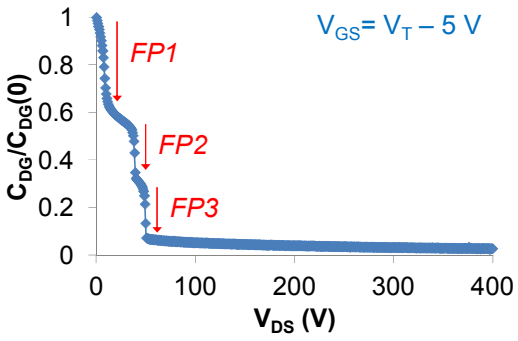


**Fig. 6.** Normalized drain-to-gate capacitance ($C_{DG}$) in the OFF state as a function of $V_{DS}$. The three steps in $C_{DG}$ indicate the complete extension of the depletion region under each of the three field plates.

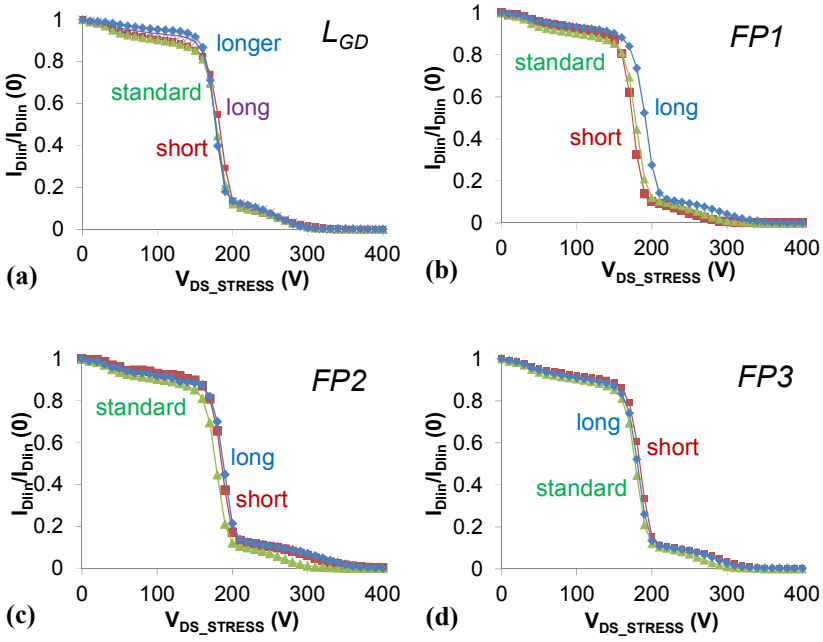


**Fig. 5.** Impact of device geometry on $I_{Dlin}$ degradation under OFF-state step-stress up to $V_{DS\_STRESS}$= 400 V and $V_{GS}$= $V_T$ – 5 V. The trapping characteristics do not depend on gate-to-drain gap length ($L_{GD}$), 1st field plate (FP1) length, 2nd field plate (FP2) length and 3rd field plate (FP3) length.

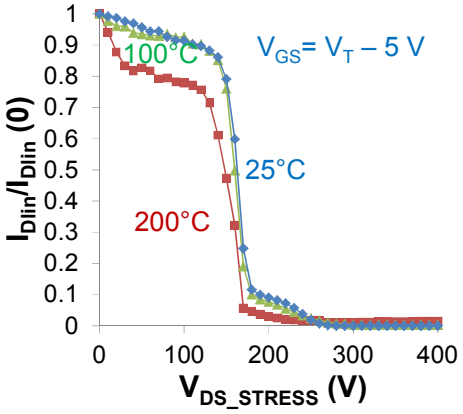


**Fig. 7.** Evolution of $I_{Dlin}$ in OFF-state step-stress experiment at temperatures from 25 to 200 °C. The trapping characteristics are insensitive to temperature.

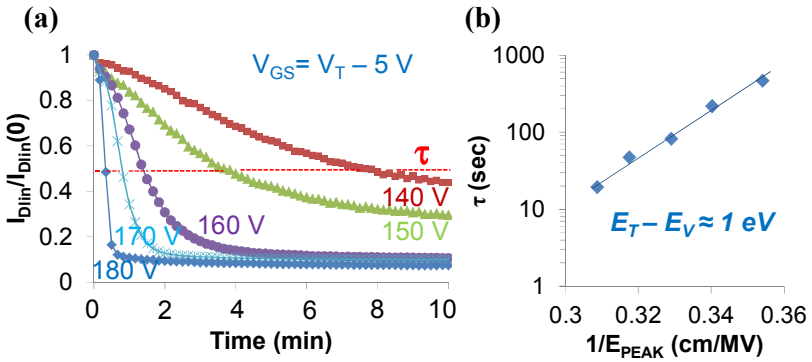


**Fig. 8** (a) Evolution of normalized $I_{Dlin}$ as a function of time in a device under constant stress bias from $V_{DS\_STRESS}$=140 to 180 V at room temperature. A characteristic trapping time (τ) is defined at the 50% degradation point of $I_{Dlin}$. (b) Zener dependence of τ: τ vs. $1/E_{PEAK}$ in a semi-log scale. $E_{PEAK}$ is the peak value of electric field inside AlGaN layer under FP3 estimated from field simulations in the same OFF-state bias conditions (**Fig. 11**). The straight line that is obtained strongly suggests a Zener tunneling process. A trap energy level of around 1 eV above valence band edge is estimated.

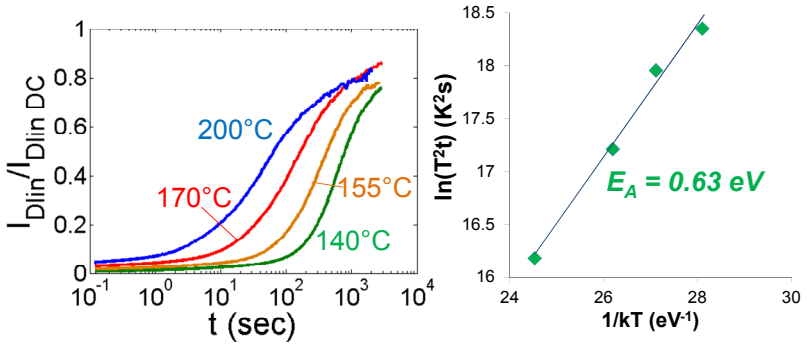


**Fig. 9.** Normalized $I_{Dlin}$ recovery transients in the dark after 600 sec OFF-state stress at $V_{DS\_STRESS}$= 200 V and $V_{GS}= V_T - 5$ V at different temperatures. $I_{Dlin\_DC}$ is the virgin DC value of $I_{Dlin}$. As T increases, the recovery speeds up. An activation energy of around 0.63 eV is extracted.

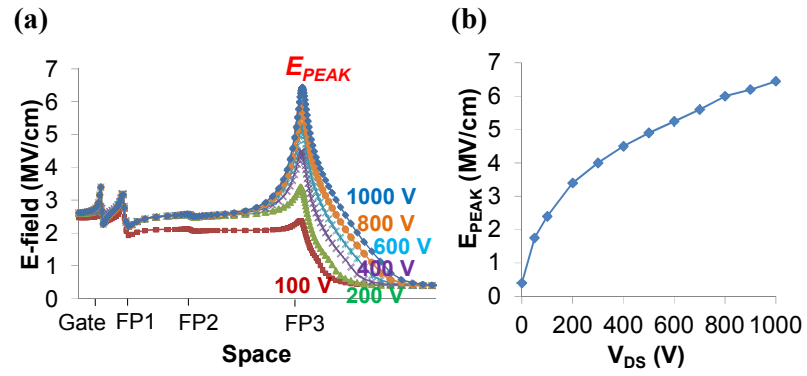


**Fig. 11.** (a) Evolution of electric field at the top surface of AlGaN barrier from gate to drain obtained from TCAD simulations (Silvaco). Beyond $V_{DS}$=200 V, the peak electric field appears under the edge of the outermost field plate and increases with $V_{DS}$. (b) Magnitude of $E_{PEAK}$ under third field-plate edge vs. $V_{DS}$ is described. At $V_{DS}$= 200 V, $E_{PEAK}$ is around 3.4 MV/cm and it increases up to 6.4 MV/cm at 1,000 V.

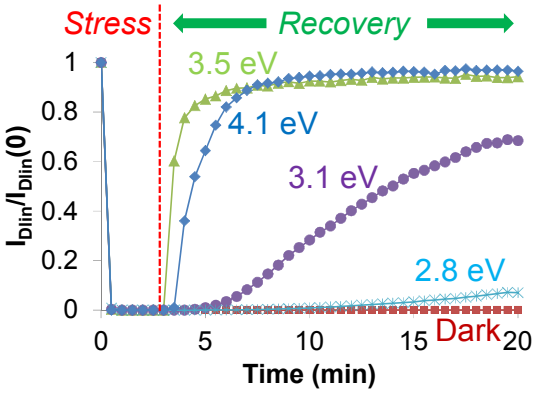


**Fig. 10.** UV-induced recovery of a device collapsed after 300 V OFF-state stress for 3 min for different energies of UV light at room temperature. Enhanced recovery is observed for light energies above 2.8 eV.

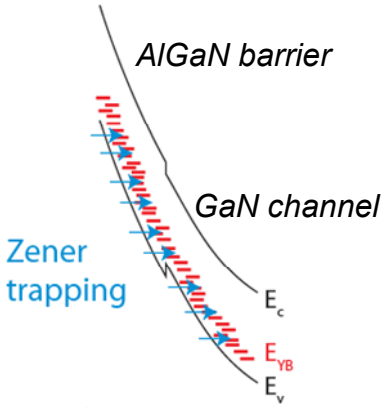


**Fig. 12.** Proposed Zener trapping mechanism responsible for the observed total current collapse. Direct electron tunneling from the valence band into defect states can be triggered under intense electric-field inside the AlGaN barrier layer or at the top of the GaN channel.

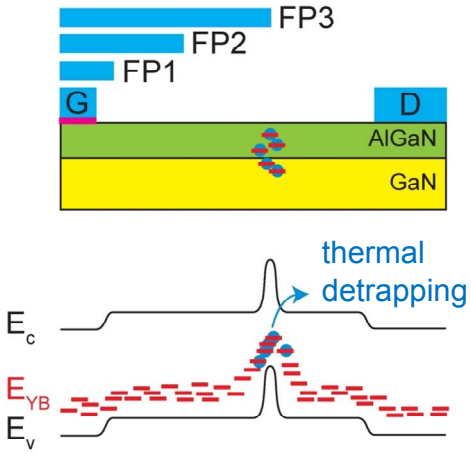


**Fig. 13.** Energy band diagram along surface from gate to drain with device biased in the linear regime after a total current collapse event. OFF-state trapping results in a sharp energy barrier directly below the edge of the outermost field plate that blocks current. In the linear regime, thermal detrapping can take place as indicated with an activation energy substantially lower than the ionization energy of the trap.