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High-Frequency Characteristics of InGaAs Quantum-Well MOSFETs

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1. Introduction

It has been more than 3 decades since the High-Electron Mobility Transistor (HEMT) was invented, revolutionizing the world of high-frequency electronics [1-2]. According to Prof. Mimura who invented the HEMT in 1980 [3], it is interesting to see that his groups at that time began with research on GaAs metal-oxide-semiconductor field-effect transistors (MOSFETs) in 1977, motivated by superior carrier transport of GaAs material which would offer high-speed performance than Si electronics [4]. However, their efforts failed to exhibit accumulation and/or inversion carriers in the channel due to poor interface-state quality between oxide and GaAs [4]. This makes it challenging to realize a III-V MOSFET. Instead, III-V HEMTs have been matured and steadily achieved higher levels of performance matrix, such as high-frequency gain, noise figure (NF) and power density. To date, InAs HEMTs on GaAs deliver the best balanced high-frequency response (high f_T *and* high f_{max}) of any transistor technology toward the first true THz transistor (both f_T and f_{max}>1 THz) [1].

In early 2000s, indium-rich $In_xGa_{1-x}As$ material system re-gained its interest, and now stands out as the most promising non-Si n-channel material for next-generation low-power and high-speed nano-scale CMOS [5]. This is a consequence of its superior electron carrier transport properties coupled with excellent interface quality between high-k dielectric and InGaAs channel by ALD [6]. Indeed, significant progress has been made on a variety of GaAs and InGaAs MOSFETs for several years by many different groups. This paper reviews recent progress on high-frequency characteristics of InGaAs quantum-well MOSFETs, and discusses options to further improve high-frequency response.

2. Evolution of III-V Gate Stack

The key enabler for InGaAs MOSFETs is a high-quality oxide/semiconductor interface by ALD. Many groups have successfully demonstrated excellent interfacial quality between ALD-grown Al_2O_3 and InGaAs channel, finally demonstrating surface-channel InGaAs transistors [7-10]. In principle, it must be trap and/or defect free at the semiconductor/oxide interface, and should consist of a metal gate for work-function engineering and a high-k insulator on III-V channels for future EOT consideration. The pressing need is for an ultra-scaled gate-to-channel design with total EOT well below 1 nm, toward 7-nm technology-node. In fact, a bi-layer Al_2O_3/HfO_2 MOS structure has been proposed with EOT < 1 nm by several groups [8, 11].

In the meantime, buried-channel design schemes, such as Al_2O_3-$In_{0.52}Al_{0.48}As$ and Al_2O_3-InP, allow to demonstrate excellent ON-to-OFF transition in the transistor operation, as assessed by subthreshold-swing and DIBL [12-15]. **Fig. 1** shows C-V and interface-state density (D_{it}, inset) characteristics of III-V MOS-Capacitor with Al_2O_3/InP (3/2-nm) on $In_{0.53}Ga_{0.47}As$ channel, indicating reasonably good oxide-semiconductor interface quality (D_{it} = ~ 4×10^{12} /cm^2-eV) [15]. **Fig. 2** shows subthreshold characteristics of buried-channel InGaAs MOSFET with $Al_2O_3/In_{0.52}Al_{0.48}As$ (3/10-nm) composite barrier [13]. This yields nearly ideal subthreshold characteristics with L_g = 150 nm device, such as S = 70 mV/dec and DIBL = 35 mV/V [13].

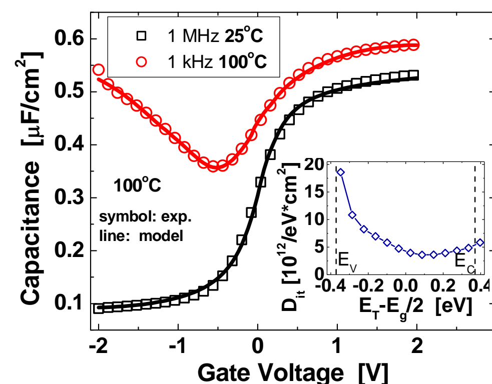

Fig. 1: C-V and interface-state density (D_{it}, inset) characteristics of III-V MOS-Capacitor with Al_2O_3/InP buried-channel design [15].

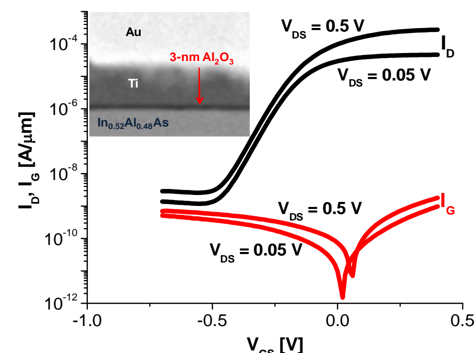

Fig. 2: Subthreshold characteristics of L_g = 150 nm buried-channel InGaAs MOSFETs with $Al_2O_3/In_{0.52}Al_{0.48}As$ (3/10-nm) composite barrier [13].

3. Progress on RF III-V MOSFETs

A major step was the use of ALD-grown Al_2O_3 as a gate dielectric in the course of III-V MOSFET fabrication [6]. The bottom line is that during ALD, a kind of 'self-cleaning effect' takes places such that III-V surface oxides are effectively removed [5]. This has been successfully demonstrated and reported by many groups since then. Finally, this opens the door to a variety of III-V MOSFET demonstration. For example, **Fig. 3** shows microwave characteristics of L_g = 60 nm buried-channel $In_{0.7}Ga_{0.3}As$ MOSFETs with Al_2O_3/InP (1/3-nm) composite barrier [16]. Excellent high-frequency characteristics can be observed in III-V MOSFETs, such as current-gain cutoff frequency (f_T) = 371 GHz and maximum oscillation frequency (f_{max}) = 280 GHz [16].

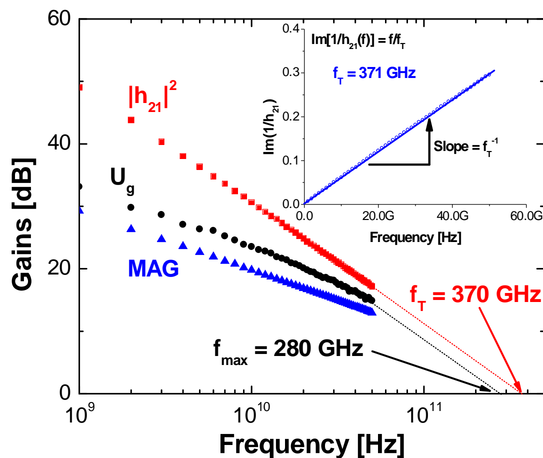

Fig. 3: Microwave gain characteristics of L_g = 60 nm buried-channel $In_{0.7}Ga_{0.3}As$ MOSFETs with Al_2O_3/InP (3/1-nm) composite barrier [16].

4. Prospect of III-V MOSFETs for RF applications

Starting from III-V MOSFETs with state-of-the-art high-frequency characteristics, it is very useful to benchmark InGaAs MOSFETs against III-V FETs. **Fig. 4** shows the evolution of the current-gain cut-off frequency of InGaAs MOSFETs as well as III-V FETs as a function of time, such as GaAs MESFET, GaAs PHEMT and InP HEMT. Today's InP HEMTs still exhibit a far better f_T than InGaAs MOSFETs. But, this is mostly due to low-parasitic capacitance design employed in InP HEMTs, such as T-gate. In fact, InGaAs MOSFETs have now matched or even surpassed the transconductance (g_m) of InP HEMTs. This is a consequence of lower R_{ON} (ON-resistance) in the device operation. In order words, InGaAs MOSFETs indeed exhibit a far better source- and drain-resistance (R_s and R_d) than those of InP HEMTs. What is behind is the effective removal of the presence of a barrier tunnel resistance in InGaAs MOSFET contact design. Sooner or later, it is expected that InGaAs MOSFETs with better high-frequency characteristics would be reported if low parasitic-capacitance MOSFET designs are proposed and/or developed.

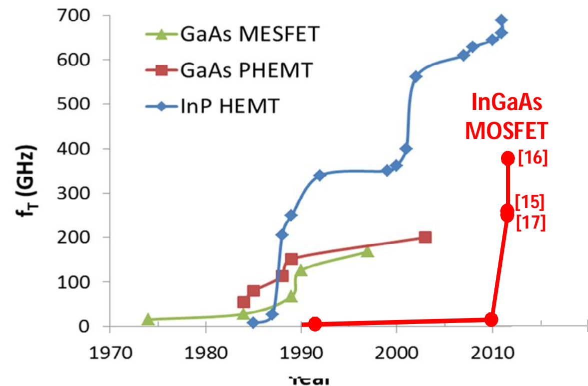

Fig. 4: f_T vs year of demonstration of InGaAs MOSFETs and III-V FETs, such as GaAs MESFET, GaAs PHEMT and InP HEMT.

5. Conclusions

III-V MOSFETs is poised to take the lead on high-frequency electronics. If and when this happens, indium-rich $In_xGa_{1-x}As$ is the most preferable channel material. Indeed, remarkable progress has been made, in the area of III-V gate-stack with ALD-grown dielectric. This paper has briefly reviewed the evolution of high-frequency III-V MOSFETs and has discussed paths forward to further improve high-frequency response.

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