Applied Physics Express **5** (2012) 064002
DOI: 10.1143/APEX.5.064002

A Self-Aligned InGaAs Quantum-Well Metal–Oxide–Semiconductor Field-Effect Transistor Fabricated through a Lift-Off-Free Front-End Process

Jianqiang Lin*, Tae-Woo Kim, Dimitri A. Antoniadis, and Jesús A. del Alamo

Massachusetts Institute of Technology, Cambridge, MA 02139, U.S.A.

Received March 17, 2012; accepted April 22, 2012; published online May 16, 2012

We present a novel n-type InGaAs quantum-well metal–oxide–semiconductor field-effect transistor (QW-MOSFET) fabricated by a self-aligned gate-last process and investigate relevant Si-like manufacturing issues in future III–V MOSFETs. The device structure features a composite InP/Al_2O_3 gate barrier with a capacitance equivalent thickness (CET) of 3 nm and non alloyed Mo ohmic contacts. We have found that RIE introduces significant damage to the intrinsic device resulting in poor current drive and subthreshold swing. The effect is largely removed through a thermal annealing step. Thermally annealed QW-MOSFETs exhibit a subthreshold swing of 95 mV/dec, indicative of excellent interfacial characteristics. The peak mobility of the MOSFET is 2780 $cm^2 V^{-1} s^{-1}$.

InAs-rich InGaAs is a promising candidate as a channel material for future high-performance complementary metal–oxide–semiconductor (CMOS) applications because of its superior electron transport properties. Studies on high-electron-mobility transistors (HEMTs) have demonstrated that excellent logic characteristics, such as current drive, subthreshold swing, and drain-induced barrier lowering (DIBL), can be obtained from thin-channel devices.[1–4] Deeply scaled InGaAs HEMTs have also shown greatly improved electron injection velocity with respect to Si metal–oxide–semiconductor field-effect transistors (MOSFETs) at a much reduced voltage.[5,6] Significant progress has recently been made on gate dielectric integration, transistor architecture, and process innovation in InGaAs MOSFETs.[7–12] Recently, InGaAs-based quantum-well MOSFETs (QW-MOSFETs) on silicon substrate have been demonstrated.[13] However, all these devices have been fabricated through a non scalable and non-manufacturable HEMT-like fabrication process that yields a large source–drain (S/D) contact separation on the order of 1.5 to 2 μm and is based on lift-off of metals that are not compatible with Si processing. In a future high-density III–V CMOS technology, it is imperative to utilize self-aligned device architectures involving highly anisotropic etching and Si-compatible metals. In this regard, RIE damage is a serious concern. There are reports of RIE damage of III–V heterostructures caused by fluorine, oxygen, and hydrogen.[14–18] However, RIE damage to a III–V MOSFET is a topic that has so far received little attention in the emerging field of III–V CMOS. In this work, we demonstrate a self-aligned InGaAs QW-MOSFET architecture utilizing a lift-off free gate-last front-end process that utilizes Si-CMOS-process-compatible metals. We show that reactive ion etching (RIE) damage is indeed severe, but that to a great degree, it can be removed by a low-temperature annealing process.

Figure 1 shows a schematic diagram of the QW-MOSFET structure. This device architecture leverages a self-aligned process developed for high-frequency InGaAs HEMTs.[9,19,20] In essence, this is a gate-last process in which the gate is nested in a self-aligned way in a recess fabricated in the ohmic contact structure.

The heterostructure is epitaxially grown on InP substrate and includes a 15 nm InGaAs channel, a 4 nm InP etch stop and a 15 nm InGaAs cap doped to 2×10^{19} cm^{-3} with Si. All the layers are lattice-matched with InP. A sheet dopant of silicon 1×10^{12} cm^{-2} is introduced 5 nm beneath the channel in the InAlAs buffer. The total InAlAs buffer is about 400 nm.

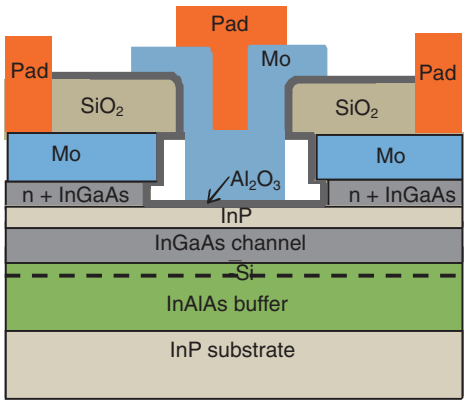

Fig. 1. Cross-sectional schematic of self-aligned InGaAs QW-MOSFET. A self-aligned air spacer that is passivated by Al_2O_3 separates the S/D and gate metal. The side recess length (L_{side}) is 100 nm.

Device fabrication begins with a blanket evaporation of 50 nm of Mo. After mesa isolation, a 60 nm plasma-enhanced chemical vapor deposition (PECVD) SiO_2 layer is deposited. Following gate foot photolithography, the SiO_2 is etched with CF_4-based RIE.[19] The Mo is etched vertically in a process adapted from a W etch recipe.[19] This is an anisotropic SF_6-based RIE process step with a DC bias of −50 V and RF power of 250 W. The etchstop is monitored in real time. The total etch time is 180 s including at least 30% overetching. Then, the Mo is pulled back from the edges of the SiO_2 using time-controlled isotropic plasma etching with O_2/CF_4 ($O_2 : CF_4 = 4 : 1$). The conditions of this etch are 300 W RF power and zero DC bias.[19,20] This etching is selective to InGaAs and SiO_2 and results in less than 100 nm side recess of the Mo for an etch time of 120 s. At this point, a 15 min, 340 °C anneal in Nitrogen is performed to eliminate RIE damage. The InGaAs cap is subsequently etched using citric acid/H_2O_2. This results in a small undercut beneath the Mo. The total length, L_{side}, from the edge of the gate to the edge of the cap is 100 nm. A short ashing step is introduced to remove residual surface particles. Diluted H_2SO_4 is used as the pregate dielectric deposition cleaning process. At this point, the InP barrier is

*E-mail address: linjq@mit.edu

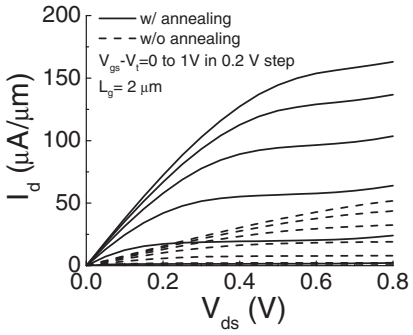

Fig. 2. Output characteristics of QW-MOSFET with (solid) and without (dashed) RIE damage annealing.

exposed and is slightly thinned. Following this, a 4 nm Al_2O_3 layer is deposited using atomic layer deposition (ALD) at 250 °C with trimethyl aluminum (TMA) and H_2O as precursors. The conformal Al_2O_3 also passivates the exposed surface of the air spacers and minimizes parasitic resistance. Immediately after ALD, the Mo gate electrode is evaporated, followed by RIE patterning. In our process, the use of Mo as gate metal has several advantages: Mo is a CMOS-compatible material, it allows top-down patterning through RIE, and has a suitable workfunction. These are all essential features for VLSI processing and ALD dielectric integration.

Figure 2 shows output characteristics of a 2-μm-gate length self-aligned QW-MOSFET without (dashed) and with (solid) the 340 °C RIE damage annealing. It is clear that Mo RIE introduces severe damage to the device (the Mo layer shields the semiconductor structure during SiO_2 RIE).

The transfer characteristics of the QW-MOSFET are shown in Fig. 3(a). For devices with RIE damage annealing, the peak transconductance is 205 μS/μm at $V_{ds} = 0.5$ V. $V_{t\text{-sat}}$ is −37 mV ($V_{t\text{-sat}}$ is defined at $V_d = 0.5$ V and at 1 μA/μm). This is close to the enhancement-mode operation required for CMOS logic application. The subthreshold and gate leakage characteristics are shown in Fig. 3(b). The subthreshold swing (S) improved from 300 mV/dec without RIE damage annealing to 95 mV/dec. A very low gate leakage current density (J_g) of 1.1×10^{-4} A/cm^2 at 1 V gate overdrive is also achieved. These results suggest not only a high-quality gate stack, but also that the self-aligned device structure has excellent isolation between S/D and gate in spite of their close proximity.

The capacitance equivalent oxide thickness (CET) for the composite InP/Al_2O_3 gate barrier is estimated to be 3 nm. The capacitance–voltage (C–V) characteristics at 1 and 100 kHz are shown in Fig. 4(a), where the capacitance is measured between the gate and S/D. Significant frequency dispersion appears in the sample without annealing. The CET is 3 nm for the annealed devices. Figure 4(b) shows channel mobility before and after annealing. While the RIE damage does not affect significantly the mobility at high carrier density, presumably because the damage-induced charges are screened, the effect is significant at low density. This is consistent with the observation of frequency dispersion in the same region of C–V curves [Fig. 4(a)] and the significant impact on the ON resistance, which is

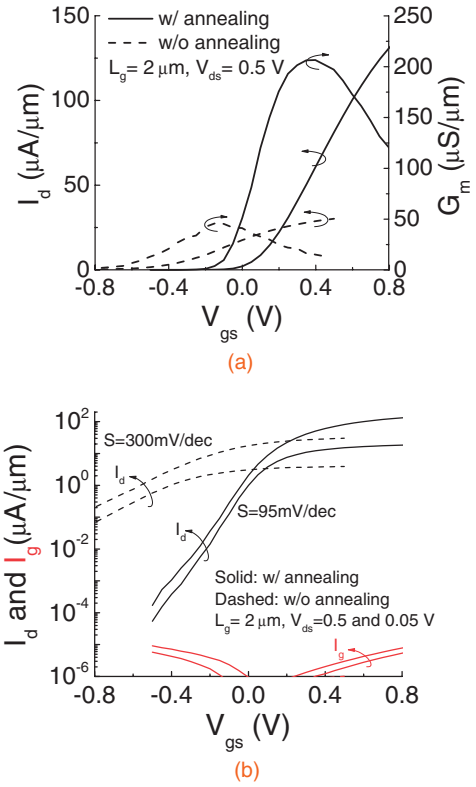

Fig. 3. (a) Transfer and transconductance characteristics of QW-MOSFET with (solid) and without (dashed) RIE damage annealing. (b) Subthreshold characteristics and gate leakage current of QW-MOSFET with (solid) and without (dashed) RIE damage annealing.

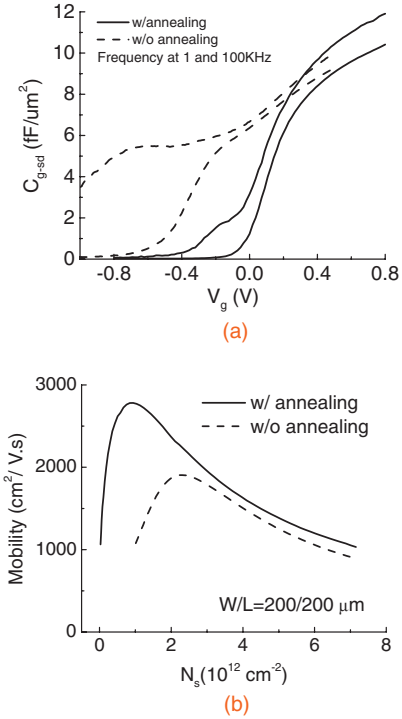

Fig. 4. (a) Capacitance vs gate voltage at 1 and 100 kHz. (b) Mobility vs channel sheet electron concentration. Capacitance and mobility are extracted from FatFETs ($W/L_g = 200/200$ μm) with and without RIE damage annealing using the split C–V method. Sheet charge density is obtained from $C_{g\text{-}sd}$ at 100 kHz. Drain current is measured at $V_{ds} = 50$ mV.

evident in Fig. 2. The peak mobility is 2780 $cm^2 V^{-1} s^{-1}$, which compares well with the results reported by other authors in similar non-reactive-ion-etched buried-channel structures.[21)]

The total source resistance (R_s) measured by the R_{ch}–L_g extrapolation method is 260 Ω μm. Using separate TLM structures, we have decomposed this into its three main components. The largest one is the Mo lateral resistance, which contributes 120 Ω μm. This arises from the relatively high resistivity of E-beam-evaporated Mo,[22)] in our case, exhibiting a sheet resistance of about 25 Ω/□. A solution to this is the use of a less-resistive metal, such as sputtered W.[19)] The next most significant component of R_s is the access resistance associated with the air spacer of length L_{side}, which is estimated to be 100 Ω μm. The access resistance can be further mitigated by reducing L_{side} and by higher inverted doping. Finally, the vertical resistance between the Mo cap and the channel is estimated to be 50 Ω μm. This is substantially smaller than in a conventional HEMT.[19)] It can be further reduced through cap design optimization. The sum of these three components is in good agreement with the R_s determined by the R_{ch}–L_g extrapolation method.

The incorporation of fluorine and oxygen in these types of heterostructures is known to cause reductions in carrier concentration and mobility,[14–16)] presumably as a result of ion incorporation that results in dopant passivation and increased scattering. Our work shows that RIE also severely impacts the subthreshold characteristics, suggesting additional interface damage. Its detailed nature is unknown. Fortunately, a relatively benign thermal step is effective in mitigating this damage.

In summary, a novel n-type InGaAs QW-MOSFET is fabricated via a gate-last process. The QW-MOSFET features a self-aligned Mo contact and a composite InP/Al_2O_3 gate barrier, and Mo gate metal. The front-end process is entirely lift-off free. RIE-induced damage is observed but largely annealed through a pregate thermal treatment. The QW-MOSFET exhibits excellent subthreshold behavior, mobility, and parasitic resistance characteristics. The demonstrated self-aligned device architecture offers the potential of scaling to very small dimensions.

Acknowledgments This research was sponsored by the Focus Center Research Program at the Center for Materials, Structures, and Devices. The authors would like to thank J. Hoyt for helpful discussions. Epitaxial heterostructures were grown by IntelliEpi Inc. Device fabrication was carried out at the Microsystems Technology Laboratories of MIT.

1) J. A. del Alamo: Nature **479** (2011) 317.
2) J. A. del Alamo, D.-H. Kim, T.-W. Kim, D. Jin, and D. A. Antoniadis: IPRM Tech. Dig., 2011.
3) G. Dewey, M. K. Hudait, L. Kangho, R. Pillarisetty, W. Rachmady, M. Radosavljevic, T. Rakshit, and R. Chau: IEEE Trans. Electron Devices **29** (2008) 1094.
4) D.-H. Kim, J. A. del Alamo, J.-H. Lee, and K.-S. Seo: IEEE Trans. Electron Devices **54** (2007) 2606.
5) D.-H. Kim, J. A. del Alamo, D. A. Antoniadis, and B. Brar: IEDM Tech. Dig., 2009, p. 861.
6) D.-H. Kim, B. Brar, and J. A. del Alamo: IEDM Tech. Dig., 2011, p. 319.
7) J. Lin, S. Lee, H.-J. Oh, W. Yang, G. Q. Lo, D. L. Kwong, and D. Z. Chi: IEDM Tech. Dig., 2008, p. 401.
8) M. Egard, L. Ohlsson, B. M. Borg, F. Lenrick, R. Wallenberg, L.-E. Wernersson, and E. Lind: IEDM Tech. Dig., 2011, p. 304.
9) Y. Yonai, T. Kanazawa, S. Ikeda, and Y. Miyamoto: IEDM Tech. Dig., 2011, p. 307.
10) R. Terao, T. Kanazawa, S. Ikeda, Y. Yonai, A. Kato, and Y. Miyamoto: Appl. Phys. Express **4** (2011) 054201.
11) S. H. Kim, M. Yokoyama, N. Taoka, R. Iida, S. Lee, R. Nakane, Y. Urabe, N. Miyata, T. Yasuda, H. Yamada, N. Fukuhara, M. Hata, M. Takenaka, and S. Takagi: Appl. Phys. Express **4** (2011) 024201.
12) X. Li, R. J. W. Hill, P. Longo, M. C. Holland, H. Zhou, S. Thoms, D. S. Macintyre, and I. G. Thayne: J. Vac. Sci. Technol. B **27** (2009) 3153.
13) M. Radosavljevic, B. Chu-Kung, S. Corcoran, G. Dewey, M. K. Hudait, J. M. Fastenau, J. Kavalieros, W. K. Liu, D. Lubyshev, M. Metz, K. Millard, N. Mukherjee, W. Rachmady, U. Shah, and R. Chau: IEDM Tech. Dig., 2009, p. 319.
14) H. Uchiyama, T. Taniguchi, and M. Kudo: IEEE Trans. Device Mater. Reliab. **5** (2005) 706.
15) A. Hulsmann, W. Bronner, A. Leuther, M. Maier, and G. Weimann: Proc. 26th Int. Symp. Compound Semiconductors, 1999, p. 329.
16) N. Hayafuji, Y. Yamamoto, N. Yoshida, T. Sonoda, S. Takamiya, and S. Mitsui: Appl. Phys. Lett. **66** (1995) 863.
17) S. J. Pearton, F. Ren, J. R. Lothian, T. R. Fullowan, R. F. Kopf, U. K. Chakrabarti, S. P. Hui, A. B. Emerson, R. L. Kostelak, and S. S. Pei: J. Vac. Sci. Technol. B **9** (1991) 2487.
18) S. J. Pearton and D. P. Norton: Plasma Processes Polym. **2** (2005) 16.
19) N. Waldron, D.-H. Kim, and J. A. del Alamo: IEEE Trans. Electron Devices **57** (2010) 297.
20) T.-W. Kim, D.-H. Kim, and J. A. del Alamo: IEDM Tech. Dig., 2010, p. 696.
21) T. Kanazawa, K. Wakabayashi, H. Saito, R. Terao, T. Tajima, S. Ikeda, Y. Miyamoto, and K. Furuya: IPRM Tech. Dig., 2010.
22) M. A. Martinez and C. Guillen: J. Mater. Process. Technol. **143–144** (2003) 326.