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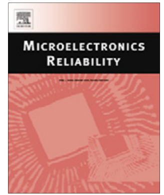

# Impact of gate placement on RF power degradation in GaN high electron mobility transistors

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A B S T R A C T

We have investigated the RF power degradation of GaN high electron mobility transistors (HEMTs) with different gate placement in the source–drain gap. We found that devices with a centered gate show different degradation behavior from those with the gate placed closer to the source. In particular, centered gate devices degraded through a mechanism that has a similar signature as that responsible for high-voltage DC degradation in the OFF state and is likely driven by electric field. In contrast, offset gate devices under RF power stress showed a large increase in source resistance, which is not regularly observed in DC stress experiments. High-power pulsed stress tests suggest that the combination of high voltage and high current stress maybe the cause of RF power degradation in these offset-gate devices.

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## 1. Introduction

GaN high electron mobility transistors (HEMTs) have revolutionized power amplification from the RF to the millimeter-wave regime. At 4 GHz, a power density in excess of 40 W/mm has been demonstrated [1]. This is over ten times that of GaAs. In W band, a power output approaching 1 W has been recently achieved [2]. This is over a factor of two better than the best prior results obtained with InP HEMT technology. GaN HEMT RF power technology is also maturing very quickly. Counter-IED (Improvised Explosive Device) systems using GaN HEMT technology have been deployed in the field. Also, cellular base stations are being deployed using GaN HEMT with multi-hundred watt power levels [3]. On the manufacturing front, several companies have announced volume manufacturing based on 100-mm SiC wafers [4–6].

Great progress has also taken place lately regarding the RF power reliability of GaN HEMTs. At 28 V, an RF operational lifetime of over 2 years has been demonstrated in X band (at 3 dB compression and $T_j$ = 150 °C) [5]. At 47 V, a mean-time to failure (MTTF) of $10^7$ h has been reported in C band with an activation energy ($E_a$) of 1.62 eV (5 dB compression, $T_j$ = 150 °C) [7]. Even at much higher frequencies, 40 GHz, an MTTF of $7 \times 10^7$ h has been obtained with $E_a$ = 1.5 eV (1.5 dB compression, $T_j$ = 150 °C) [8]. These are all very significant and encouraging results that bode well for the use of this technology in a wide range of applications.

In spite of this impressive progress, understanding of the physics of degradation of GaN HEMTs under RF power stress is still lacking. While DC reliability has been studied extensively [9–20], much less attention has been given to the RF reliability of this technology [21–26]. It is known that RF stress produces a loss of output power, gain and PAE, a reduction in the maximum drain current of the transistor, an increase in gate current, a $V_T$ shift and an increase in dispersion, among other deleterious changes [21–26]. Generally, it has been observed that RF stress introduces more degradation that its DC bias point alone [25]. The physics behind this degradation, however, is not understood. There are indications that RF degradation mechanisms might be different from DC mechanisms [22,25] and that several mechanisms might be in competition [24,26]. It is becoming clear that ensuring DC reliability does not necessarily guarantee RF reliability. In this instance, detailed understanding of the mechanisms behind RF degradation is essential in order to continue to improve the RF reliability of GaN HEMTs.

Towards this goal, we have developed a methodology to systematically investigate RF reliability and to compare it with DC reliability [25]. In a previous study, we found that RF stress introduces much more severe degradation than DC stress at a given bias point and that the degradation increases as the input power level increases. Unlike DC stress, RF stress was found to result in a prominent increase in source resistance. The pattern of degradation was very different from that induced by high-voltage OFF state stress in similar devices [12]. In fact, the degradation was traced to the simultaneous application of high voltage and high current stress during the RF swing. This mode of degradation could not be reproduced through DC stress alone as a result of instantaneous device destruction due to severe self-heating. Pulsed stress at high current and high voltage reproduced these results quite well inducing a large increase in source resistance [25].

In this work, we investigate how the placement of the gate in the source–gate gap impacts RF degradation. In devices with the gate centered in the source–drain gap, we find a pattern of

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degradation that resembles that of high-voltage DC stress in this technology. This is markedly different from the devices in Ref. [25] which had the gate offset towards the source. This research confirms the complexities involved in RF degradation and the need for further research in this area.

## 2. Experimental

This research is carried out on a four-channel Accel-RF life-test system AARTS RF10000-4/S. The built-in switching matrix in the Accel-RF system allows us to temporarily stop RF stressing and perform extensive in situ device characterization through an external semiconductor parameter analyzer [25]. This approach yields far more information about device degradation than conventional RF stress tests where only a few figures of merit are typically monitored in the course of the experiment (Fig. 1, left). Also, in the conventional approach, data interpretation can be confusing if stress conditions, such as power level or bias point, change during the test because many other parameters shift as a result of this alone. On the other hand, in our approach (Fig. 1, right), extensive and frequent RF and DC characterization enables a detailed investigation of device degradation. Also, in our scheme, external characterization is performed under standardized conditions (bias and temperature). In consequence, deliberately changing stress conditions does not confuse the experiment.

A typical experiment consists of two nested characterization loops created around the stress routine (right in Fig. 1). In an inner loop, we monitored several DC figures of merit through the external semiconductor parameter analyzer such as $I_{Dmax}$ (defined at $V_{DS}$ = 5 V and $V_{GS}$ = 2 V), $I_{Goff}$ (defined at $V_{DS}$ = 0.1 and $V_{GS}$ = –5 V), $R_S$, and $R_D$ (separately measured by the gate current injection technique [27]) and others. Using the internal RF instruments, we also monitor RF figures of merit such as saturated $P_{out}$ (measured at $V_{DS}$ = 28 V and $I_{DQ}$ = 100 mA/mm with $P_{in}$ = 23 dBm) and linear gain $G_{lin}$ (at $P_{in}$ = 10 dBm). Although the designed operating voltage for the tested MMICs was 40 V, the conditions of all these figures of merit were selected to minimize device degradation as a result of characterization alone. As shown in Fig. 2, there is a significant drop (>0.2 dB) in saturated $P_{out}$ as well as a noticeable increase in current collapse after carrying out 200 RF characterization events at 40 V. However, RF characterization at 28 V was much more benign. We have confirmed that the RF performance at 28 V correlates well with that at 40 V (Fig. 3). In the inner loop, characterization is typically carried out every 5 min at $T_{base}$ = 50 °C.

In an outer characterization loop (Fig. 1, right) at selected times during the experiment we also carried out a more comprehensive DC and RF characterization involving a complete set of *I*–*V* characteristics over a broad voltage range and a full RF power sweep at $V_{DS}$ = 28 V and $I_{DQ}$ = 100 mA/mm. We also measured current collapse (defined as the relative change in $I_{Dmax}$ in a fully detrapped device after applying a 1 s $V_{DS}$ = 0 and $V_{GS}$ = –10 V trapping pulse [28]) and permanent degradation in $I_{Dmax}$. This is defined as the change in fully detrapped $I_{Dmax}$ with respect to its original value at the beginning of the experiment. These figures of merit were measured at room temperature after a detrapping step that consisted of heating the device at 100 °C for 30 min (Fig. 1). More details of the experimental setup and experiment procedures are described in Ref. [25].

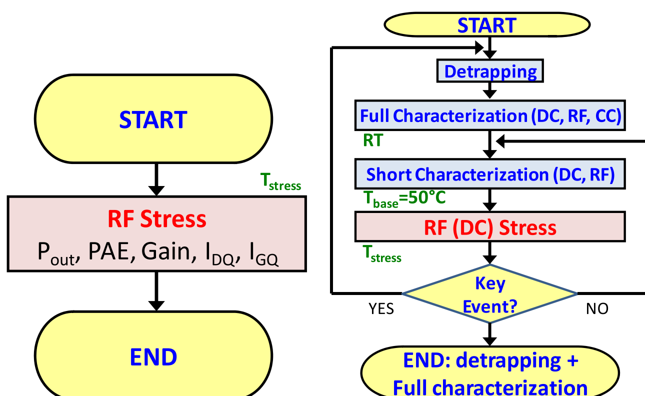


**Fig. 1.** Flowcharts of RF stress test for conventional approach (left) and the approach in this work (right).

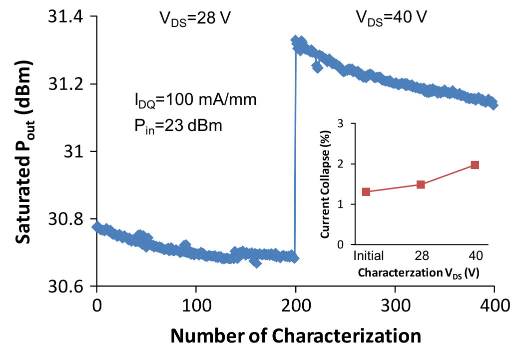


**Fig. 2.** Change in saturated $P_{out}$ during 200 RF characterization events at 28 V and 40 V without stressing the device. Inset: current collapse before and after running 200 RF characterization events at 28 V and 40 V at room temperature.

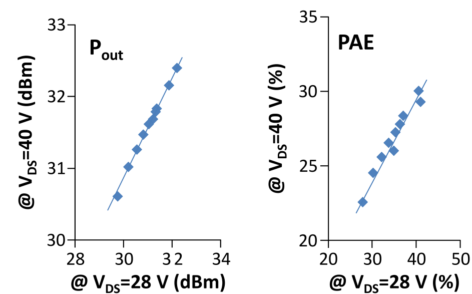


**Fig. 3.** Correlation between RF figures of merit measured at 28 V and at 40 V at room temperature during a typical RF stress test. For both conditions, $I_{DQ}$ = 100 mA/mm and $P_{in}$ = 23 dBm. The different data points represent measurements on the same device at different stages of RF stress.

In this paper we describe DC and RF step-$P_{in}$ experiments performed on single-stage internally-matched MMICs. The devices have a gate width of 4 × 100 μm with gates centered in the source–drain gap. These devices are characterized by an OFF-state stress critical voltage of about 60 V at room temperature. The main purpose of this experiment was to compare with our previous results in Ref. [25] that were obtained on similar devices where the gate was shifted towards the source by 1 μm.

We first stressed the device under DC with $V_{DS}$ = 40 V and $I_{DQ}$ = 100 mA/mm for 5 h. Then, in order to analyze the impact of RF input power level, we applied an RF signal with $P_{in}$ = 1 dBm on top of this DC bias for an additional 5 h. This was followed by large-signal RF step-stress with increasing $P_{in}$ from 20 to 27 dBm (Fig. 4). The MMIC device was stressed for 5 h at each step, and the step size was 1 dBm. $T_{base}$ for stress was constant at 50 °C throughout the experiment. The junction temperature is estimated to range from 110 °C under DC to 230 °C at its peak. However, we have confirmed in a separate experiment that maintaining the channel temperature constant throughout the experiment gives qualitatively similar results [25]. Under these conditions, the device peak PAE occurs at a $P_{in}$ = 24 dBm. In this experiment, we drive the device 3 dB beyond the peak PAE point.

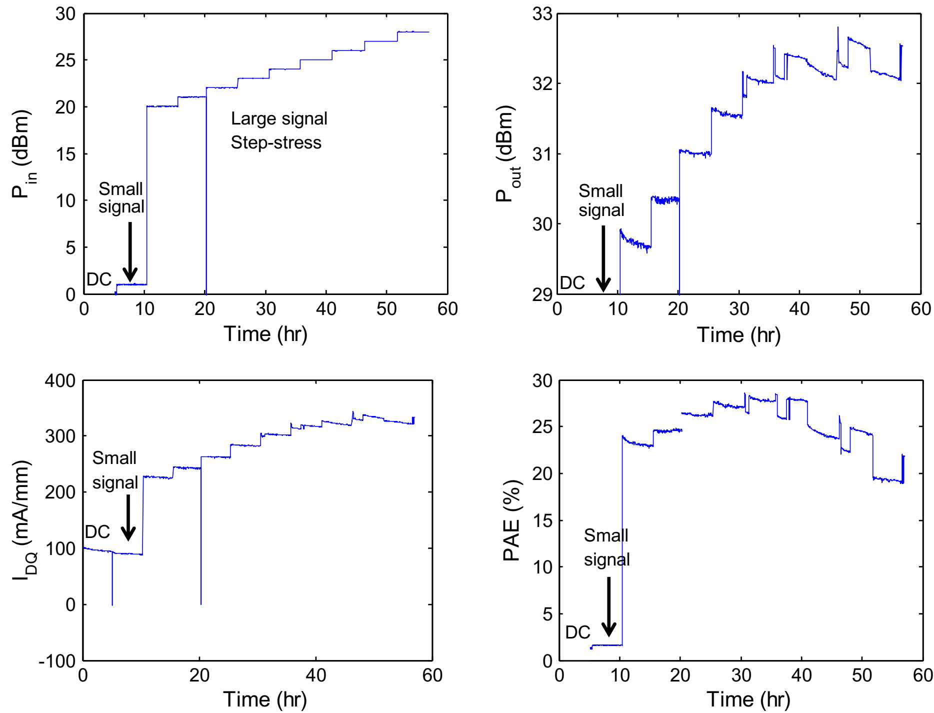


**Fig. 4.** Stress input power, output power, quiescent drain current $I_{DQ}$ and PAE during a DC and RF step-$P_{in}$ stress test. DC stress at $V_{DS}$ = 40 V and $I_{DQ}$ = 100 mA/mm was followed by RF stress steps around that bias point with varying $P_{in}$ = 1–27 dBm. These measurements were done in the inner loop (stress phase in Fig. 1, right) at $T_{base}$ = 50 °C.

## 3. Result

The instantaneous evolution of input power, output power, PAE and bias drain current during the stress is shown in Fig. 4. This is all that would have been obtained in a conventional RF power stress experiment that does not benefit from the additional characterization that we perform using our methodology. It is clear that device degradation is taking place. At any constant $P_{in}$ step, $P_{out}$ tends to drop with time, especially at high $P_{in}$. Because of the changing input power level, it is difficult to quantify the degradation that occurred in each step.

In our approach, the additional characterization that we perform (Fig. 1, right) allows us to analyze device degradation in each step in more detail. The evolution of RF figures of merit during the stress test, as evaluated during the short characterization in the inner loop, is shown in Fig. 5. During DC and RF stress with small $P_{in}$ = 1 dBm, there is some degradation of the saturated power and the linear gain. This is not surprising considering that the critical voltage of these devices in the OFF state is around 60 V but at this point, the devices are biased in a semi-ON state with some self-heating. Beyond $P_{in}$ = 20 dBm, the output power starts degrading more rapidly. From the beginning to the end of the experiment, a loss of $P_{out}$ of about 2 dBm is observed. Interestingly, the linear gain appears rather stable after its initial drop.

Insight into the changes that are taking place in the device is obtained from the DC characterization that is also performed in the inner loop. Fig. 6 shows the evolution of $I_{Dmax}$, $R_S$, $R_D$ and $I_{Goff}$ as a function of time. The top axis of the figure indicates the DC/RF stress conditions. Under initial DC stress and under RF stress with $P_{in}$ = 1 dBm, there is a noticeable increase in $I_{Goff}$, revealing some degree of device degradation. As we increase the input power to 20 dBm, there is a sudden rise in $I_{Goff}$ of an order of magnitude. At the same time, $I_{Dmax}$ and $R_D$ start to degrade visibly, and the degradation accelerates as $P_{in}$ is increased. However, the source

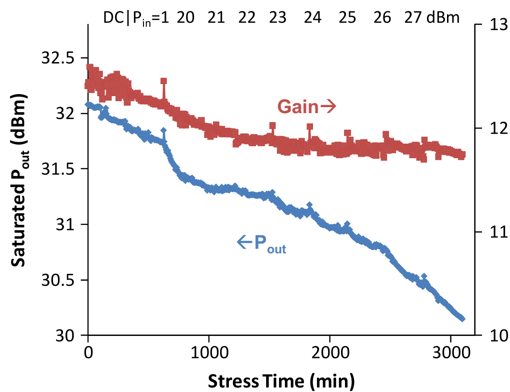


**Fig. 5.** Evolution of $P_{out}$ and $G_{lin}$ during the experiment of Fig. 4. The measurements were performed in the inner loop (short characterization in Fig. 1 right) with the device at $T_{base}$ = 50 °C.

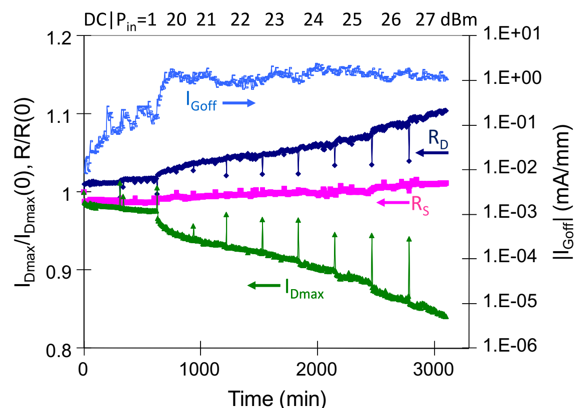


**Fig. 6.** Evolution of $I_{Dmax}$, $R_S$, $R_D$, and $I_{Goff}$ during the experiment of Fig. 4 as evaluated in the inner loop at 50 °C.

resistance changes very little throughout the experiment. In Fig. 6, spikes in $I_{Dmax}$ and $R_D$ can be seen between $P_{in}$ steps. These spikes are due to the detrapping period that we introduce when transitioning to a new stress condition through the outer loop (right in Fig. 1). This short detrapping phase produces a partial recovery in $R_D$ and $I_{Dmax}$. This suggests that stress is introducing significant trapping in the device. The fact that the original values of $R_D$ and $I_{Dmax}$ are not reached after electron detrapping indicates that there is also additional "permanent" degradation that is introduced as a result of stress.

The more detailed characterization that is performed in the outer loop confirms this interpretation. Fig. 7 shows current collapse, permanent $I_{Dmax}$ (in a fully recovered condition after the thermal detrapping step shown in Fig. 1), and saturated output power as measured at room temperature at the transition point between $P_{in}$ values. As it can be seen, all of these device parameters start to sharply degrade beyond $P_{in}$ = 20 dBm. The increase in current collapse shows that traps are being created as a result of RF stress. The permanent drop in $I_{Dmax}$ indicates that additional non-trapping related degradation of the device is taking place.

Fig. 8 shows the output power characteristics before and after the stress experiment. Although the small-signal gain (at $P_{in}$ = 10 dBm) was slightly decreased, the saturated output power (at $P_{in}$ = 23 dBm) shows much larger degradation. This is understandable in light of the other results obtained in this work. At low $P_{in}$, the degradation of $P_{out}$ reflects the degradation of $G_{lin}$ which is not as severe as that of $P_{outsat}$. This is consistent with the lack of degradation of $R_S$. For the high $P_{in}$, that leads to the saturated power condition, in addition to the drop in gain, there is a drastic reduction in $I_{Dmax}$ that further contributes to the degradation in $P_{outsat}$. There are two components to $I_{Dmax}$ degradation that are likely to propagate to $P_{outsat}$ degradation. The first one is the permanent irrecoverable degradation of $I_{Dmax}$ that is seen in Fig. 7. The second one is current collapse. At high $P_{in}$, the expansion of the RF load line towards the high $V_{DS}$ OFF-state imposes a large electric field on the device which induces current collapse. This, further contributes to a decrease in $I_{Dmax}$ and a decrease in $P_{outsat}$. The correlation between $P_{outsat}$ and $I_{Dmax}$ is very tight, as Fig. 9 shows. $I_{Dmax}$ in this figure includes both current collapse and permanent components as it was measured without a detrapping phase in the inner loop. A 1 dB degradation in saturated $P_{out}$ corresponds to a 9% degradation in $I_{Dmax}$. This close correlation between $I_{Dmax}$ and $P_{outsat}$ was also observed in our previous studies [22,25].

In order to understand the physics of failure in more detail, we have investigated the structural degradation of the device through a recently developed plan-view technique in which passivation and all metals at the surface are removed after stress [29,30].

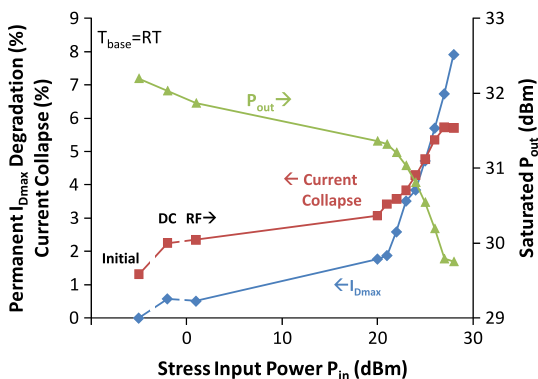


**Fig. 7.** Evolution of current collapse, permanent $I_{Dmax}$, and output power during the experiment of Fig. 4. These measurements were taken in the outer loop (full characterization in Fig. 1, right) at $T_{base}$ = RT.

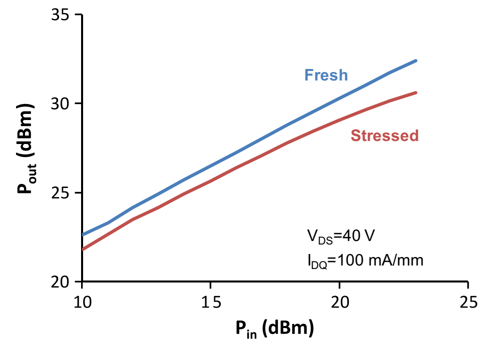


**Fig. 8.** Change in output power characteristics before and after the stress test in Fig. 4. The bias condition is $V_{DS}$ = 40 V and $I_{DQ}$ = 100 mA/mm, $T_{base}$ = 27 °C. (For interpretation of the references to colour in this figure legend, the reader is referred to the web version of this article.)

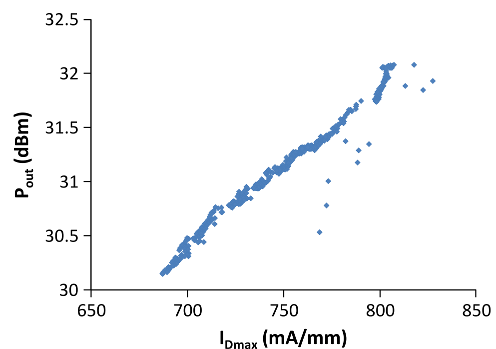


**Fig. 9.** Correlation between saturated $P_{out}$ and $I_{Dmax}$ degradation as evaluated in the inner loop at 50 °C. 1 dB degradation in saturated $P_{out}$ corresponds to 9% degradation in $I_{Dmax}$.

Fig. 10 shows plan-view SEM and AFM images of a centered-gate device that was stressed under similar conditions as in Fig. 6 and that degraded following a similar pattern. It can be seen that pits are formed along the drain side of the gate edge just as observed in devices stressed at high voltage in DC in the OFF-state [29,30]. This is consistent with the increase in $I_{Goff}$ and the changes in other DC figures of merit during the RF stress test that very closely map what is observed in high-voltage OFF-state DC stress experiments [12]. The overall pattern of degradation suggests that during high power RF stress, these devices are degrading as the dynamic load line swings through the high $V_{DS}$ region of the output characteristics plane.

Table 1 compares the degradation in high voltage DC OFF-state stress with that in RF power stress. For devices investigated in this section, very similar critical behavior in degradation of many device figures of merit is seen. Just as $I_{Dmax}$, $R_D$, $I_{Goff}$, and current collapse start to degrade beyond the critical voltage under OFF-state DC stress, similar degradation occurs beyond a critical input power under RF stress. In addition, similar pit formation at the drain side of the gate edge takes place in both cases.

## 4. Discussion

The results obtained in this work differ significantly from an earlier RF reliability study that we reported in Ref. [25]. That study was carried out in similar devices with two important differences. First, the devices in Ref. [25] came from a more rugged wafer that yields devices with an OFF-state critical voltage in excess of 80 V at 150 °C. Second, in the devices in Ref. [25] the gate is offset towards the source by 1 μm. In step-$P_{in}$ RF stress experiments, the pattern

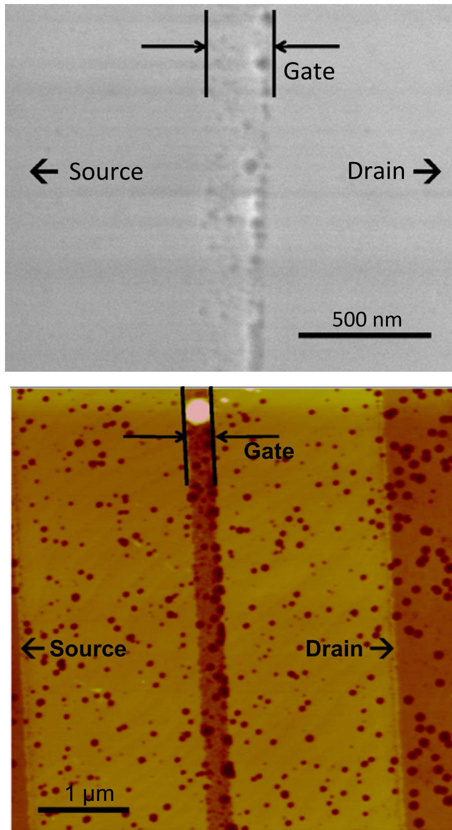


**Fig. 10.** Plan-view SEM (top) and AFM (bottom) images of a degraded device with centered gate stressed under RF. SiN passivation and gate and ohmic metals were removed to expose the semiconductor surface. The stress condition was similar to the experiment in Fig. 4. A linear array of pits is seen aligned with the drain-edge of the gate.

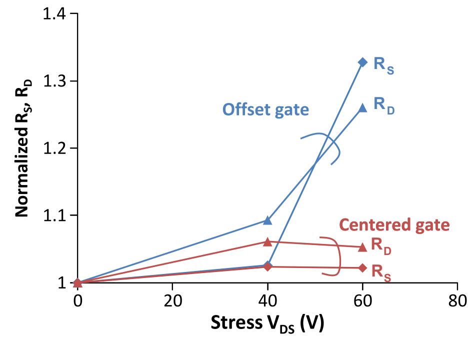


**Fig. 11.** Evolution of $R_S$ and $R_D$ under pulsed stress tests at room temperature of neighboring offset-gate and centered-gate devices. The pulse width is 500 μs and the duty cycle is 0.05%. 100 pulses were applied. The current level at the pulse was 950 mA/mm. Pulse stress under these conditions mimics well the RF degradation of the offset-gate devices. (For interpretation of the references to colour in this figure legend, the reader is referred to the web version of this article.)

of degradation observed in Ref. [25] has a lot of in common with what we report here. As in the present work, in Ref. [25], as $P_{in}$ increases, $P_{out}$, $I_{Dmax}$ and $R_D$ degrade. In contrast with the present work, in Ref. [25], at high $P_{in}$, $G_{lin}$ continues to degrade, $I_{Goff}$ does not change at all, and most surprising, $R_S$ increases in a dramatic way. The marked difference between the patterns of degradation in Ref. [25] and in the present work is accentuated by the absence of any structural surface degradation after RF stress in the devices in Ref. [25], even on the source side. Both here and in Ref. [25], the experiments were replicated in several MMICs with substantially similar results. It then seems clear that in Ref. [25] we are in front of a different degradation mechanism from the one observed in the present work. This is also summarized in Table 1.

At least partly responsible for the different degradation behavior of the devices here and in Ref. [25] is the gate placement. This has been verified through measurements in a separate wafer with a similar structure and process that contains both centered and offset gate FETs. In Ref. [25] we showed that we could replicate the observed pattern of RF degradation by applying high power pulses. We have performed similar pulsed stress experiments with high $V_{DS}$ and $I_D$ on neighboring offset-gate and centered-gate devices from a separate wafer. As shown in Fig. 11, we found that the device with centered gate does not exhibit any increase in $R_S$ under high power pulse stress though it exhibits some $R_D$ degradation. However, a neighboring device with an offset-gate shows a large increase in the source resistance after high-power pulse stress (Fig. 11). The large increase in $R_S$ in the offset-gate device is consistent with the $R_S$ increase during the high compression RF stress of [25].

Our research reveals that devices with different gate placement in the source–drain gap are affected by different degradation mechanisms under RF stress. In the present devices, the dominant degrading factor appears to be the high drain voltage that the device periodically experiences as it cycles through the dynamic loadline. The RF degradation mechanism is similar to that under high-voltage OFF-state DC stress. In the offset-gate devices in Ref. [25], we hypothesize that simultaneous occurrence of high current and high voltage degrades the device. This is unique to RF stress. The specific physical origin of the peculiar degradation of the offset gate devices in Ref. [25] still remains to be understood.

A higher level conclusion from our work is that in general, the ability of DC stress to assess the RF reliability of GaN HEMTs is at best problematic. While in some devices under carefully selected conditions there might be a correlation between RF and DC degradation, there are clear instances in which no DC conditions are capable of mimicking the degradation that is produced under RF stress.

## 5. Conclusion

We have investigated the RF degradation of GaN HEMTs with gate centered in the source–drain gap. These devices exhibit a pattern of degradation that matches what is commonly observed

**Table 1**
Summary of degradation in DC high voltage OFF-state stress and RF power stress for centered (this work) and offset gate devices [25].

| | HV OFF-state DC | RF power centered gate | RF power offset gate |
|---|---|---|---|
| $I_{Dmax}$ | ↓ Beyond $V_{crit}$ | ↓ Beyond $P_{in-crit}$ | ↓ Beyond $P_{in-crit}$ |
| $R_D$ | ↑ Beyond $V_{crit}$ | ↑ Beyond $P_{in-crit}$ | ↑ Beyond $P_{in-crit}$ |
| $R_S$ | Small increase | Small increase | ↑↑Beyond $P_{in-crit}$ |
| $I_{Goff}$ | ↑ Beyond $V_{crit}$ | ↑ Beyond $P_{in-crit}$ | No change |
| Current collapse | ↑ Beyond $V_{crit}$ | ↑ Beyond $P_{in-crit}$ | ↑ Beyond $P_{in-crit}$ |
| Permanent $I_{Dmax}$ | ↓ Beyond $V_{crit}$ | ↓ Beyond $P_{in-crit}$ | ↓ Beyond $P_{in-crit}$ |
| Pits under drain end of gate | Yes | Yes | No |
| Pits under source end of gate | No | No | No |

under high-voltage OFF-state DC stress. This behavior contrasts with devices with the gate offset towards the source that were studied earlier. Under RF stress, those devices appear to degrade through a different mechanism. The results from high-power pulse stress are consistent with a hypothesis that offset-gate devices degrade as a consequence of the simultaneous application of high current and high voltage. In this instance, DC stress is a poor predictor of RF reliability.

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