Sub-30 nm InAs Quantum-Well MOSFETs with Self-Aligned Metal Contacts and Sub-1 nm EOT HfO_2 Insulator

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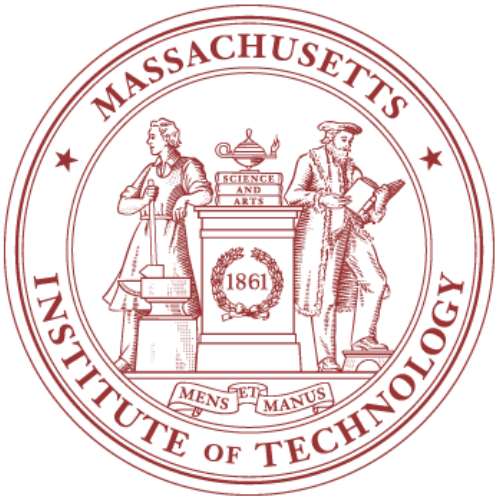
December 12, 2012

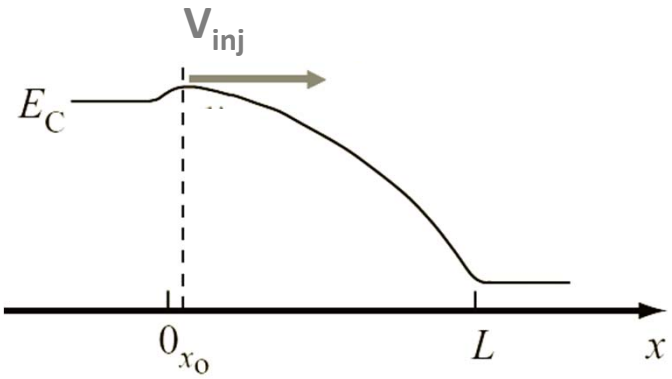


Sponsors: FCRP-MSD Center, Intel Corp.

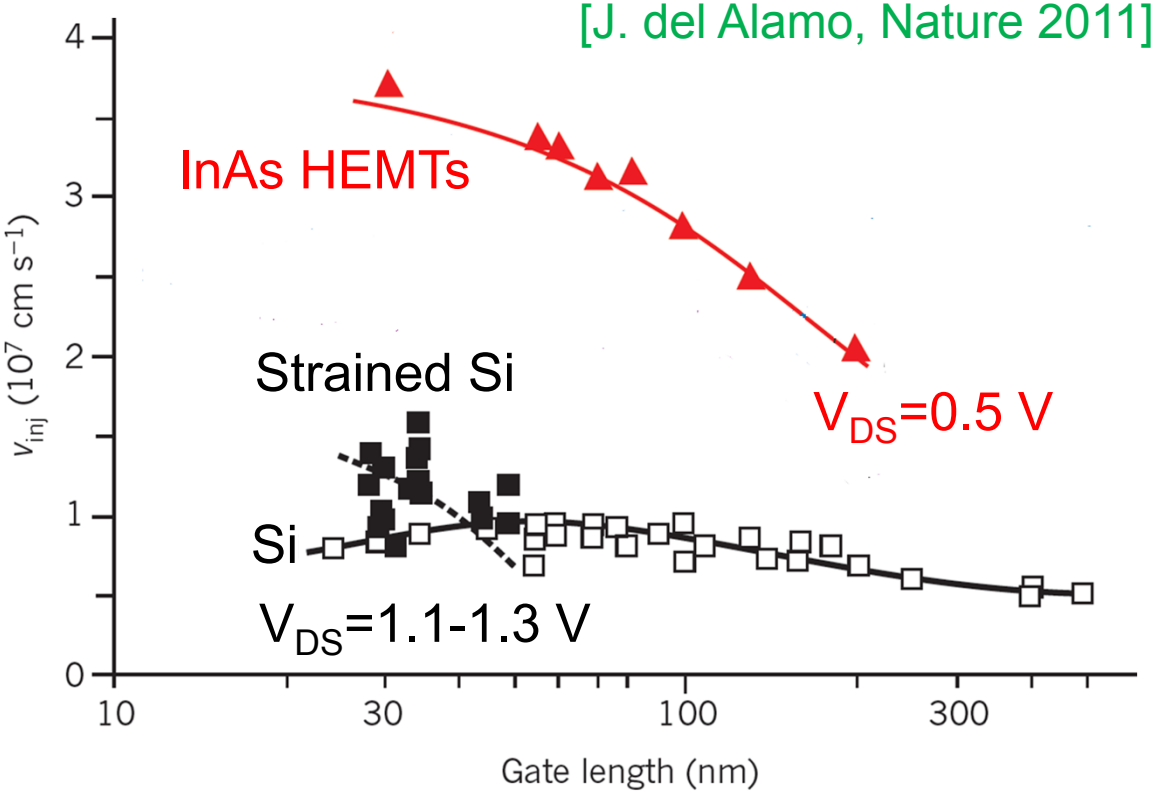
Motivation

- Superior electron transport properties in InAs and InGaAs material systems
  - ~10X mobility *vs*. Silicon
  - Extraordinary electron velocity

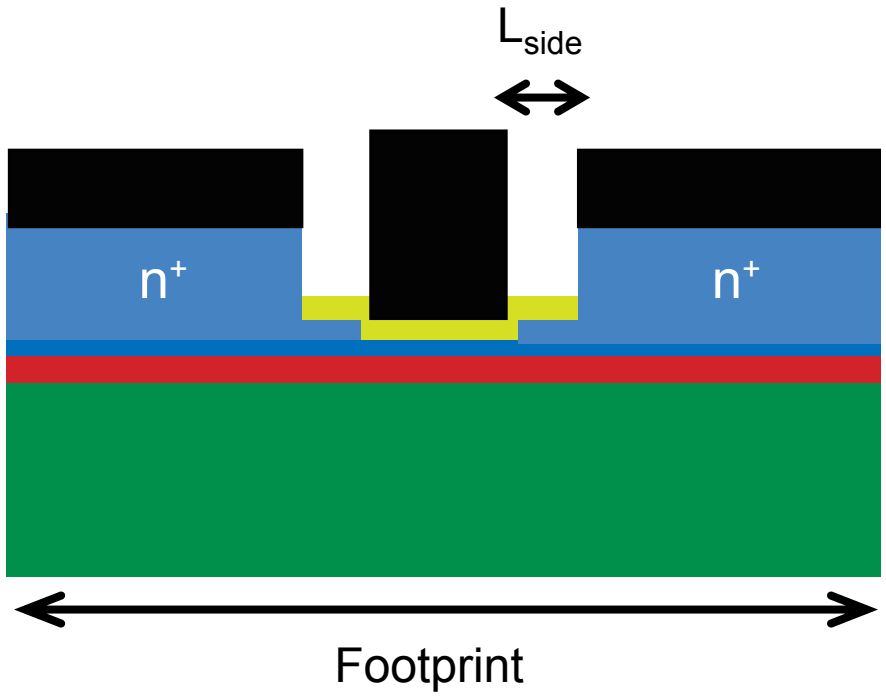
$I_{d\text{-}sat} = Q_{i\_xo} \times v_{inj}$



[J. del Alamo, Nature 2011]

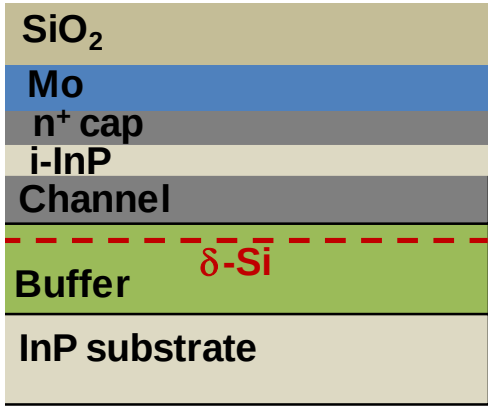


Goal: Self-aligned III-V QW-MOSFETs



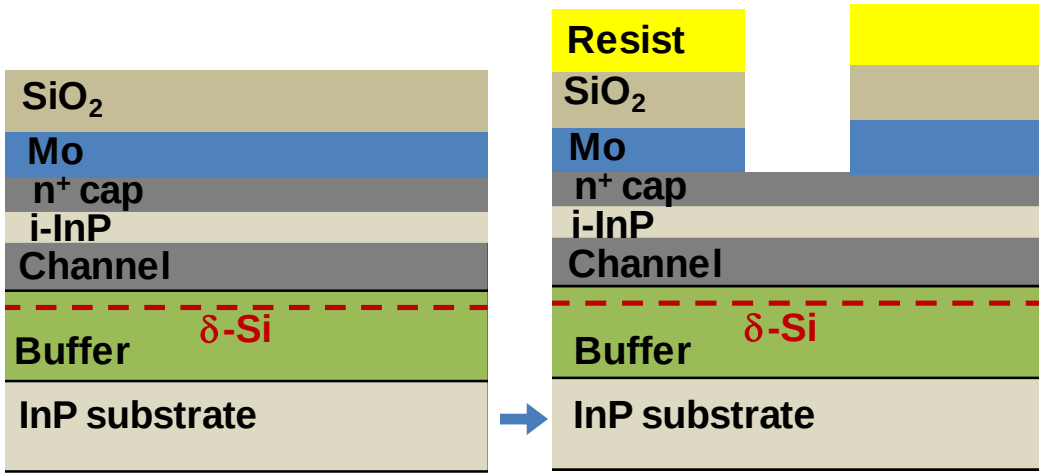
- Deeply scaled channel and barrier
- Architecture: Self-aligned contact
- Process integration: towards Si-MOS-compatible processes and materials

Device fabrication



- **Sputtered Mo contact**
- **CVD SiO_2 hard mask**
- **Mesa isolation**

Device fabrication



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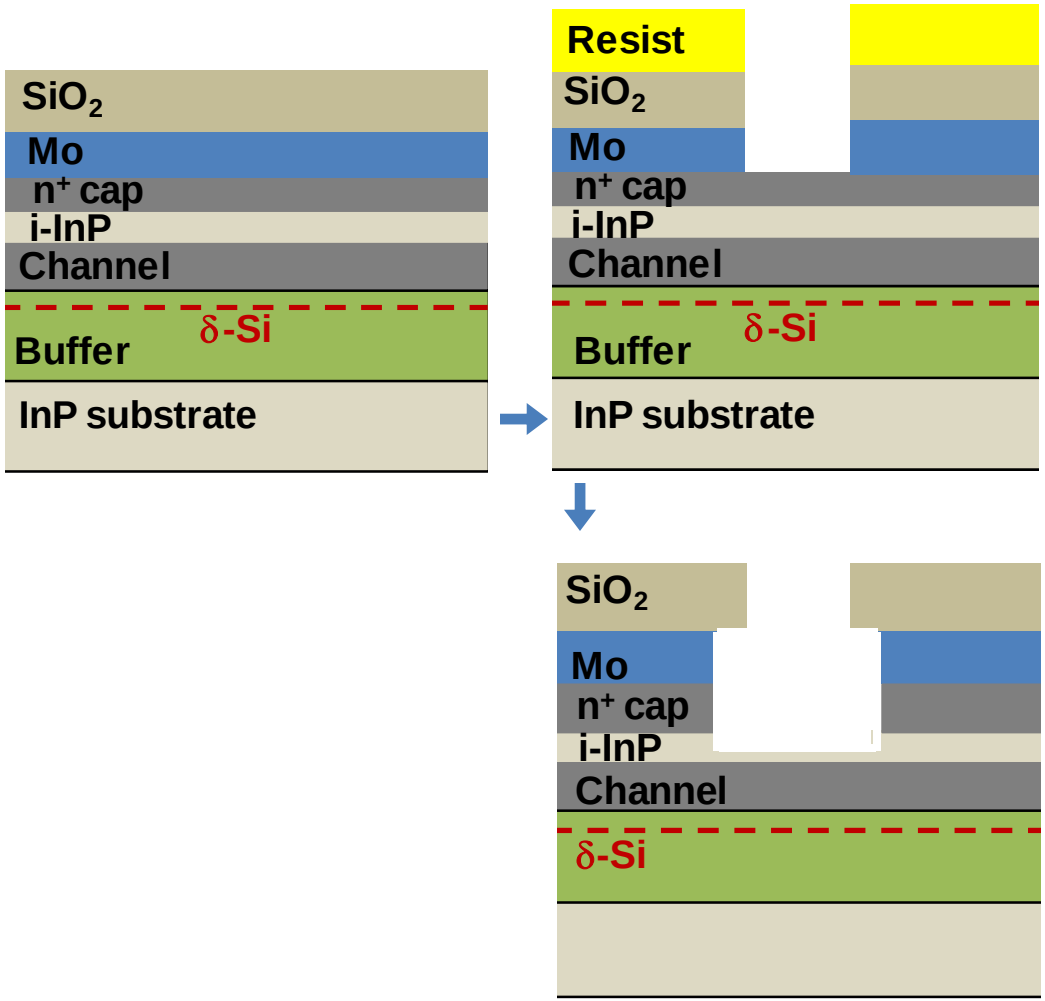
- CVD SiO_2 hard mask
- Mesa isolation
- **Gate lithography**
- **Gate recess by RIE SiO_2/Mo**

Device fabrication



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- CVD SiO_2 hard mask
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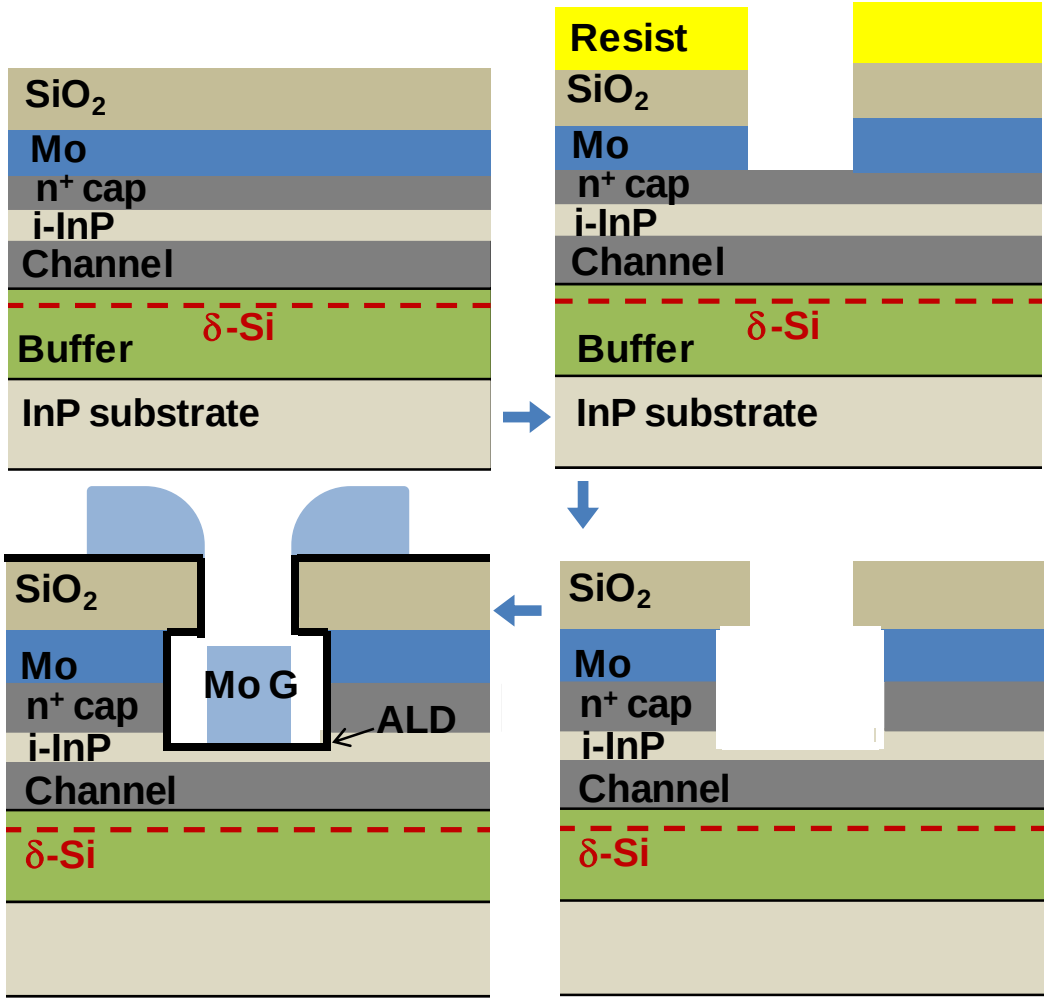
- **Damage annealing ***
- **Cap wet etch; Mo pulled-in**
- **Digital etching of InP**

* [Lin, APEX 2012]

Device fabrication



- Sputtered Mo contact
- CVD SiO_2 hard mask
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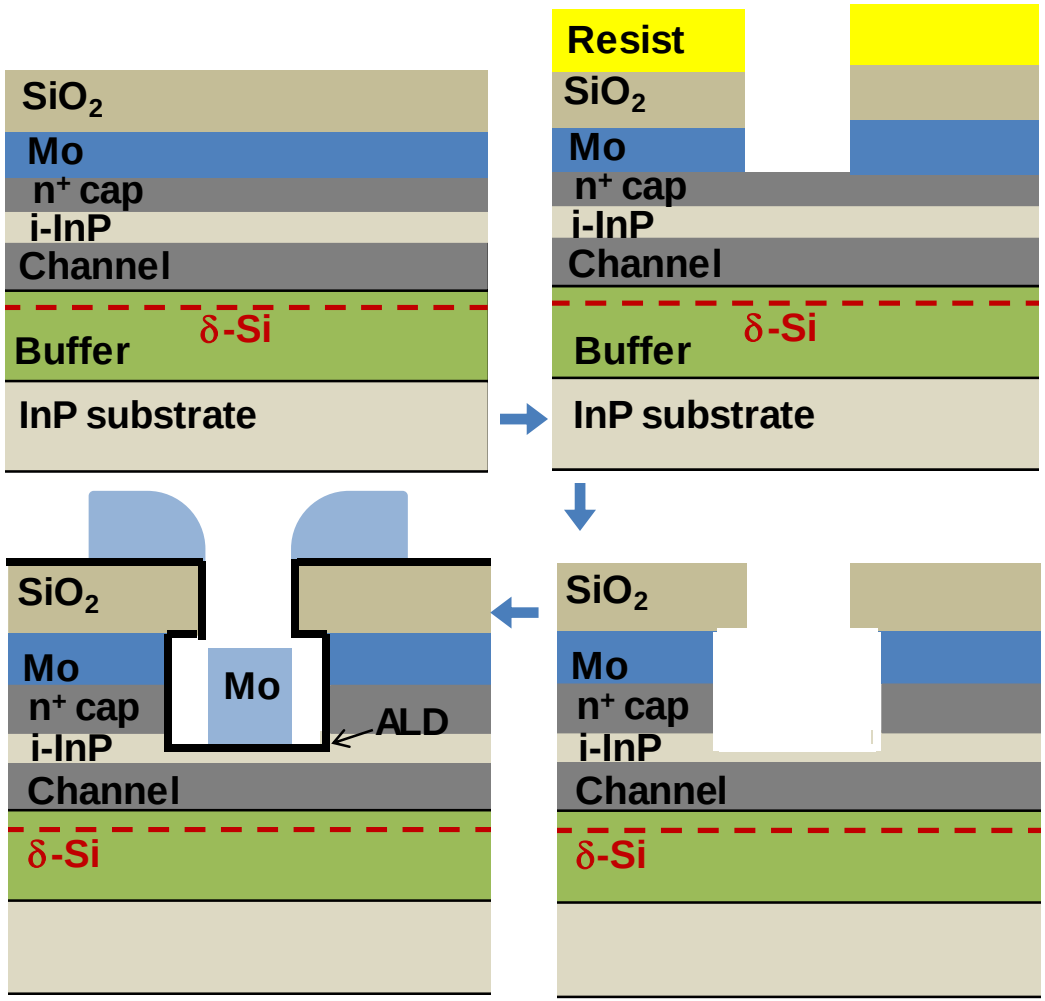
- Digital thinning of InP
- **ALD gate dielectric deposition**
- **Mo gate evaporation**
- **Gate head photo and pattern**
- **Pad formation**

Device fabrication



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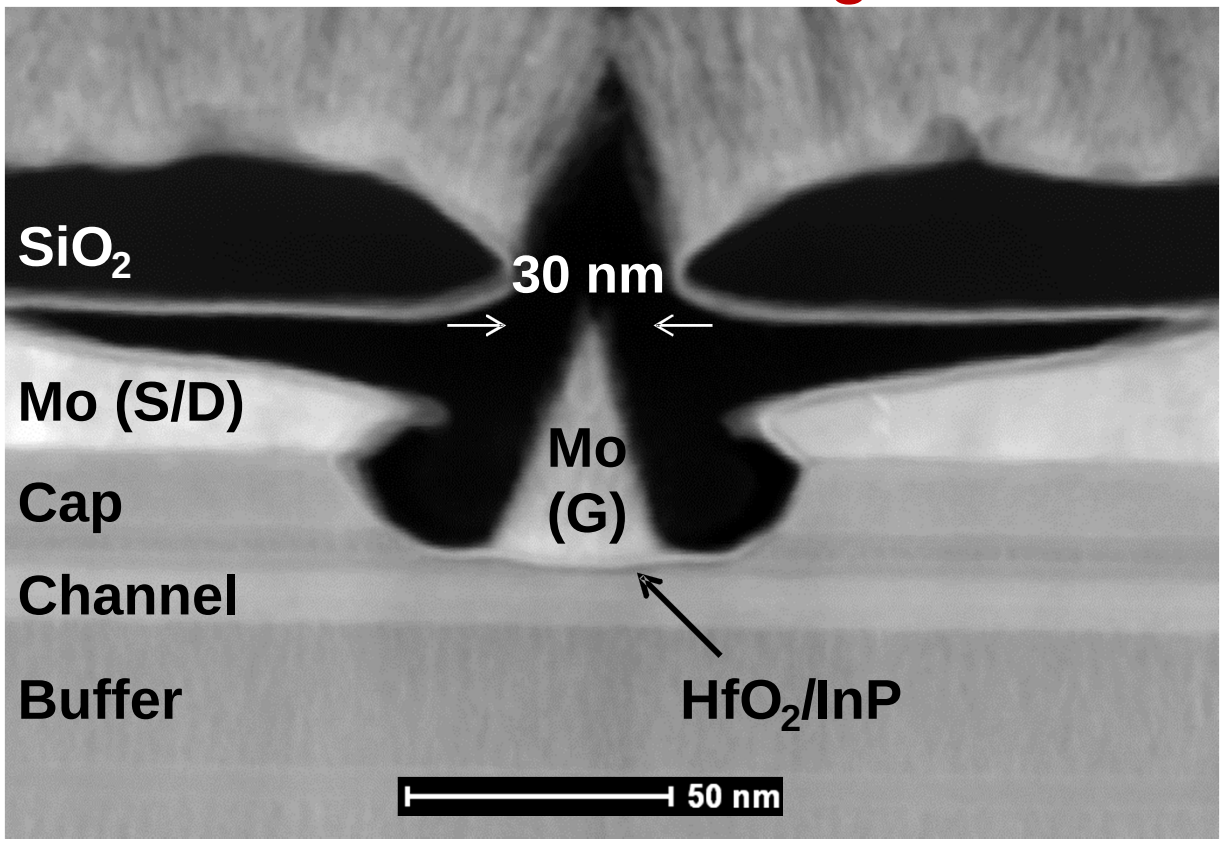
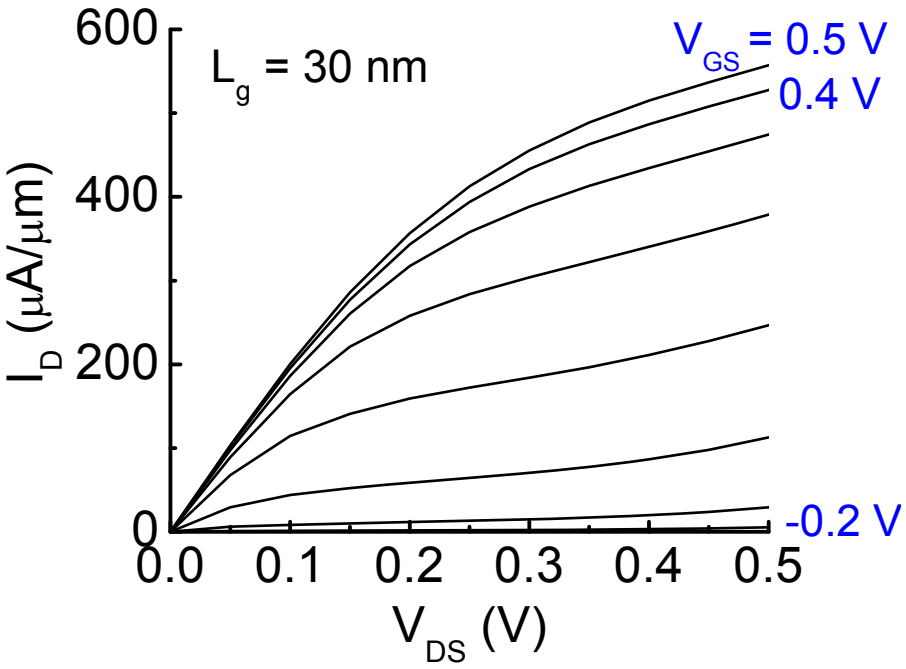
- **Self-aligned**
- **InP exposed last**
- **Low thermal budget**
- **Au-free (Front-end)**
- **Lift-off free (Front-end)**

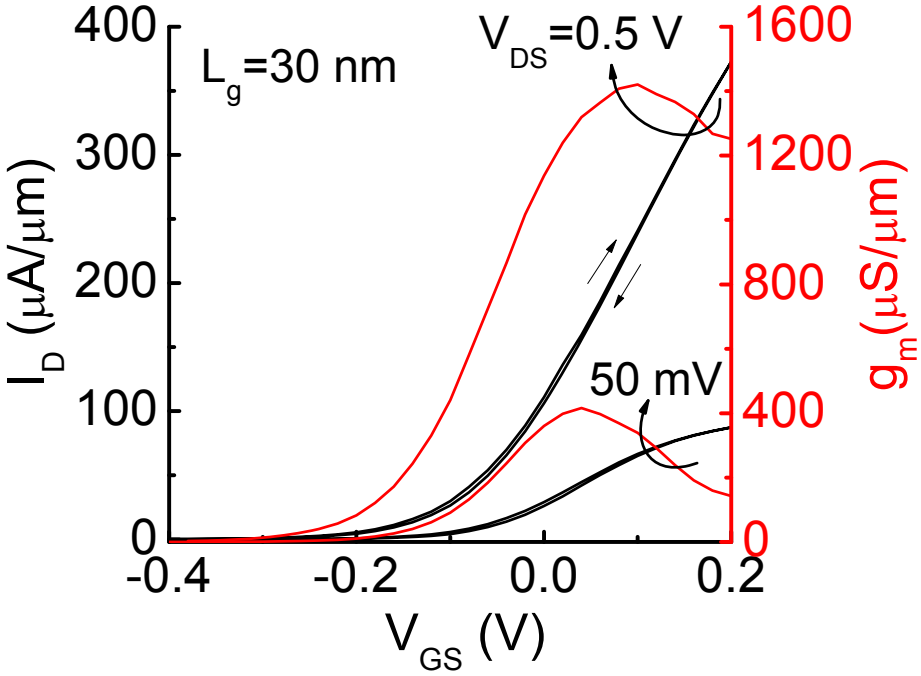
QW-MOSFET: L_g=30 nm



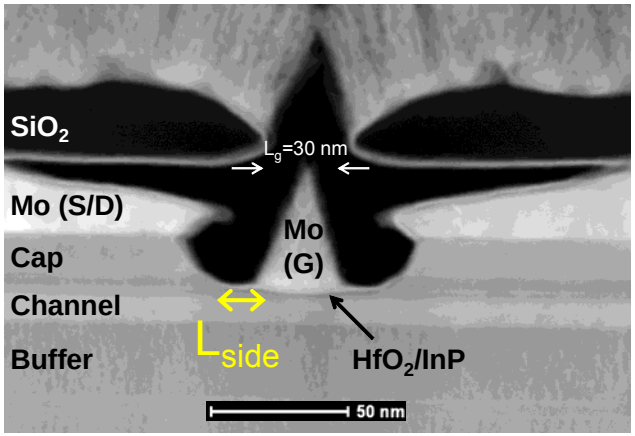
- Channel (total t_{ch}=10 nm): 2 nm InAs clad by 3 and 5 nm $In_{0.7}Ga_{0.3}As$
- InP barrier thinned by digital etch
- Barrier InP =1 nm, HfO_2 =2 nm [including barrier: EOT~ 0.8 nm]
- Low-ρ Mo: $t_{Mo,S/D}$ =30 nm, R_{sh}=5 Ω/□
- Contact to gate spacing = 20~30 nm

QW-MOSFET: L_g=30 nm

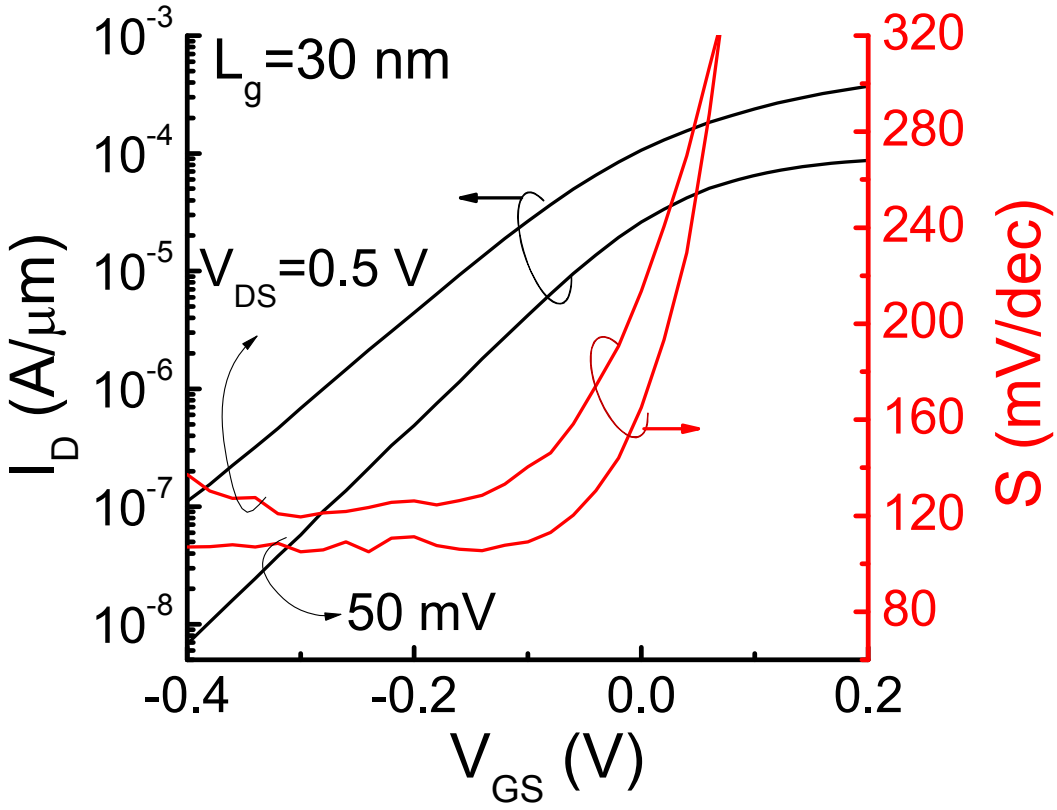




- $g_{m,max}$ = 1.4 mS/μm at V_{DS}=0.5 V
- Little hysteresis (< 10 mV)
- R_{on}=470 Ω.μm, R_{sd}=450 Ω.μm (mainly attributed to L_{side})

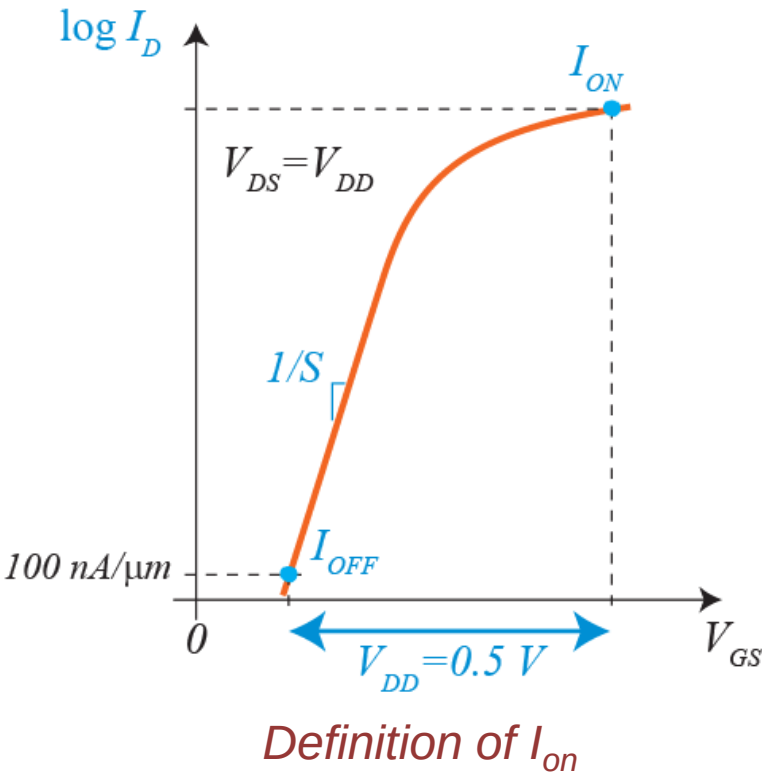


QW-MOSFET: L_g=30 nm subthreshold characteristic

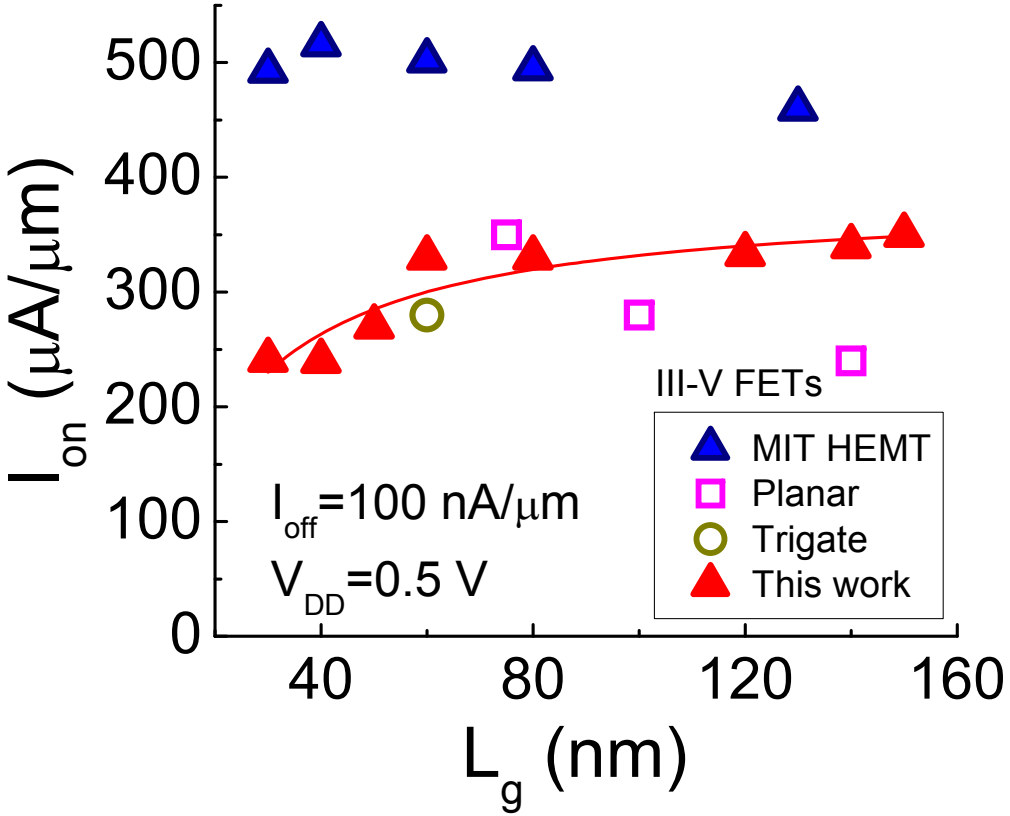


- S_{min}=114 mV/dec at V_{DS}=0.5 V, DIBL=230 mV/V
- Nearly constant S throughout subthreshold region
- I_g<1 nA/μm over entire voltage range

Scaling and benchmarking: ON current

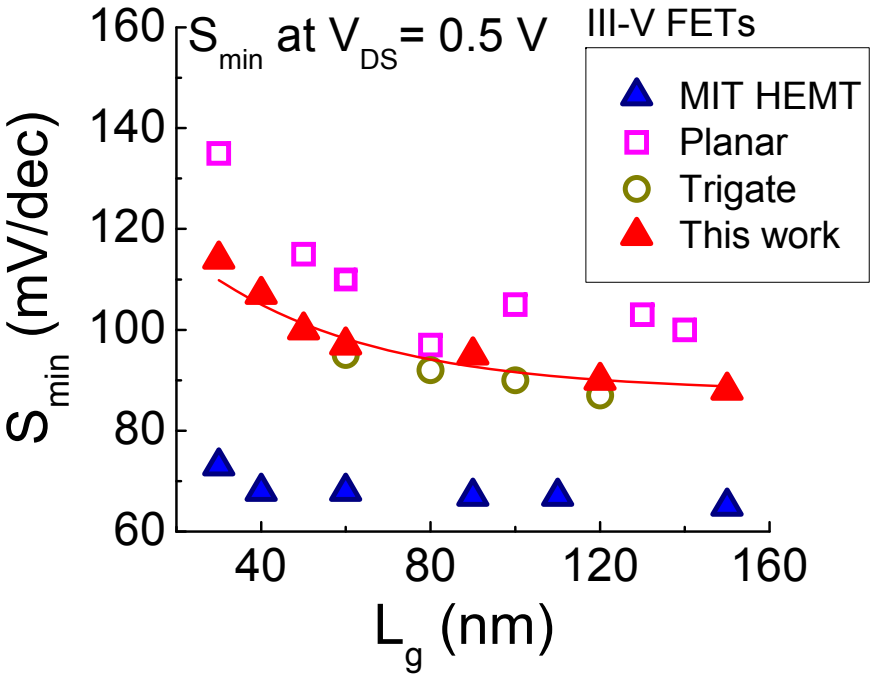


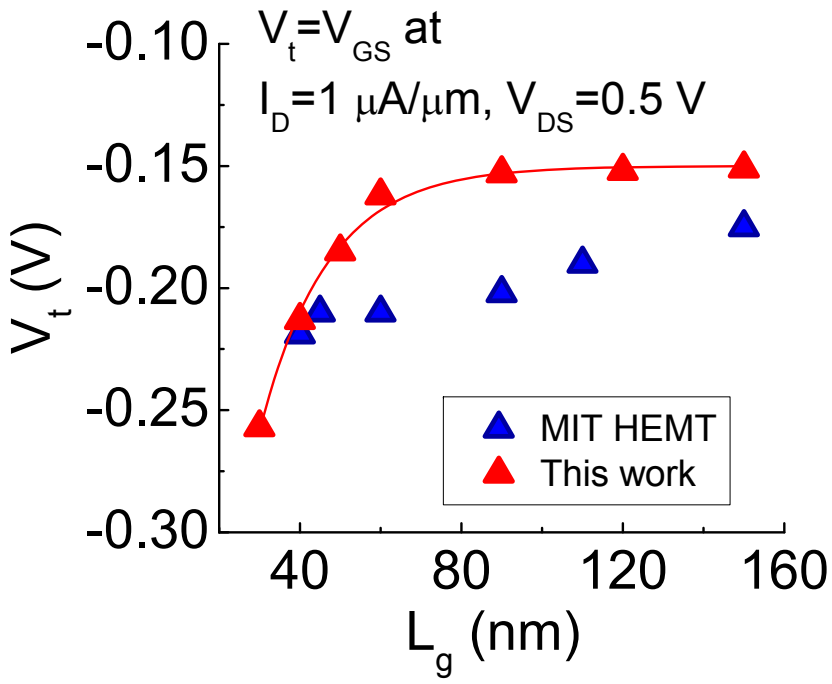
Definition of I_{on}



- Superior behavior to any planar III-V MOSFET to date
- Matches performance of III-V Trigate MOSFETs [Radosavljevic, IEDM 2011]

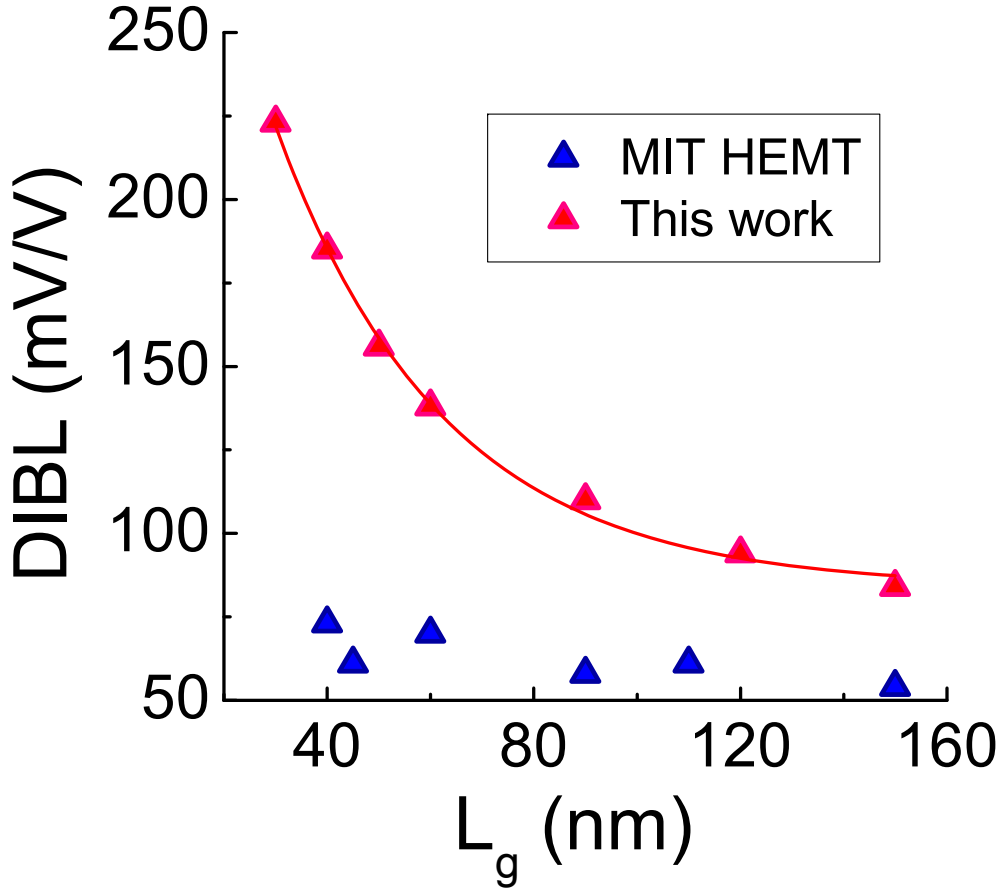
Scaling and benchmarking: Subthreshold swing and V_t roll-off





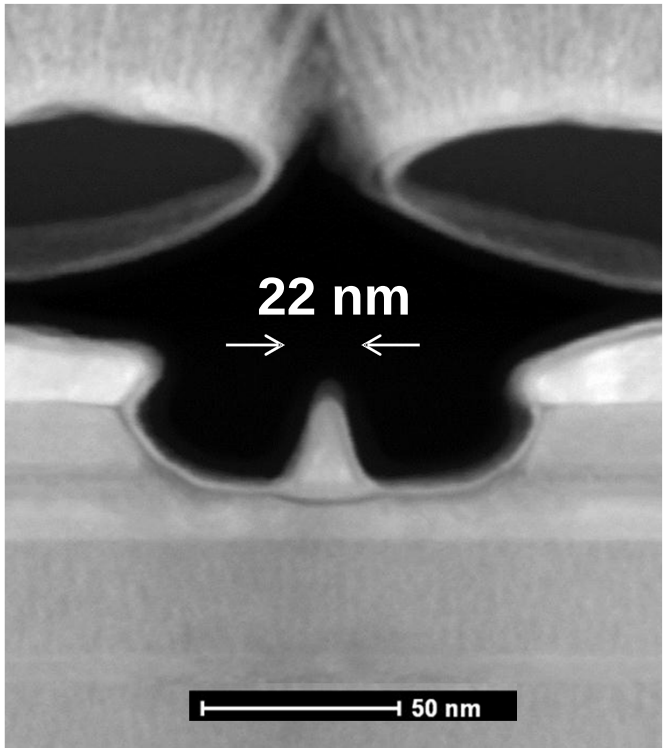
- S_{min} superior to all planar III-V MOSFETs to date
- Matches III-V Trigate MOSFET [Radosavljevic, IEDM 2011]
- V_t roll-off starts at L_g ~50 nm

DIBL

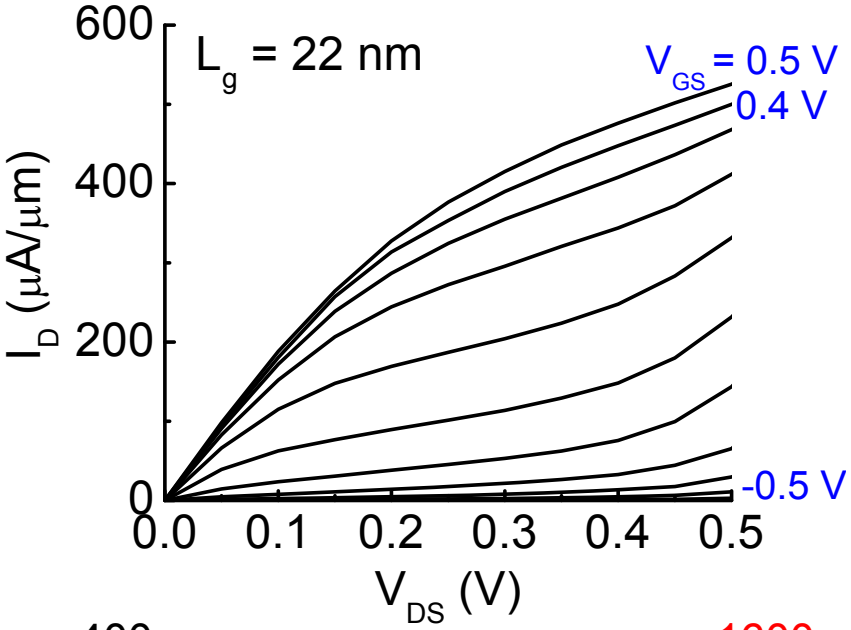


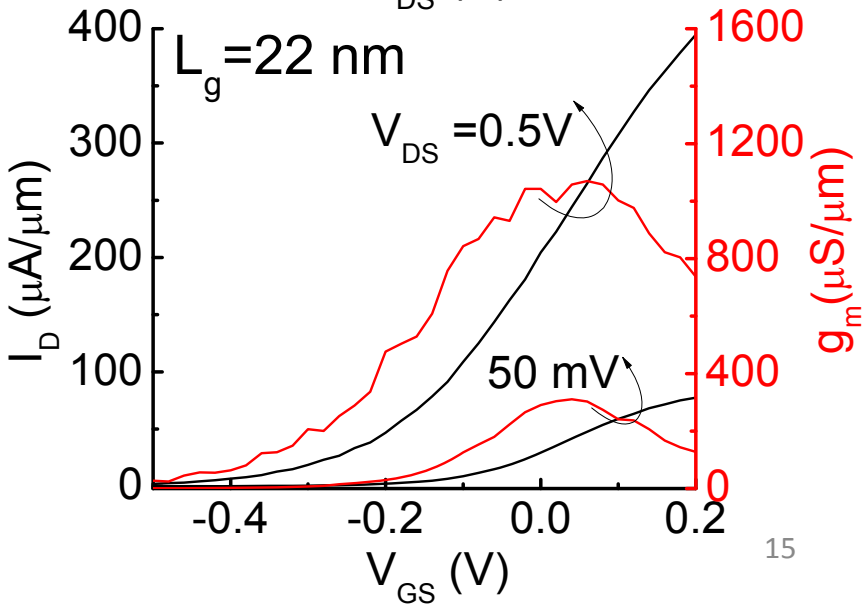
- DIBL= 230 mV/V for L_g=30 nm
- Related to residual RIE damage and the heterostructure

QW-MOSFET: L_g=22 nm



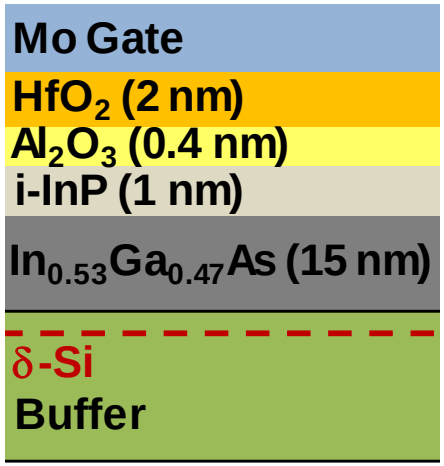
- Functional device with L_g =22 nm
- $g_{m,\,max}$ = 1.1 mS/μm at V_{DS}=0.5 V



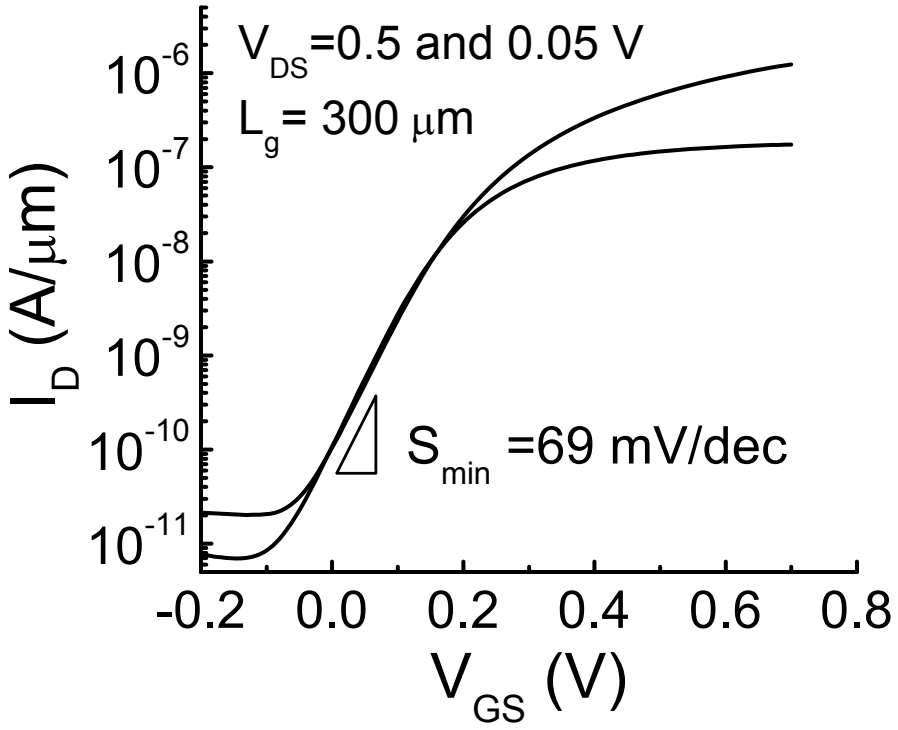


Dielectric/barrier scaling

Long-channel $In_{0.53}Ga_{0.47}As$ QW-MOSFET

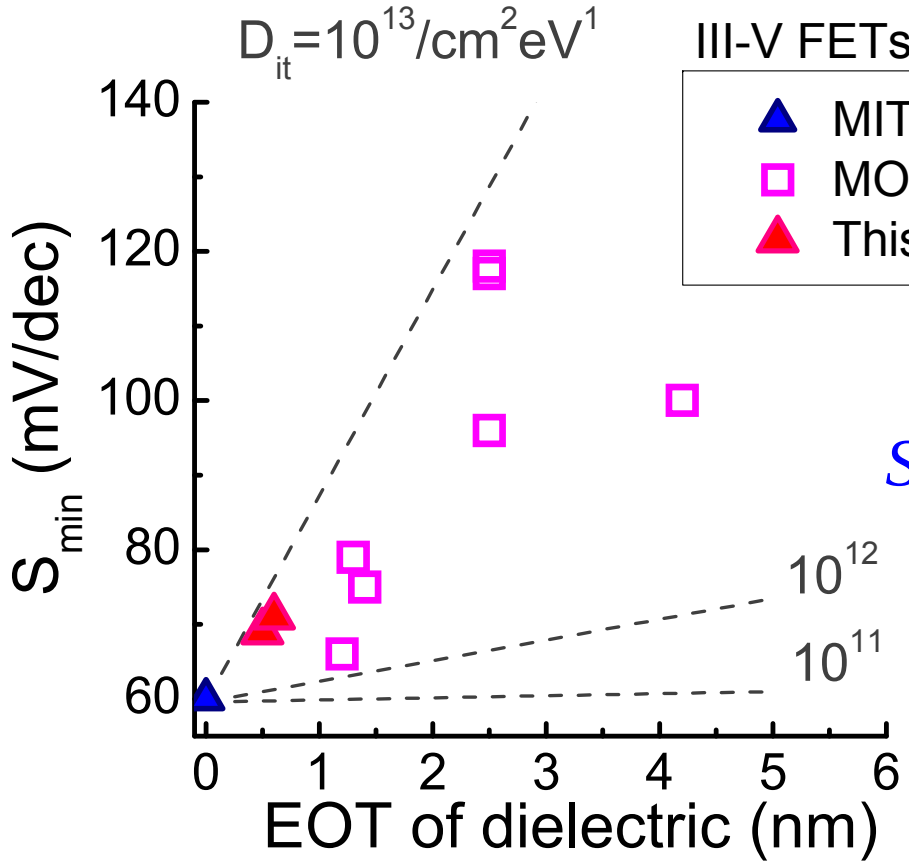


Cross section:
Intrinsic portion of the device



- Fresh InP surface exposed right before high-k deposition
- Al_2O_3 (0.4 nm) + HfO_2 (2 nm) [EOT of deposited insulator layer ~0.6 nm]
- InP thinned to ~ 1 nm [Gate-Channel EOT~0.9 nm]

Benchmarking: Long-channel subthreshold swing on planar MOSFETs



$$S_{\min} = 60\left(1+\frac{qD_{it}}{C_{ox}}\right)\ \mathrm{mV/dec}$$

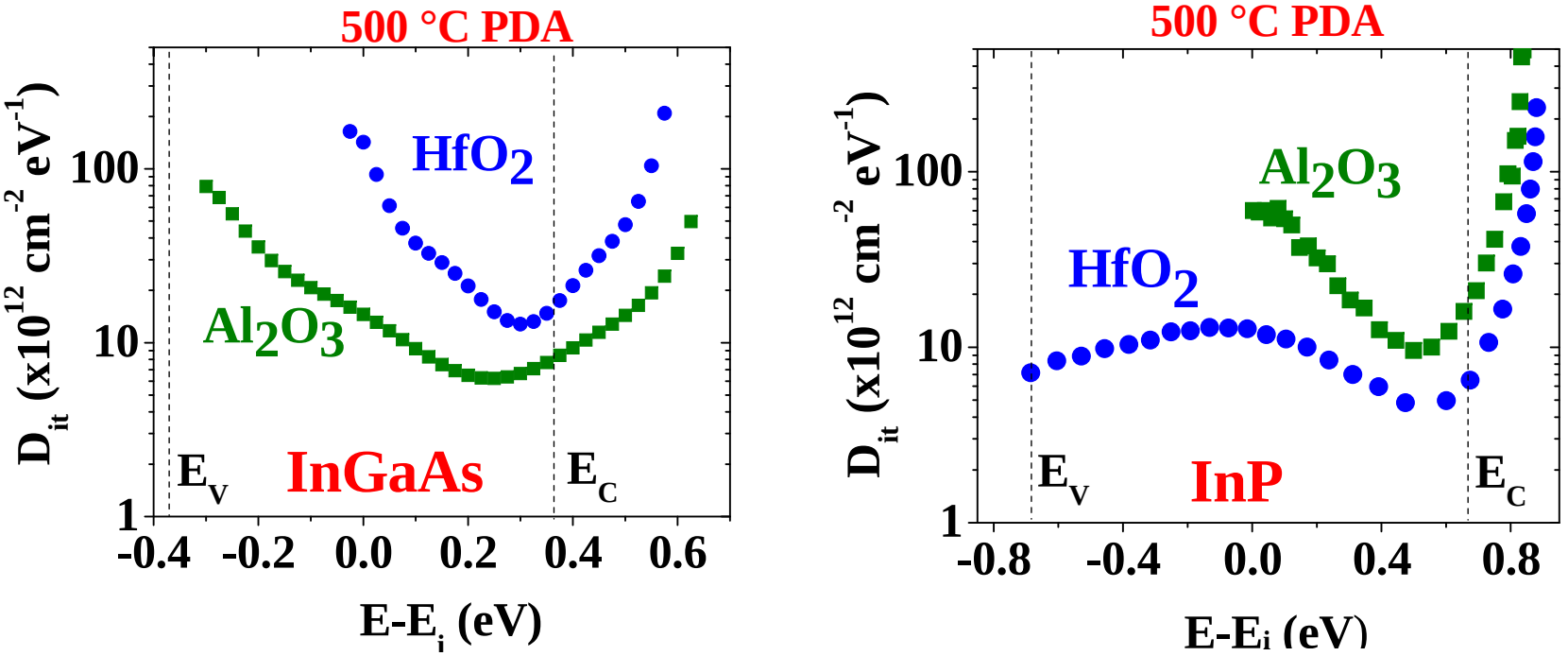
EOT of dielectric refers to the deposited insulating layer

- Close to lowest S_{min} reported in any III-V MOSFET: 66 mV/dec [EOT=1.2 nm] [Radosavljevic, IEDM 2011]

HfO_2 vs. Al_2O_3

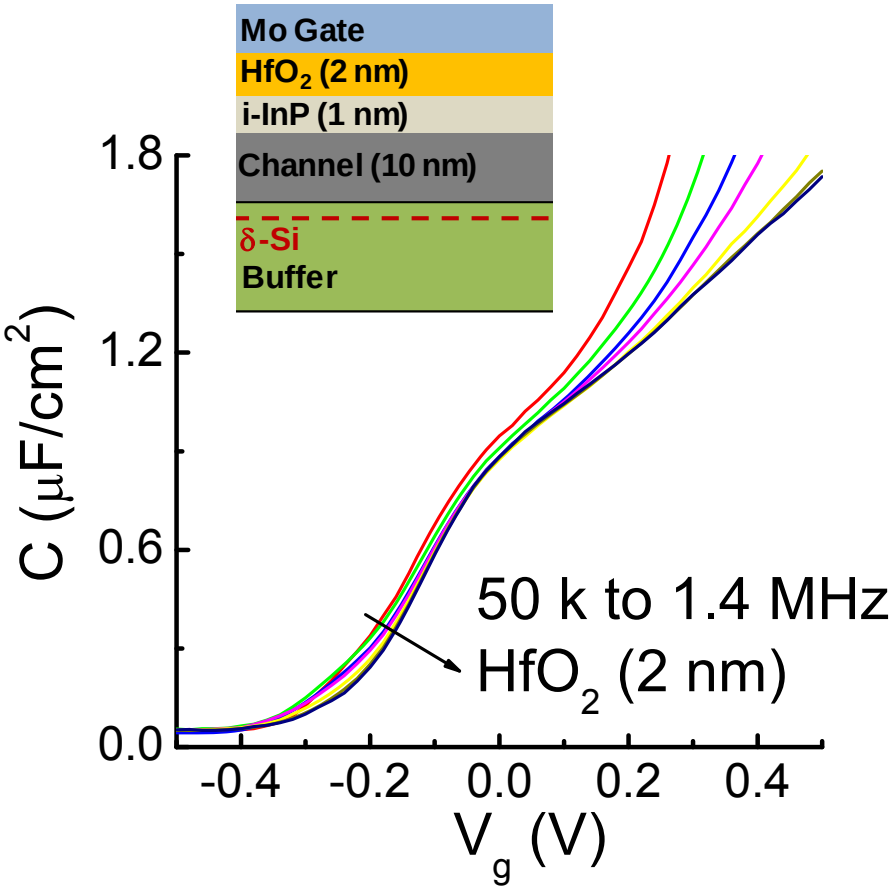
Recent study at U. Texas at Dallas:

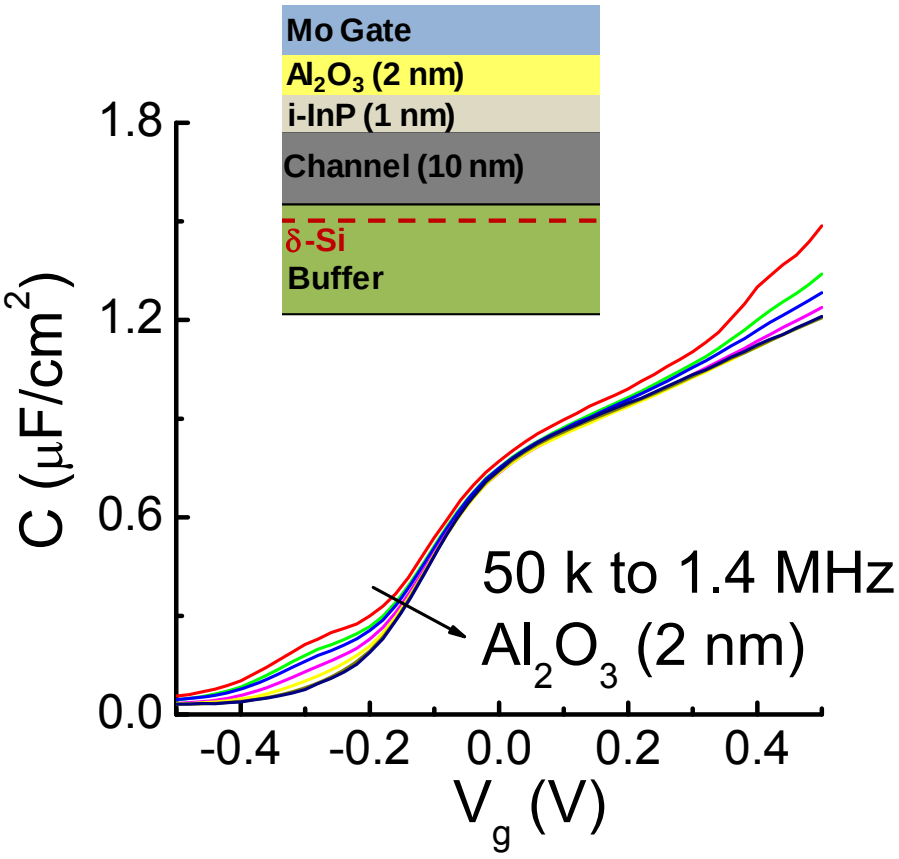
- HfO_2 on InP yields lower D_{it} than Al_2O_3



[R. Galatage, R.M.Wallace, E.M.Vogel - UT Dallas]

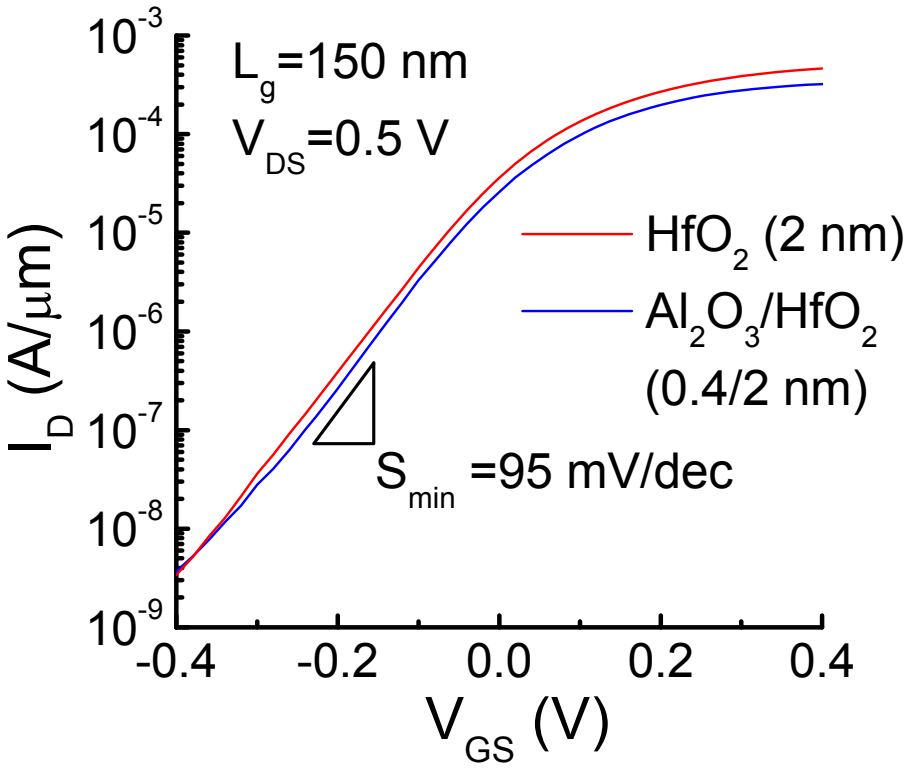
HfO_2 vs. Al_2O_3

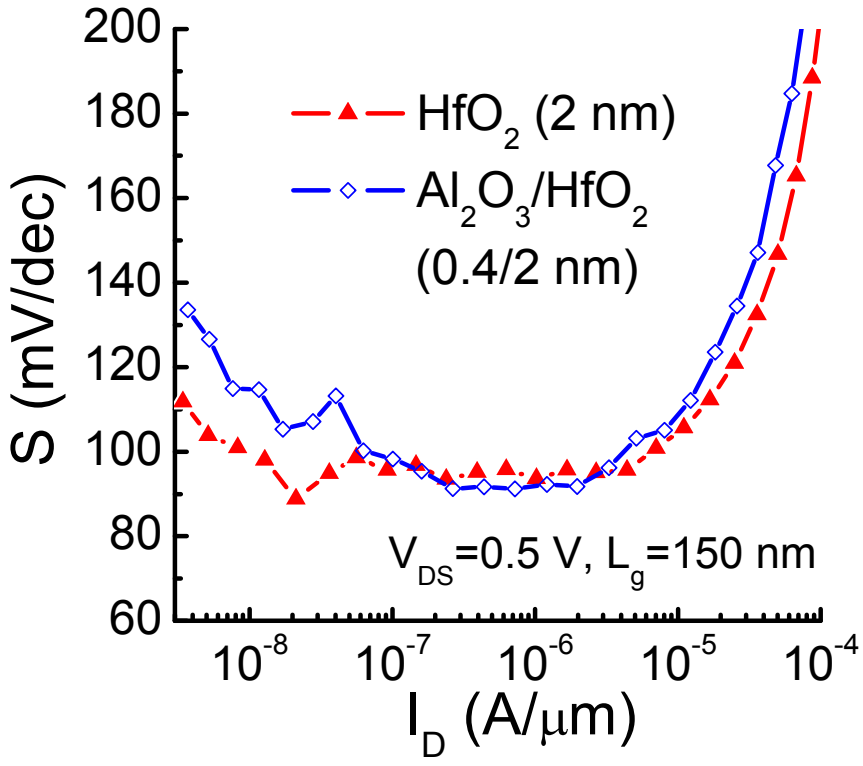




- Split C-V measurement on L_g = 20 μm
- Lower dispersion for HfO_2 below threshold

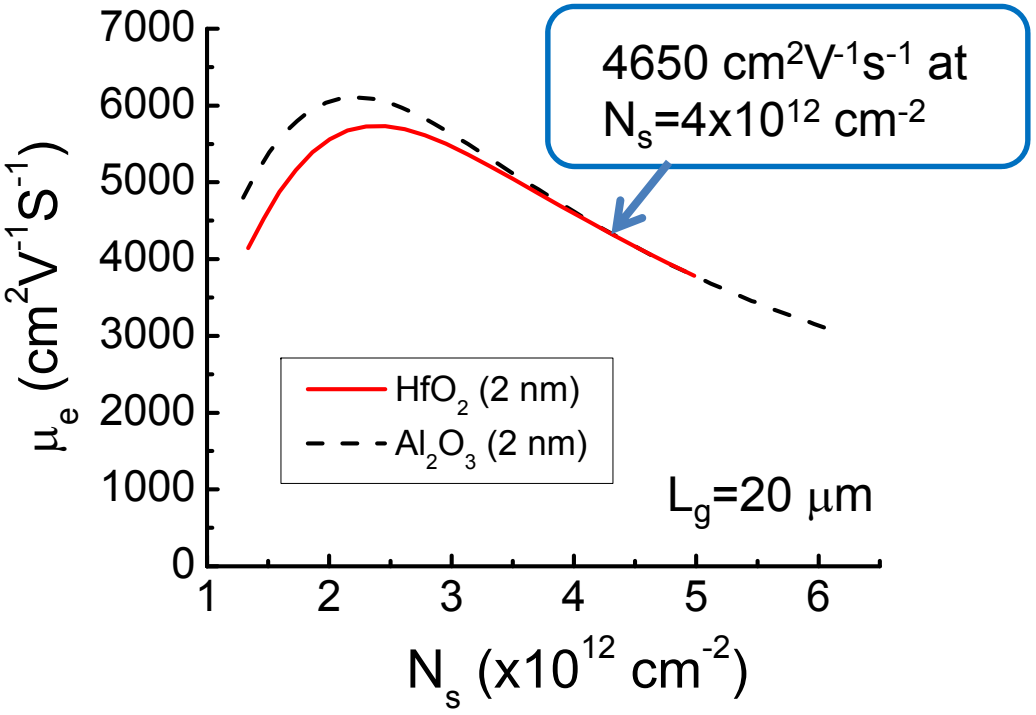
HfO_2 vs. Al_2O_3

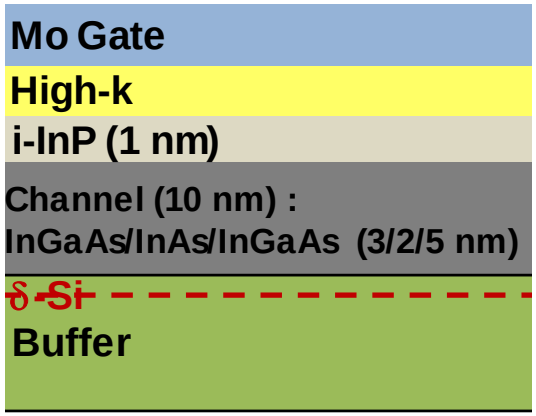




- First demonstration of HfO_2 directly on InP for InAs QW-MOSFET
- Steeper subthreshold swing at L_g=150 nm at low V_{GS}
- Lower EOT

Mobility in Long QW-MOSFETs





- Mobility extracted by split C-V method
- N_s not corrected by D_{it}
- Channel design beneficial to maintain high mobility:
  - Undoped channel
  - InAs-rich channel
  - Buried-channel design

Conclusions

- Novel self-aligned gate-last MOSFET architecture:
  - Self-aligned gate to contact metals (L_{side}~20-30 nm)
  - Improved Si-MOS process compatibility
  - Fresh InP surface exposed right before high-k deposition
  - Deeply scaled dielectric
- Outstanding performance and short-channel effects in devices with L_g=30 nm
- Demonstrated subthreshold swing of 69 mV/dec and mobility of 4650 $cm^2V^{-1}s^{-1}$ at N_s=4x10^{12} cm^{-2} in long channel QW-MOSFETs
- HfO_2 / InP dielectric for superior performance

Acknowledgement

- Fabrication facility at MIT labs: MTL, NSL, SEBL.
- Heterostructure grown by IntelliEPI Inc.
- MIT collaborators: L. Xia, D. Jin, A. Guo, X. Zhao, S. Warnock, L. Guo, J. Hoyt, J, Teherani, W. Chern.
- MSD collaborators: R. Galatage, R. M. Wallace, E. M. Vogel .
- Industrial collaborators: T.-W. Kim (Sematech), D.-H. Kim (Global Foundries), J.-M. Kuo (IntelliEPI).

Thank you.