InAs High-Electron Mobility Transistors on the Path to THz Operation

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1. Introduction

The invention of the High-Electron Mobility Transistor (HEMT) revolutionized the world of high-frequency electronics [1]. First on GaAs, then on InP and more recently on GaN, HEMTs have steadily achieved higher levels of performance in terms of high frequency gain, noise and power. Today, InAs HEMTs on InP exhibit the best balanced high-frequency response (high f_T *and* high f_{max}) of any transistor technology [2]. InAs HEMTs are uniquely poised to attain the first true THz transistor (both f_T and f_{max}>1 THz). This paper reviews the evolution of HEMTs along their path towards THz operation and discusses steps to be taken in order to attain this ultimate prize.

2. Historical evolution of high-frequency HEMTs

Fig. 1 shows the evolution of the current-gain cut-off frequency (f_T) of GaAs and InP HEMTs as well as GaAs MESFETs as a function of time. Soon after their first demonstration, GaAs HEMTs (with the GaAs lattice constant) surpassed GaAs MESFETs in terms of f_T only to be soon overtaken by the newer InP HEMTs (with the InP lattice constant). Since the late 80s, HEMTs on InP have exhibited the highest f_T of any FET on any material system. The current record is 688 GHz set by a collaboration between Teledyne Scientific and MIT [2].

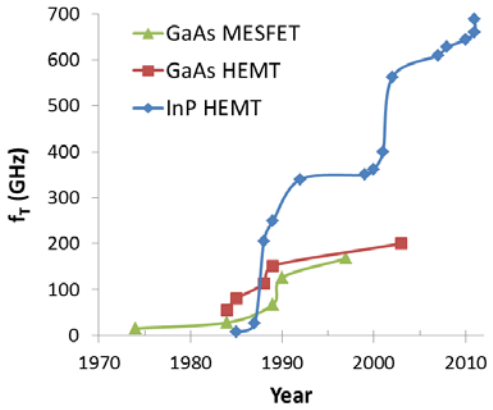

Fig. 1: f_T vs year of demonstration of GaAs MESFETs, GaAs HEMTs and InP HEMTs.

More remarkable is the outstanding balance between f_T and f_{max} that HEMTs have demonstrated. The record device in [2] simultaneously demonstrates an f_T of 688 GHz and an f_{max} of 800 GHz. No other transistor comes close to this. f_{max}>1 THz devices have been reported [3].

It is interesting to study the structural evolution of these record devices. Fig. 2 shows gate length, channel InAs composition, channel thickness and insulator thickness vs. time for the record devices of Fig. 1. Rapid gate length scaling took place in the first 20 years but this has now stalled at around 20-40 nm. In early designs, the channel consisted of pure GaAs but soon it moved to $In_xGa_{1-x}As$ lattice matched to InP (x=0.53). Over time the InAs composition has increased to 100% InAs in the subchannel of recent designs. Channel and insulator thickness also scaled rapidly at first, but they recently have saturated to about 10 and 4 nm, respectively. Structurally, little has changed in InGaAs HEMTs on InP in the last 10 years which explains the recent modest progress.

There are several reasons for this. Harmonious scaling requires that all dimensions scale in a proportional way. First, when the InAlAs barrier thickness reaches around 4 nm, the gate current quickly becomes unmanageable [4]. In the absence of barrier thickness scaling, further reductions in gate length severely degrade the transconductance which increases the extrinsic and parasitic delays [2]. A second reason is the mobility degradation that comes with channel thickness scaling [5]. This does not affect much the velocity of carriers in the channel, which is what matters for the intrinsic delay, but it increases the source and drain resistances and degrades the parasitic delay [6]. Furthermore, in advanced devices the intrinsic delay is a small fraction of the total delay with parasitic resistance and capacitance becoming overwhelmingly important [2]. In this limit, maintaining high intrinsic g_m and high electrostatic integrity is essential and these are often hurt by excessive L_g scaling.

3. Prospects for THz transistors

Starting from the current world record devices, a straightforward reduction of all parasitics by 30% together with gate length scaling to 20 nm should bring us to an f_T of about 1 THz [2]. To accomplish this, series resistance reduction is imperative. Key to this is bringing the metal contacts in very close proximity to the gate [7]. This demands self-aligned designs [8].

Parasitic capacitance reduction is more difficult. Gate structures with a tall stem, a cavity around the gate [9] and

the use of different gate-contact spacings on the source and drain sides [9] have all been demonstrated.

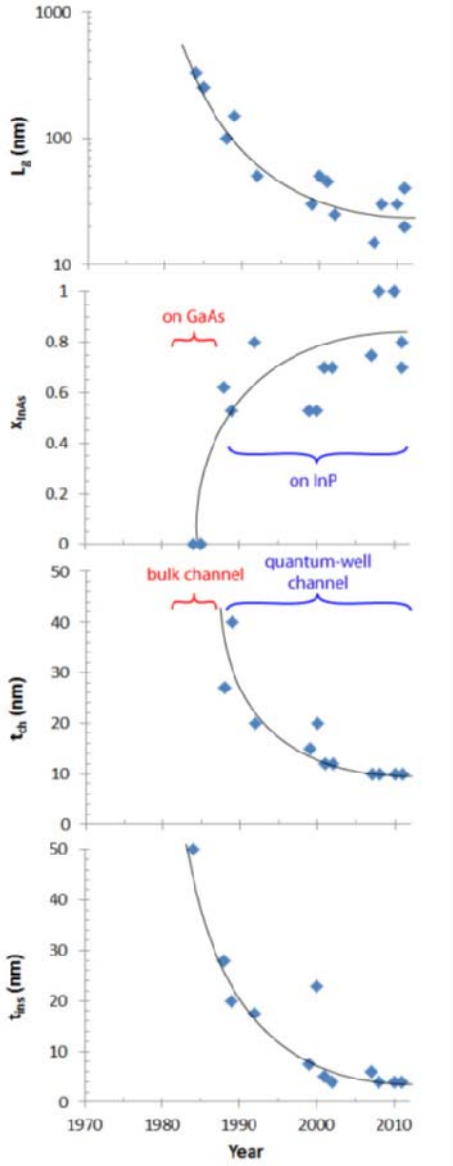

Fig. 2: Evolution of structural design of record f_T HEMTs.

Attaining high g_m without degrading anything else is also difficult. Harmonious scaling of all device dimensions is a possible path but this is not straightforward in conventional designs. A 3D Tri-Gate [10] or Nanowire FET [11] approach might be required. These designs offer greatly improved electrostatic control of the channel by the gate and therefore potentially higher g_m.

Staying with a planar design, gate leakage can be suppressed through the use of a dielectric gate barrier. This should enable further gate length scaling. Recently, there has been great progress in the development of high-quality high-K oxide/III-V interfaces as a result of the exploding interest in III-V CMOS [12]. Today, InGaAs Quantum-Well MOSFETs have already been demonstrated with f_T=245 GHz [13]. Whether oxide-semiconductor interfaces ever approach the quality of semiconductor heterostructures so as to enable the high electron velocities and mobilities that we have come to expect of the InGaAs system is a topic of current research.

An additional path to improve g_m and frequency response is by enhancing the electron velocity in the channel. One way to do this is through strain engineering. Tensile stress enhances electron mobility through a reduction in the effective mass. InAs quantum wells grown on substrates with a larger lattice constant than InP have been shown to exhibit extraordinary electron mobilities [14,15]. Another path is through the use of InAsSb ternary channels [16]. In fact, there has been a lot of effort to exploit the extraordinary transport properties of relaxed InAs or InAsSb. Transistors based on these materials with ~0.6 nm lattice constant have yielded excellent performance at very low voltages but have yet to approach InAs HEMTs on InP probably due to excessive impact ionization and large output conductance [17]. Device structural innovation introducing a high degree of channel confinement will be required to overcome these issues.

4. Conclusions

THz transistors, that is transistors in which both f_T and f_{max} are over 1 THz, are just around the corner. InAs HEMTs with lattice constants close to that of InP are best positioned to accomplish this feat. This paper has briefly reviewed the evolution of high-frequency HEMTs and has discussed paths forward to attain this enticing goal.

Acknowledgements

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References

[1] J. A. del Alamo, 2011 CS-MANTECH, p. 17.
[2] D.-H. Kim et al., 2011 IEDM, p. 319.
[3] R. Lai et al., 2007 IEDM, p. 609.
[4] J. A. del Alamo et al., 2011 IPRM.
[5] T.-W. Kim et al., 2010 IPRM, p. 496.
[6] T.-W. Kim and J. A. del Alamo, 2011 IPRM.
[7] H. Matsuzaki et al., 2005 IEDM.
[8] T.-W. Kim et al., 2010 IEDM, p. 696.
[9] T. Takahashi et al., 2011 IPRM.
[10] M. Radosavljevic et al., 2011 IEDM, p. 765.
[11] J. J. Gu et al., IEEE Electron Dev. Lett. 33, 967 (2012).
[12] J. A. del Alamo, Nature 479, 317 (2011).
[13] T. W. Kim et al., 2012 VLSI Tech. Symp., p. 179.
[14] X. Wallart et al., Applied Phys. Lett. 87, 043504 (2005).
[15] N. Kuze et al., J. Crystal Growth 175/176, 868 (1997).
[16] A. Ali et al., 2012 VLSI Tech. Symp., p. 181.
[17] B. Y. Ma et al., IEEE Trans Microw. Theory and Techn. 54, 4448 (2006).