III-V High-Electron Mobility Transistors on the path to THz operation

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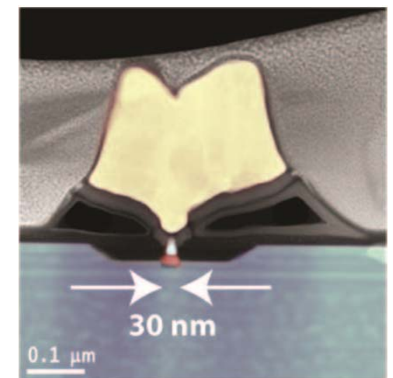

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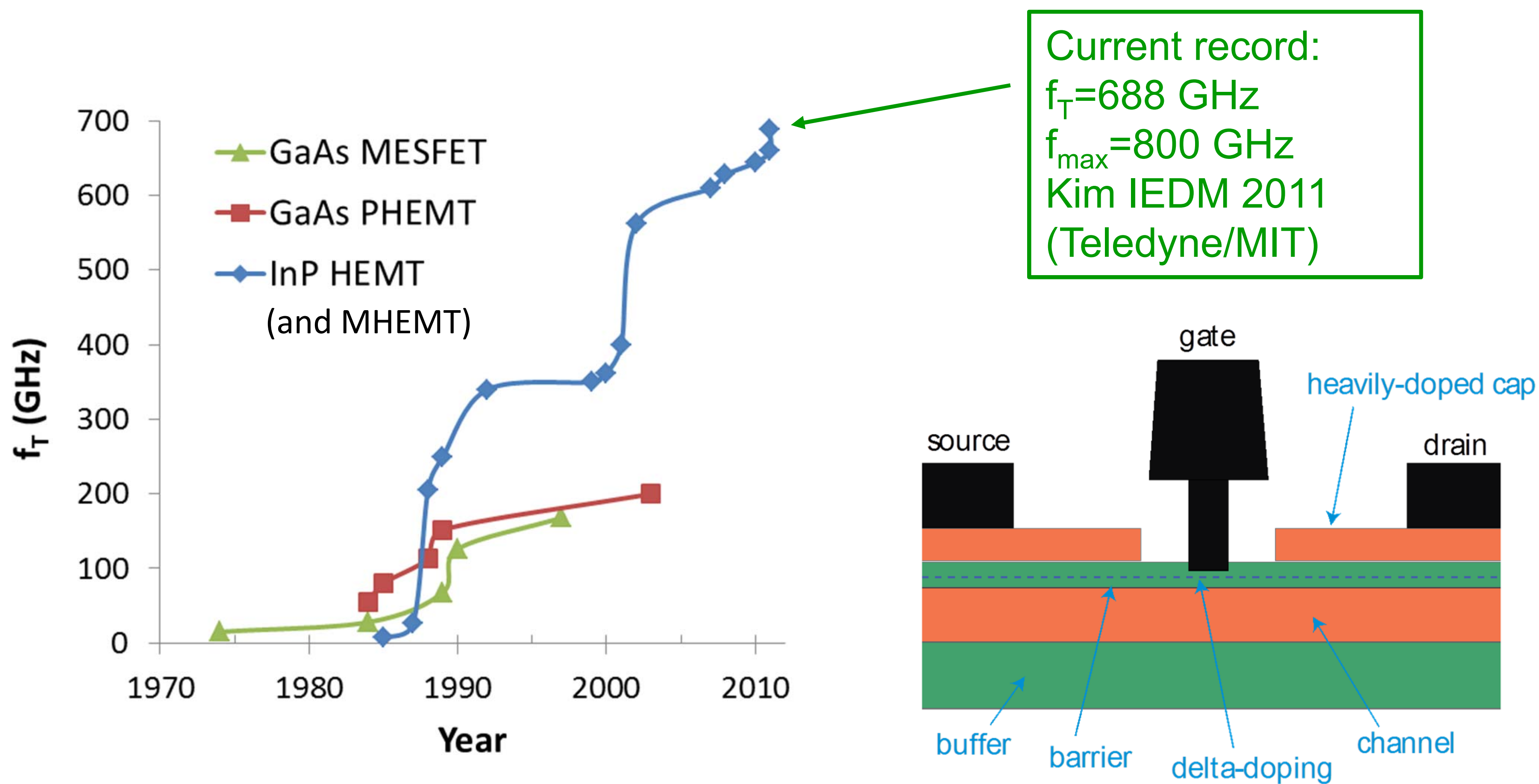
Outline

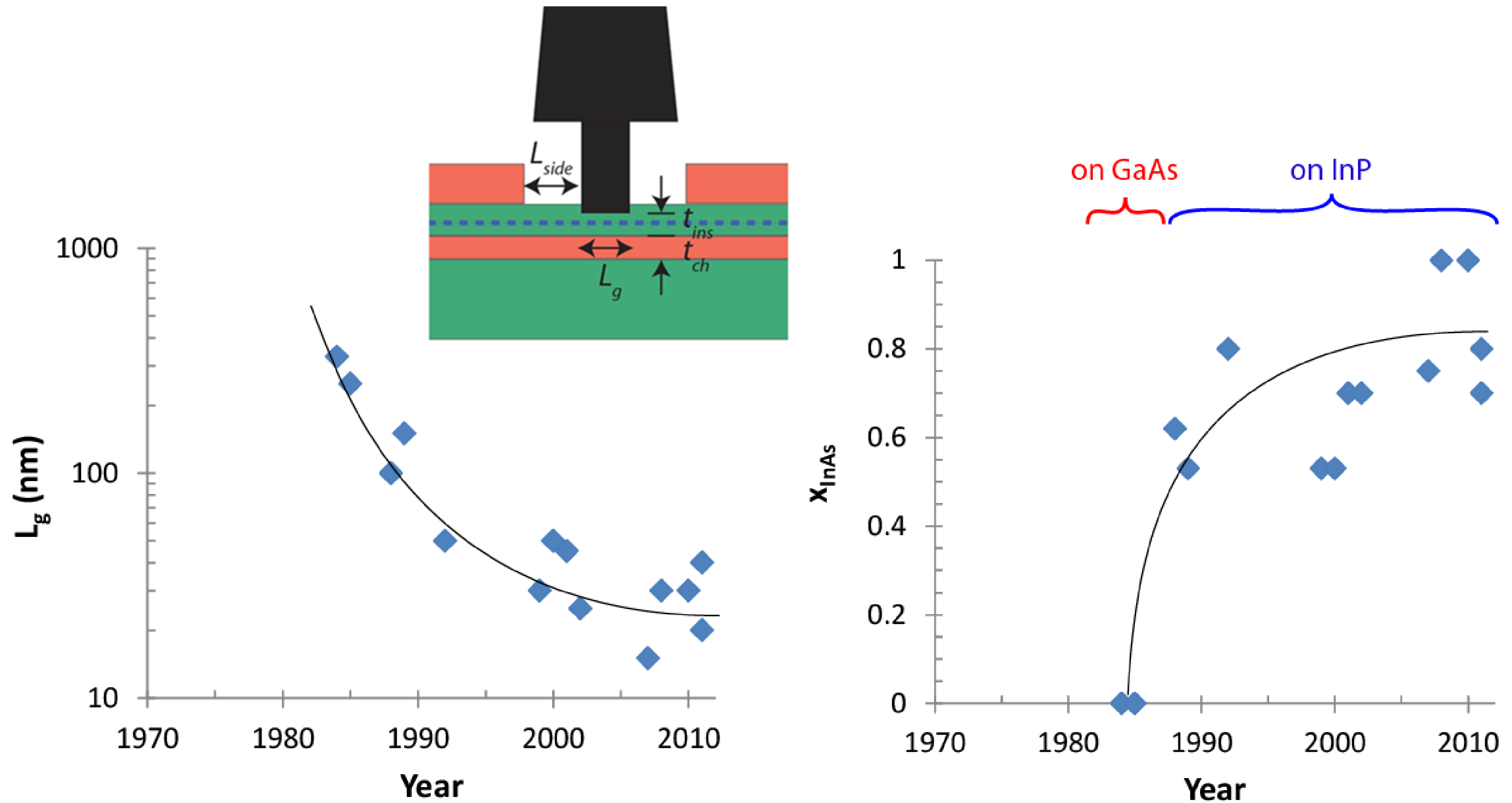
1. High-frequency III-V HEMTs: megatrends
2. State-of-the-art InGaAs HEMTs and f_T analysis
3. The path to THz operation

1. III-V HEMT: record f_T vs. time



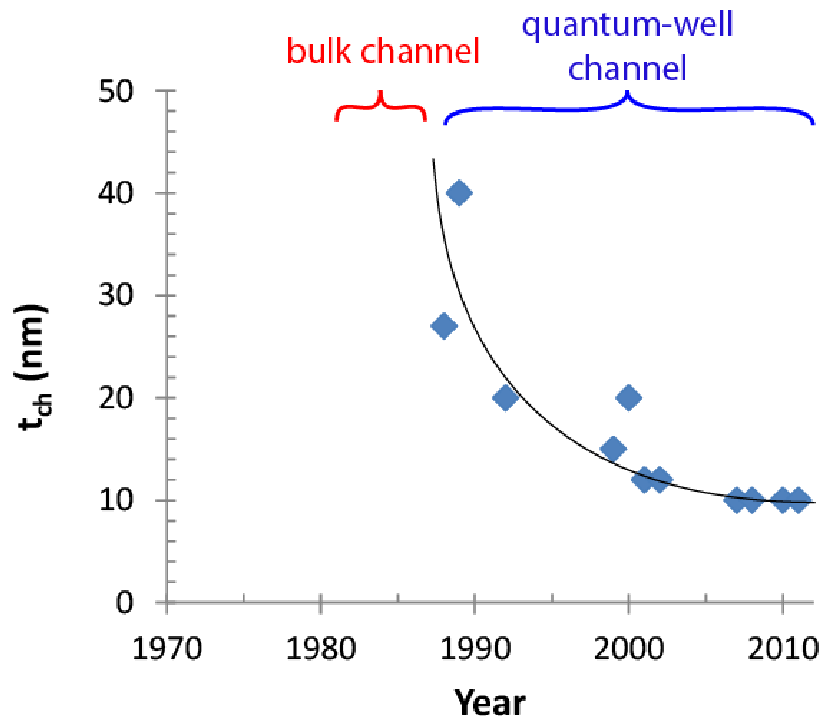
- For >20 years, record f_T obtained on InGaAs-channel HEMTs
- InGaAs-channel HEMTs offer record balanced f_T and f_{max}

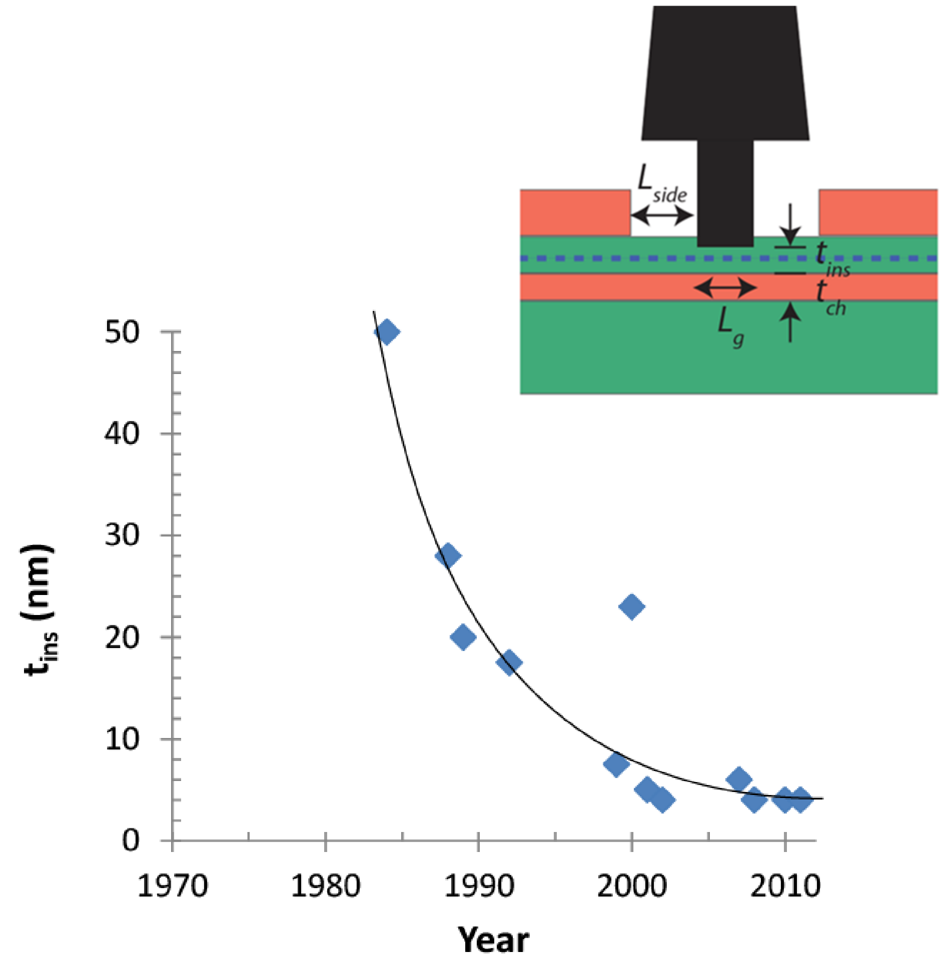
Record f_T III-V HEMTs: megatrends



- Over time: $L_g\downarrow$, $In_xGa_{1-x}As$ channel $x_{InAs}\uparrow$
- L_g, x_{InAs} saturated → no more progress possible?

Record f_T III-V HEMTs: megatrends

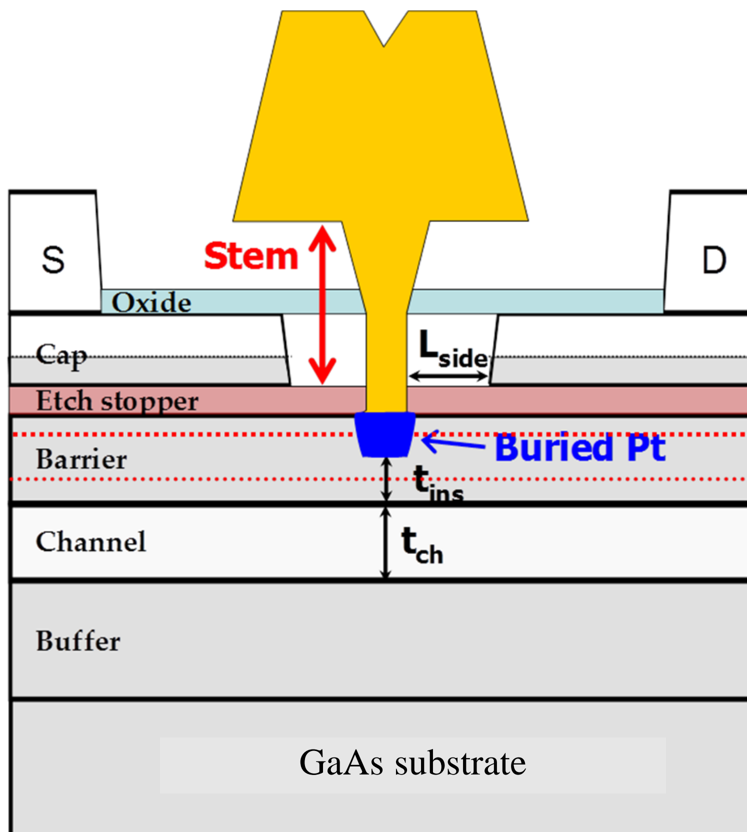




- Over time: $t_{ch}\downarrow$, $t_{ins}\downarrow$
- t_{ch}, t_{ins} saturated → no more progress possible?

2. State-of-the-art InGaAs HEMT

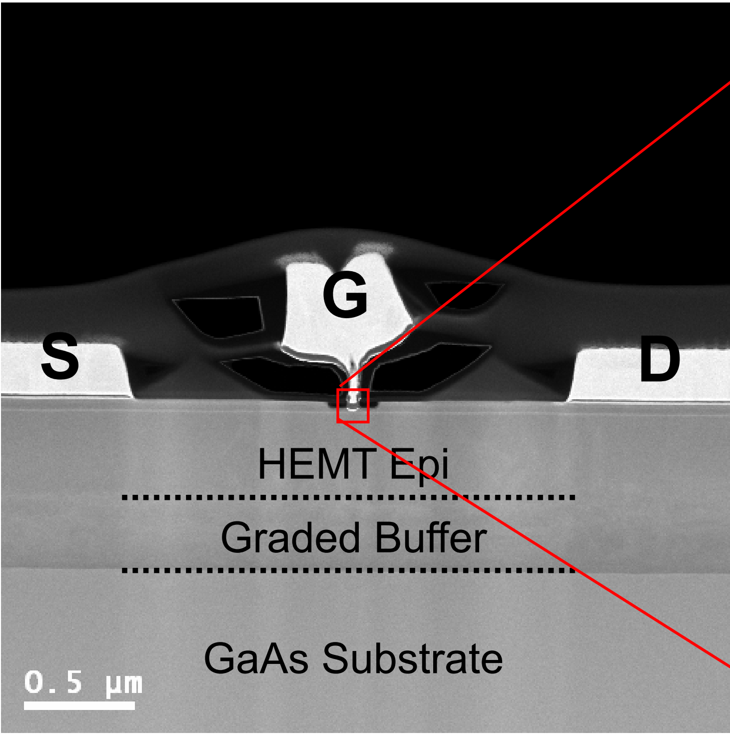
L_g=40 nm InGaAs MHEMT

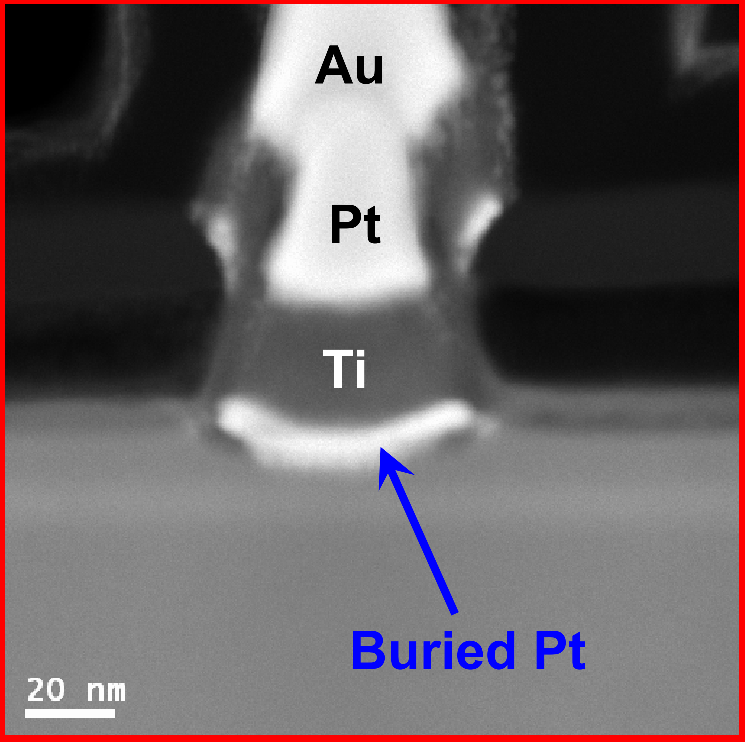


- $In_{0.7}Ga_{0.3}As$ QW channel
  - t_{ch} = 10 nm
  - $\mu_{n,Hall}$ > 10,000 cm^2/V-sec
- $In_{0.52}Al_{0.48}As$ barrier + $In_{0.7}Al_{0.3}As$ spacer (Kim, EL 2011)
- Dual Si δ-doping (Kim, IEDM 2010)
- Pt (3 nm)/Ti/Pt/Au Schottky
  - t_{ins}=4 nm
- InP etch stop (t_{InP}=6 nm)
- L_{side}=100 nm
- Gate stem > 250 nm
- Mo-based S/D with 2 μm S-D spacing

Kim, IEDM 2011

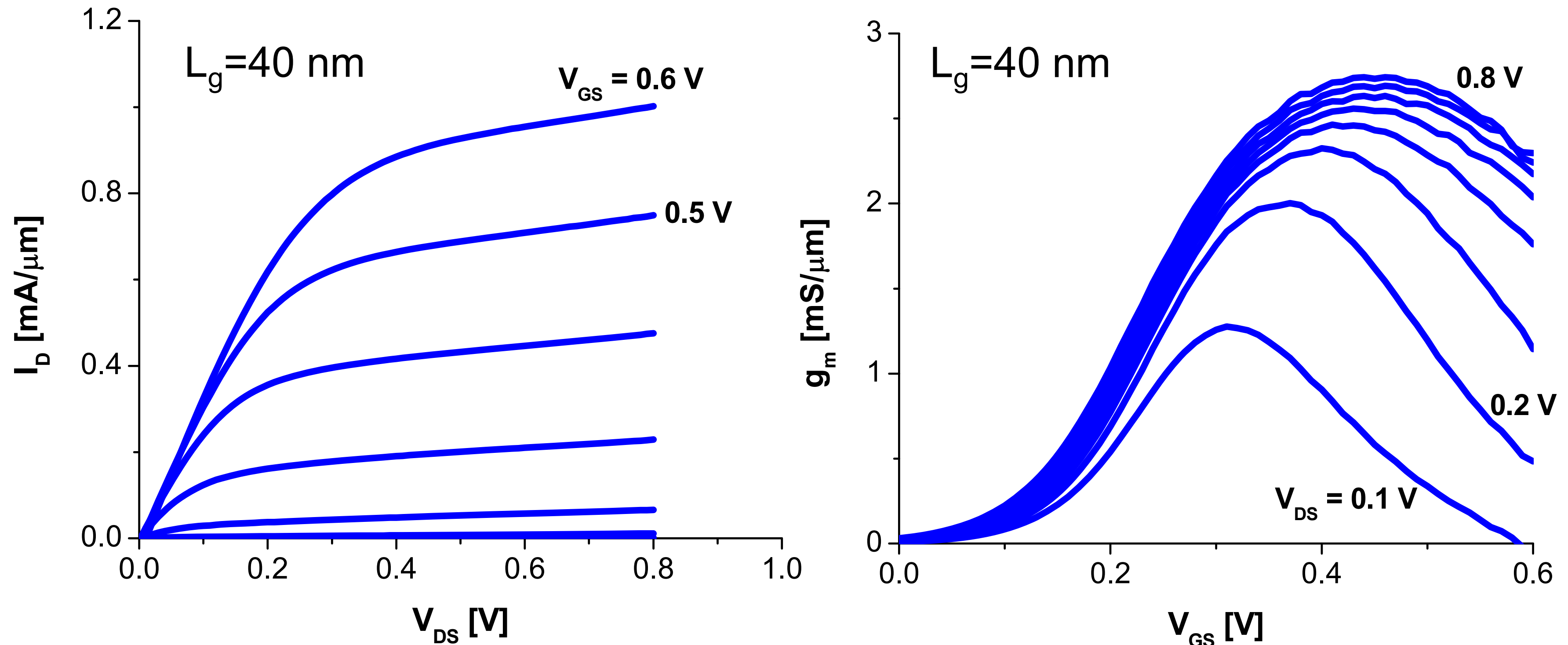
TEM cross section





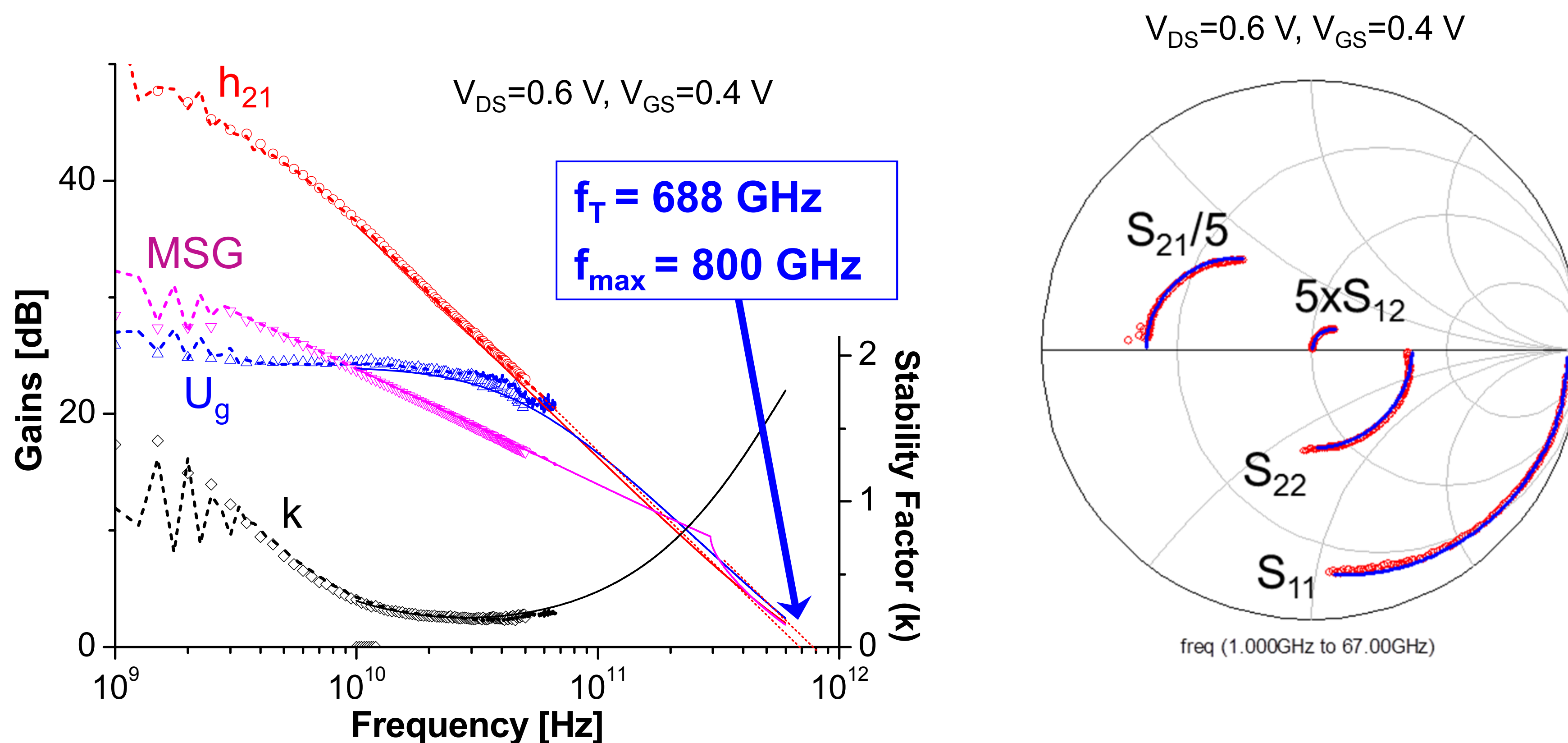
Output and transfer characteristics

Kim, IEDM 2011



- Large current drive: I_D>1 mA/μm at V_{DS}=0.8 V
- High transconductance: g_{mpk}= 2.75 mS/μm at V_{DS}=0.8 V
- $V_T \approx 0$ V, R_{ON}=280 Ω.μm

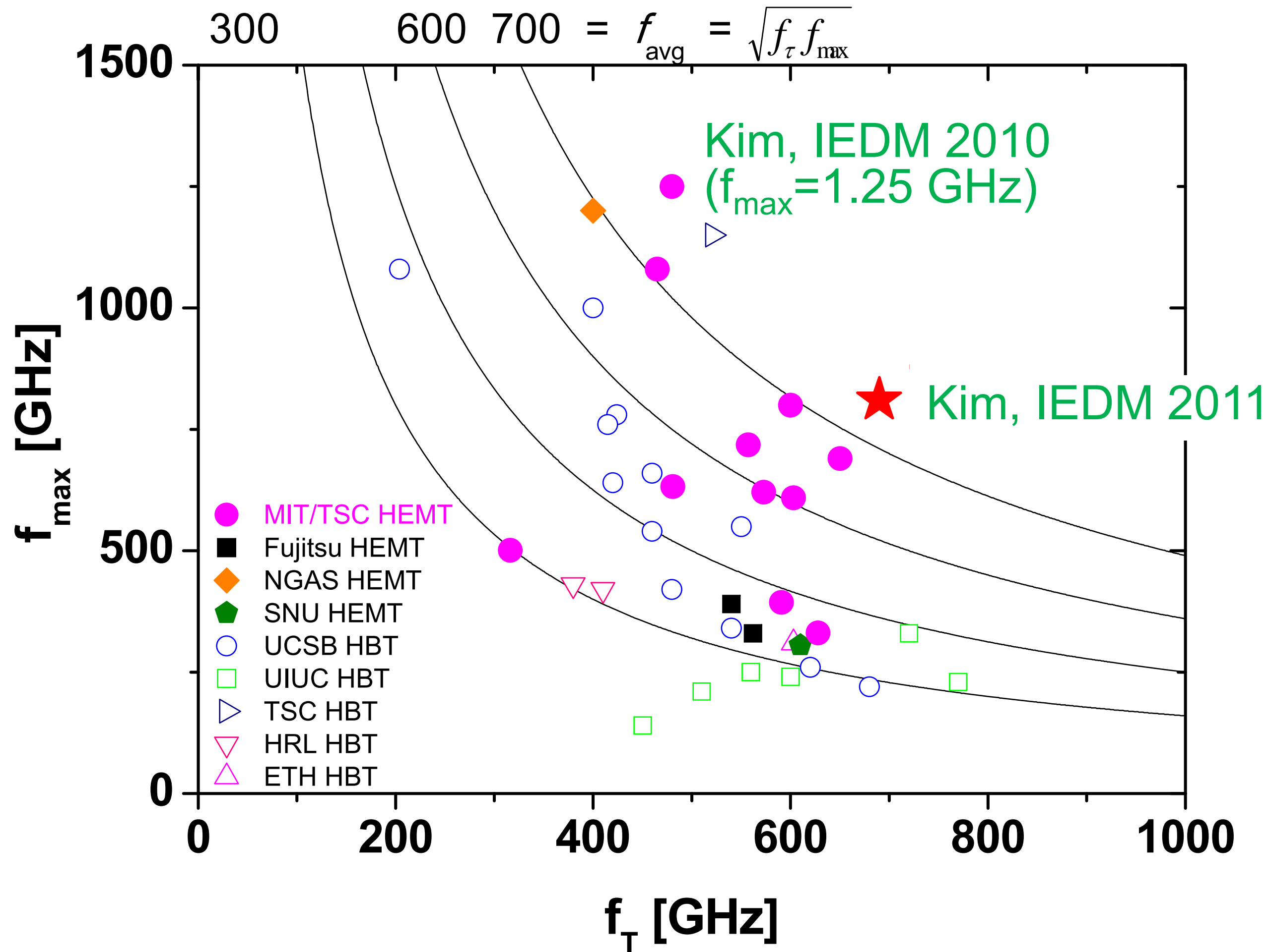
High-frequency characteristics



- Only transistor of any kind with both f_T and f_{max} > 680 GHz
- Obtained at same bias point, V_{DS}=0.6 V

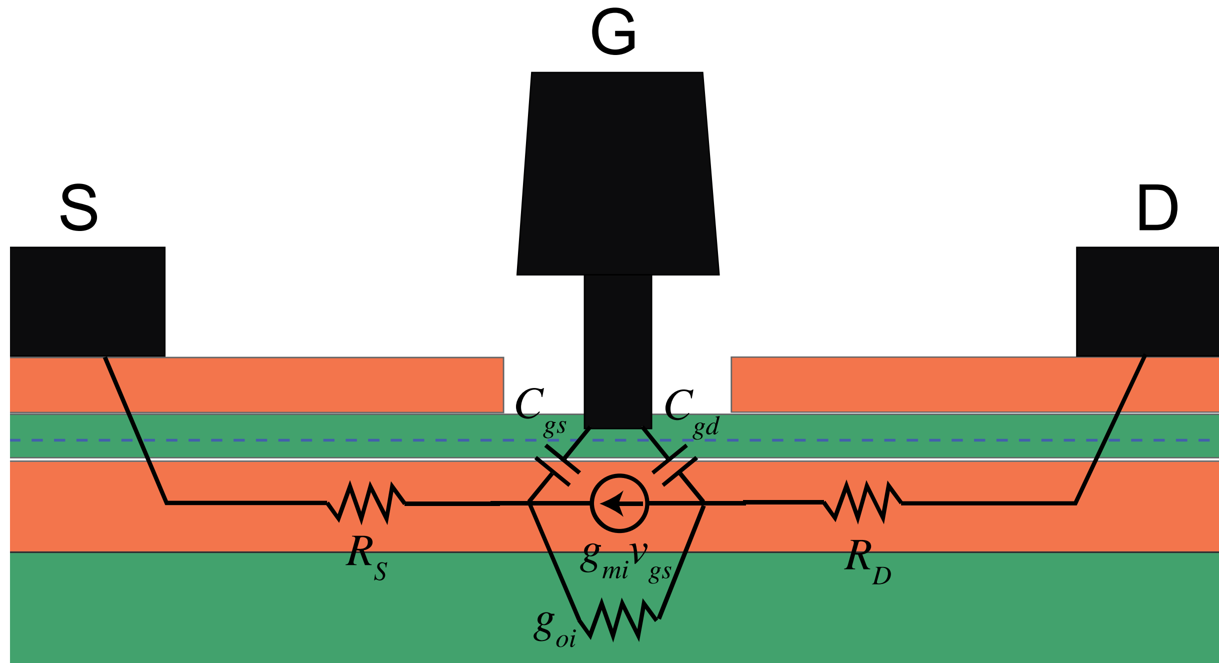
Kim, IEDM 2011

f_T *vs.* f_{max}



- Record f_T FET
- Best-balanced f_T and f_{max} transistor

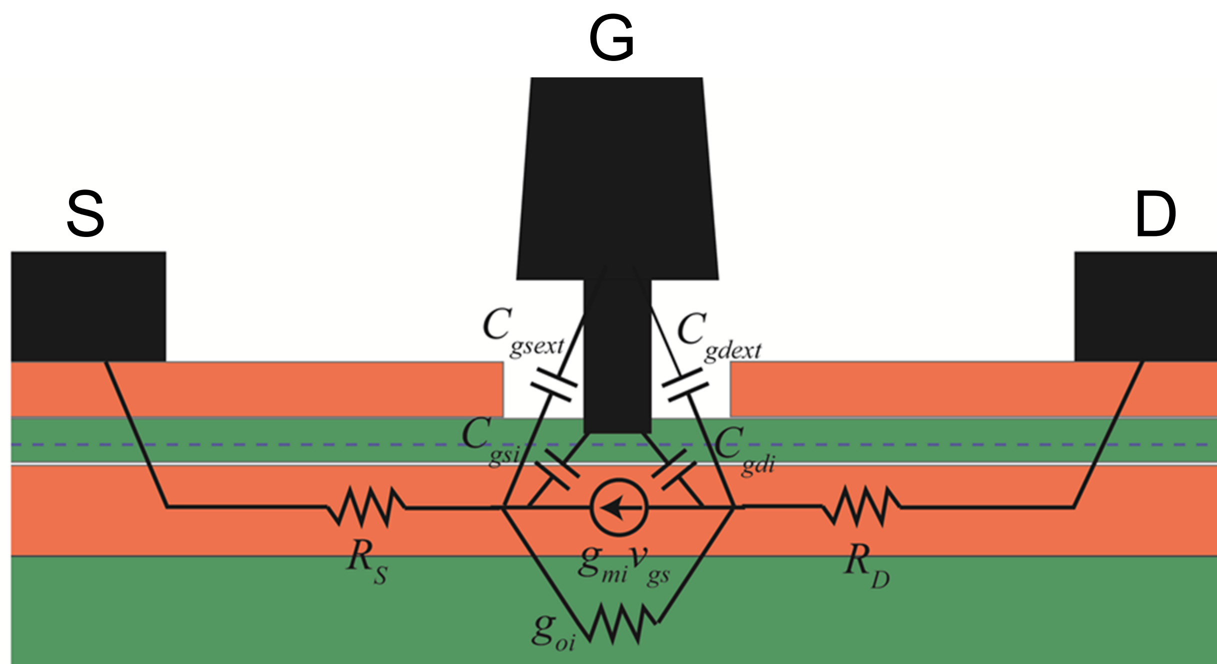
f_t analysis



- First-order f_T expression for HEMT:

$$f_T = \frac{1}{2\pi}\frac{g_{mi}}{C_{gs}+C_{gd}+g_{mi}(R_S+R_D)[C_{gd}+(C_{gs}+C_{gd})\frac{g_{oi}}{g_{mi}}]}$$

Break out extrinsic capacitances



- Capacitance components:

$$C_{gs} = C_{gsi} + C_{gsext} \qquad C_{gd} = C_{gdi} + C_{gdext}$$

Delay time analysis

- Delay time:

$$\tau = \frac{1}{2\pi f_T} = \tau_t + \tau_{ext} + \tau_{par}$$

- Components of delay time:

$$\tau_t = \frac{C_{gsi} + C_{gdi}}{g_{mi}} = \frac{L_g}{< v_e >}$$

Intrinsic delay (transit time)

Extrinsic delay

$$\tau_{ext} = \frac{C_{gsext} + C_{gdext}}{g_{mi}}$$

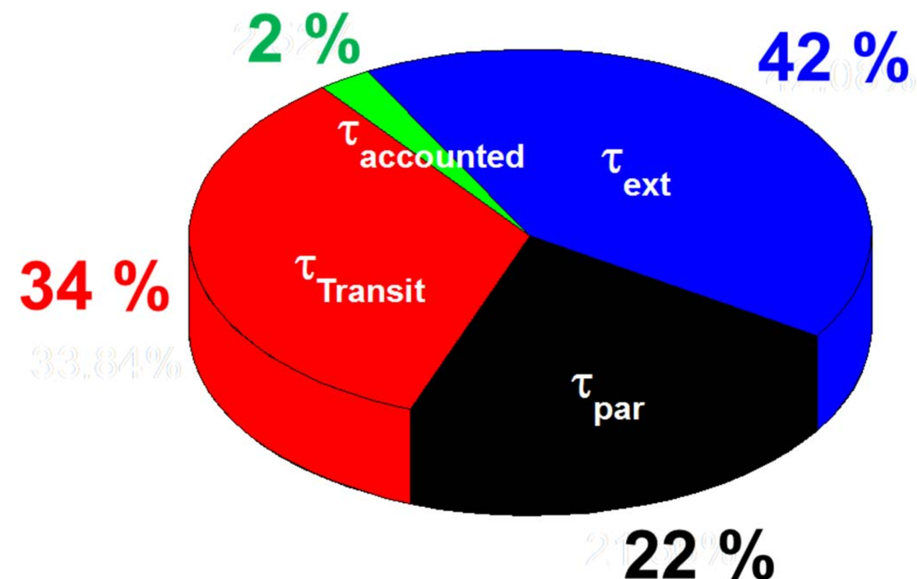
Parasitic delay

$$\tau_{par} = (R_S + R_D)[C_{gd} + (C_{gs} + C_{gd})\frac{g_{oi}}{g_{mi}}]$$

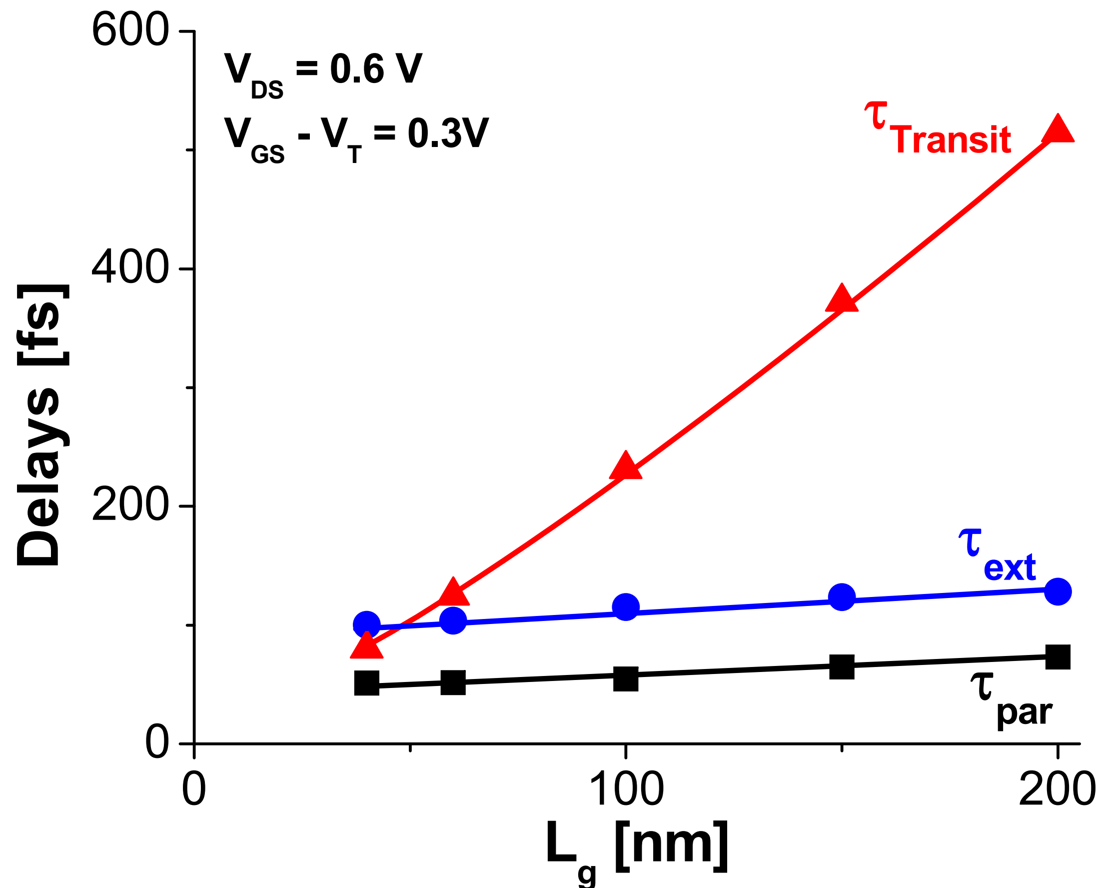
Delay components of L_g=40 nm InGaAs HEMT

Delay time from f_T: ~231 fs

- Intrinsic delay: ~81 fs ← yields $<v_e>=5x10^7$ cm/s
- Extrinsic delay: ~99 fs ← most significant
- Parasitic delay: ~50 fs
- Unaccounted: ~9 fs

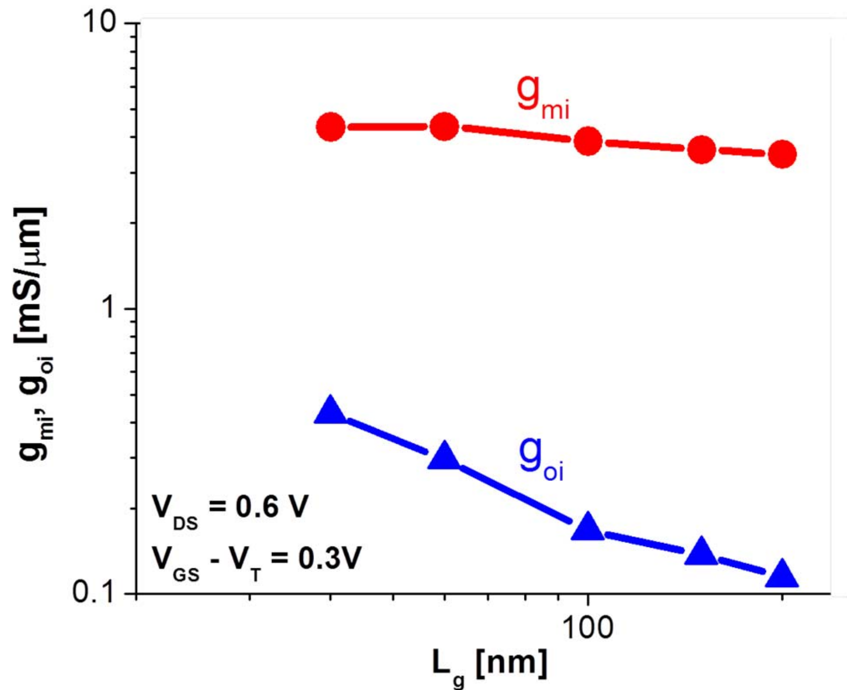


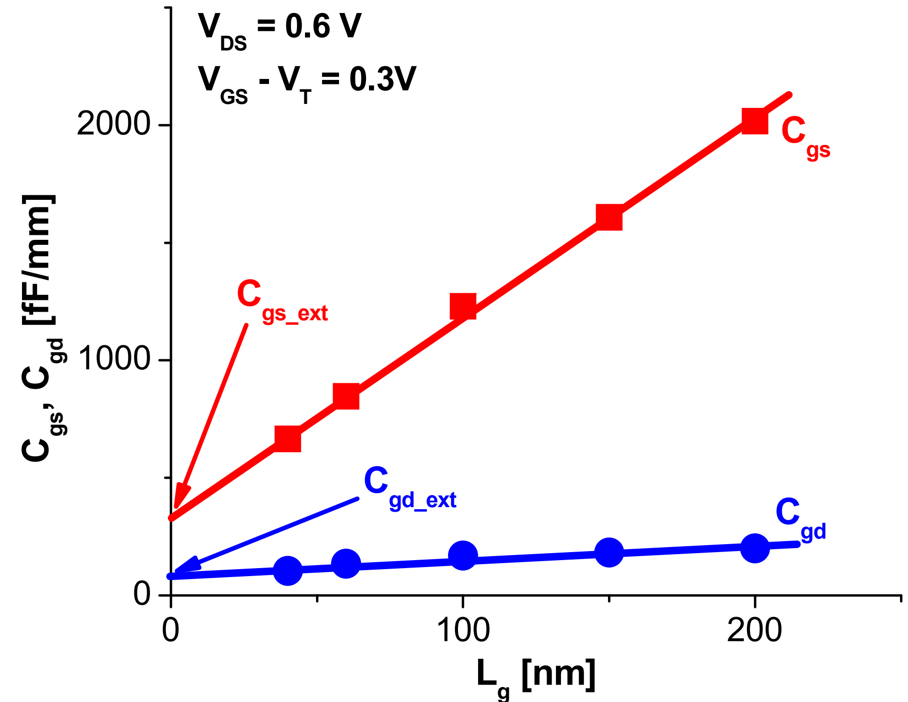
Scaling of delay components



τ_{ext} and τ_{par} do not scale, become dominant for L_g< 50 nm

Scaling of small-signal components





As $L_g \downarrow$:

$$\tau_{ext} = \frac{C_{gsext} + C_{gdext}}{g_{mi}}$$

do not scale

do not scale

$$\tau_{par} = (R_S + R_D)[C_{gd} + (C_{gs} + C_{gd})\frac{g_{oi}}{g_{mi}}] \uparrow$$

3. The path to THz operation

- Intrinsic delay ↓ → L_g ↓
- Extrinsic delay ↓:

$$\tau_{ext} = \frac{C_{gsext} + C_{gdext}}{g_{mi}}$$

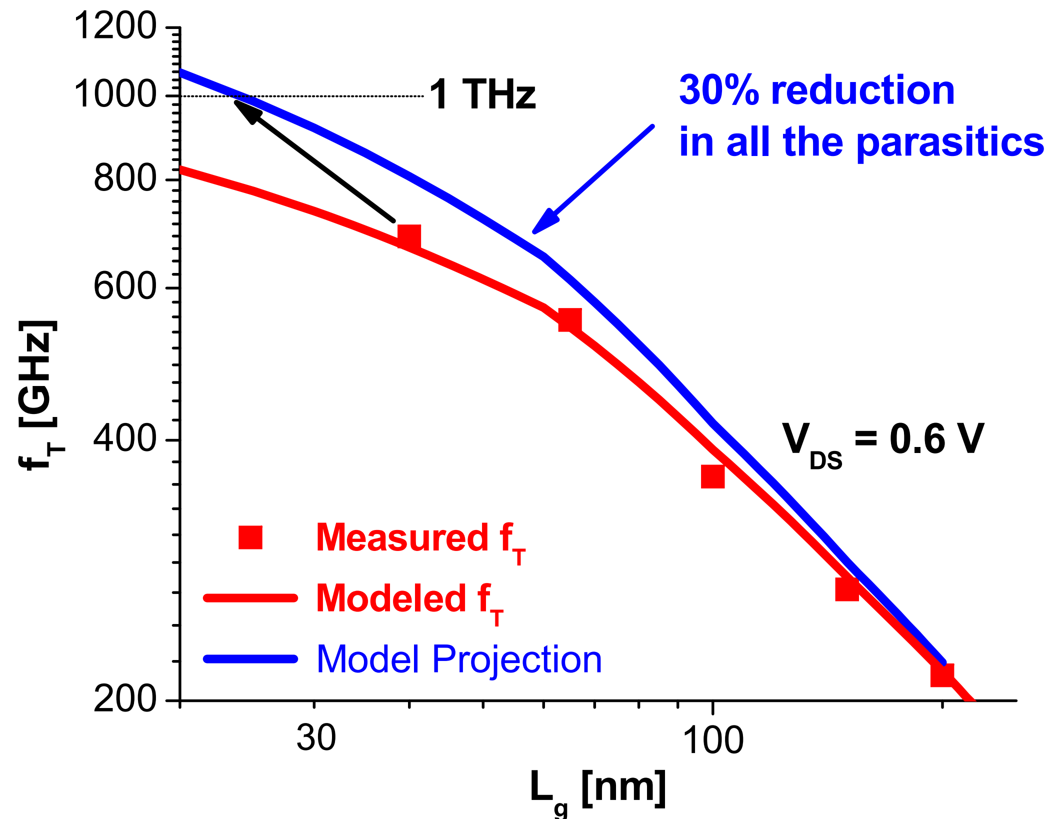
→ C_{gsext}, C_{gdext} ↓ → gate engineering
→ g_{mi} ↑ → harmonious scaling

- Parasitic delay ↓:

$$\tau_{par} = (R_S + R_D)[C_{gd} + (C_{gs} + C_{gd})\frac{g_{oi}}{g_{mi}}]$$

→ R_S+R_D ↓ → S/D engineering
→ g_{oi}/g_{mi} ↓ → harmonious scaling

How to reach f_t = 1 THz?

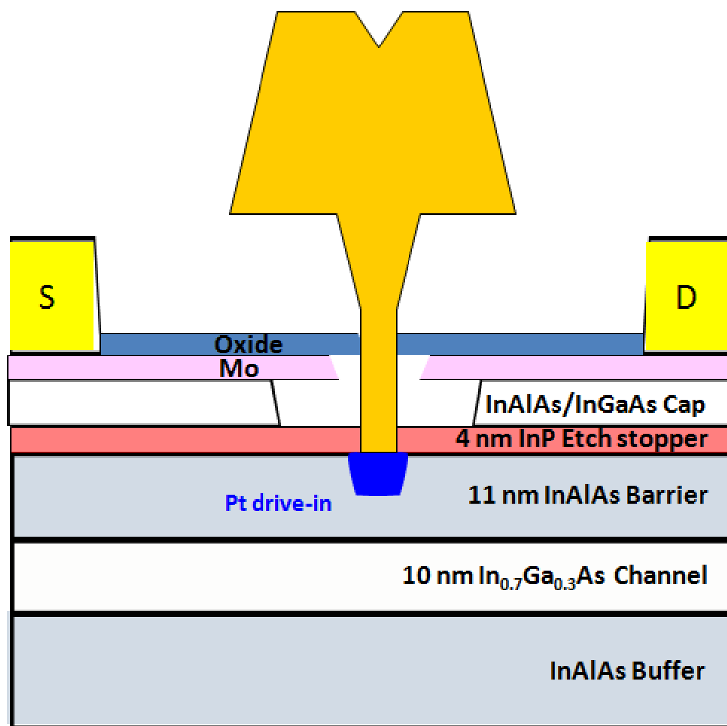


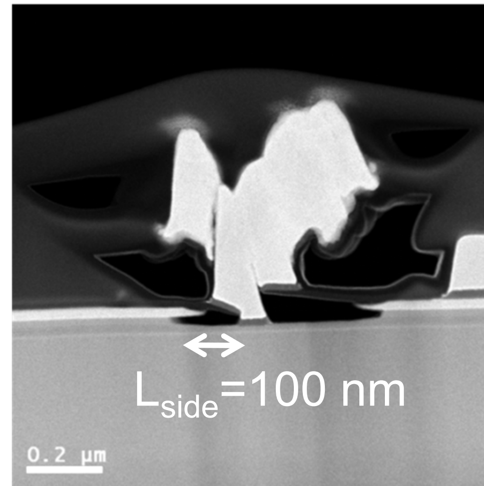
f_T = 1 THz feasible by:

→ scaling to $L_g \approx$ 25 nm

→ ~30% parasitic reduction

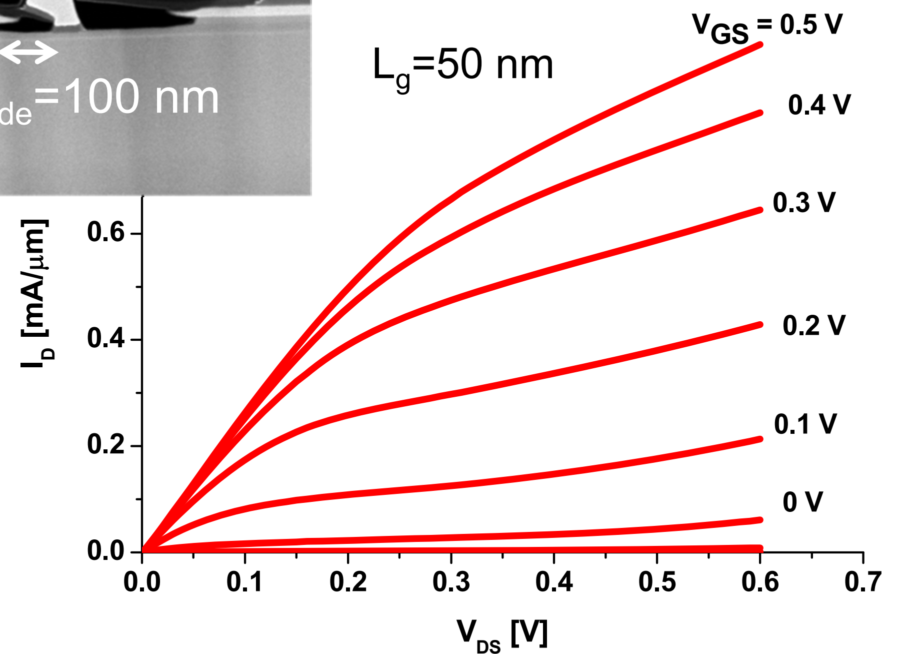
Approach to $R_S + R_D \downarrow$: self-aligned process





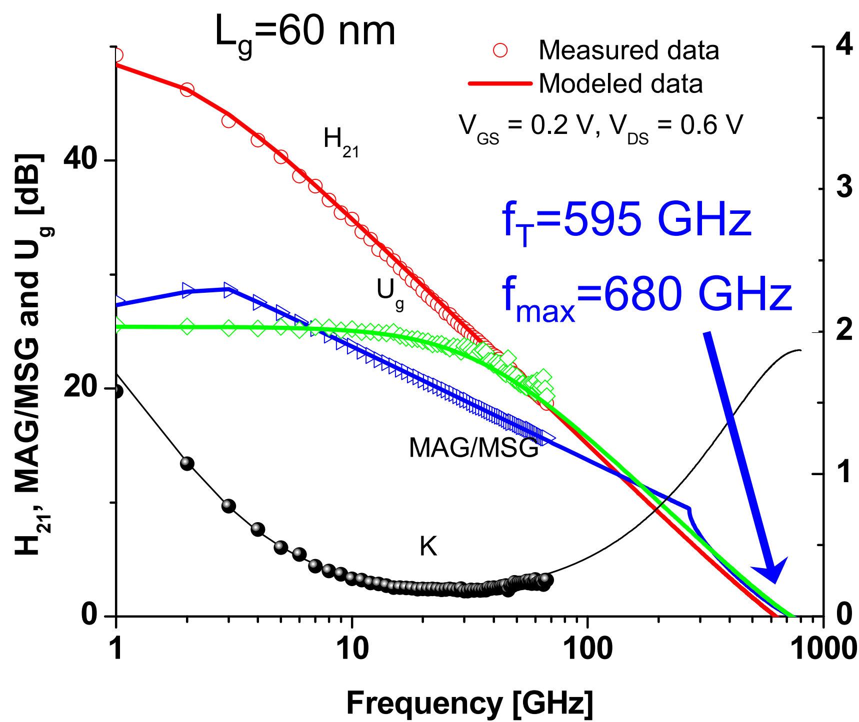
Kim, IEDM 2010

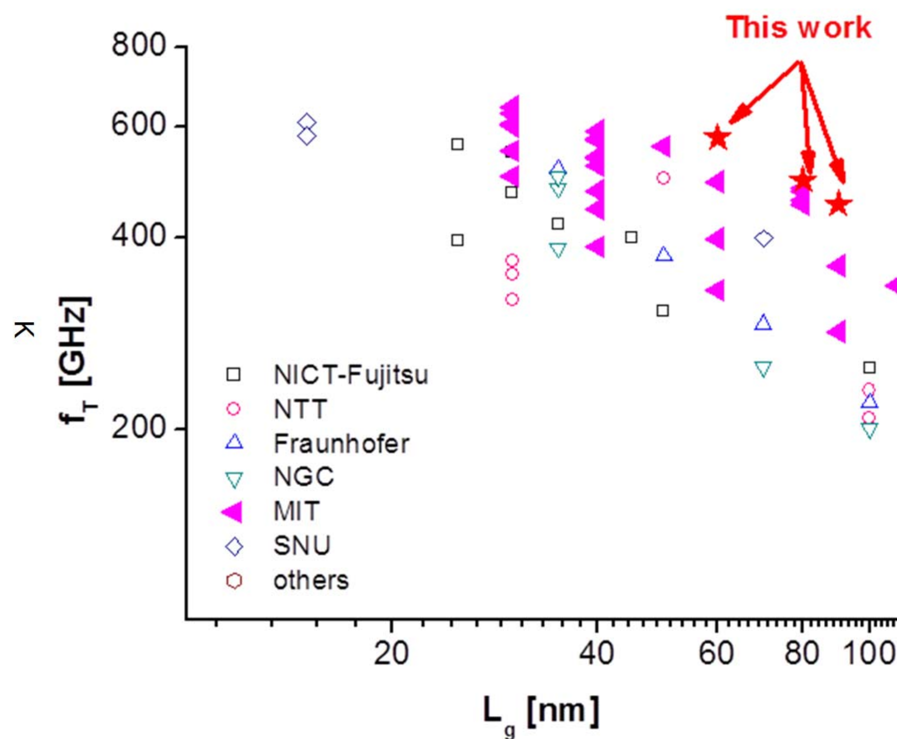
Waldron, TED 2010



- Dry-etched Mo contacts: R_c = 7 Ω.µm
- L_g=50 nm, R_{ON}=290 Ω.µm, g_{mpk}=2.2 mS/µm @ V_{DS}=0.5 V

L_g=60 nm self-aligned $In_{0.7}Ga_{0.3}As$ HEMT



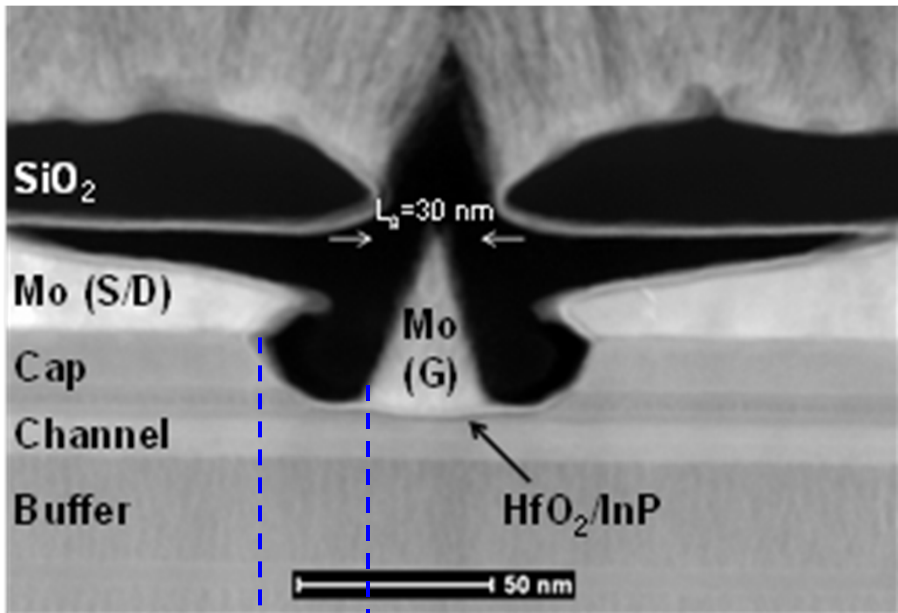


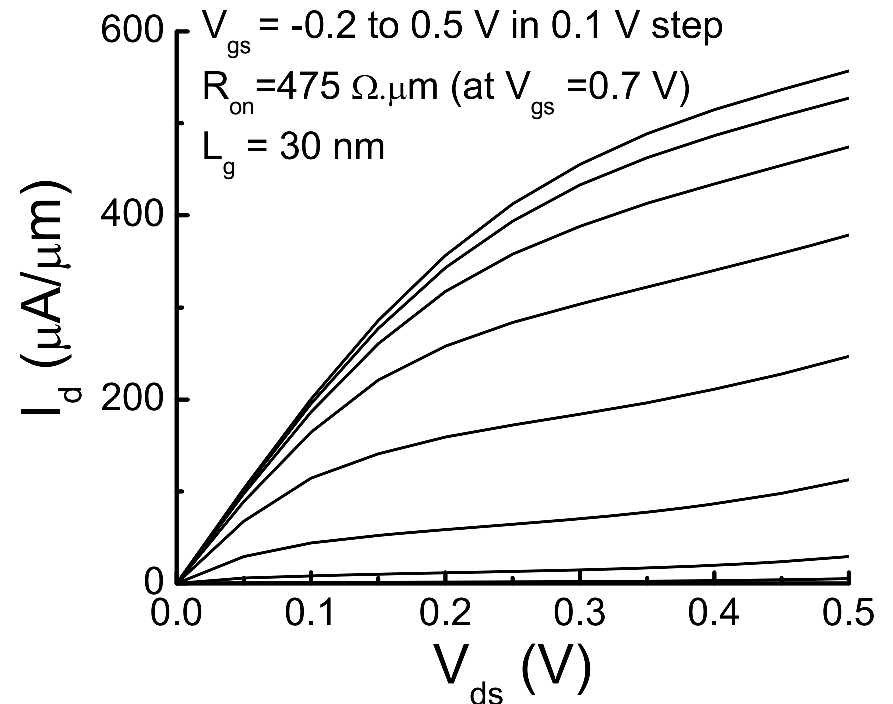
Kim, IEDM 2010

Highest f_T and f_{max} of any FET at $L_g \geq 60$ nm

L_g=30 nm self-aligned InGaAs MOSFET with L_{side}~30 nm

Lin, IEDM 2012

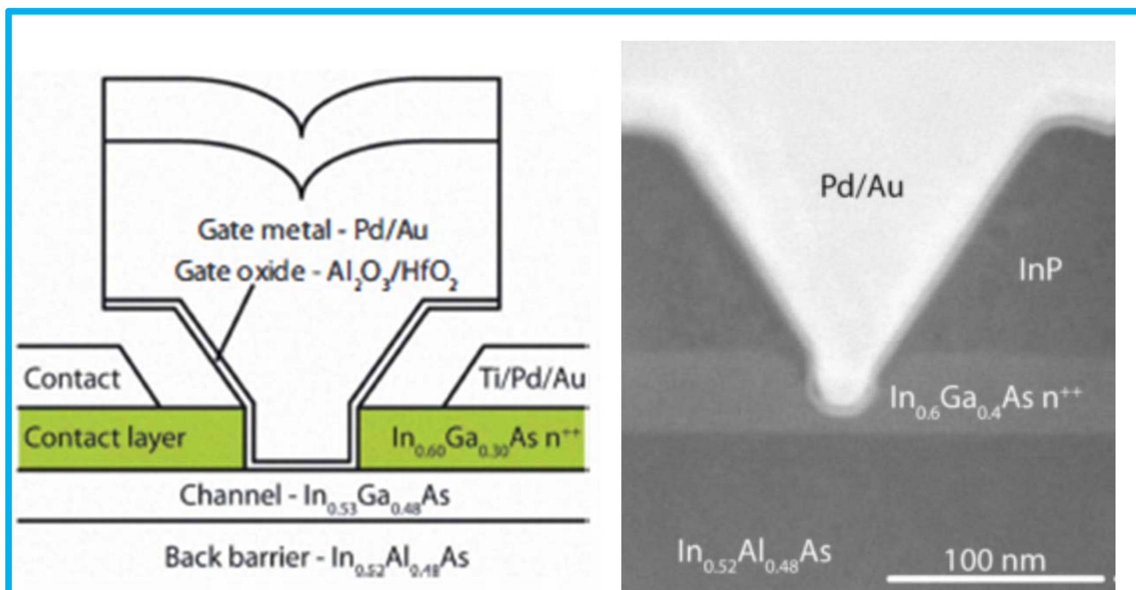




g_{mpk}=1.4 mS/μm

R_{ON}=475 Ω.μm → access region design critical!

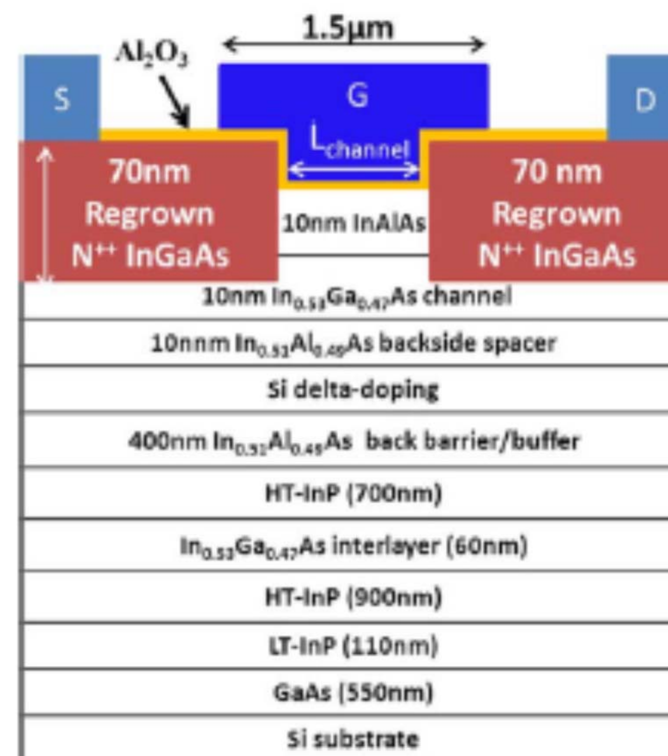
Regrown source and drain regions

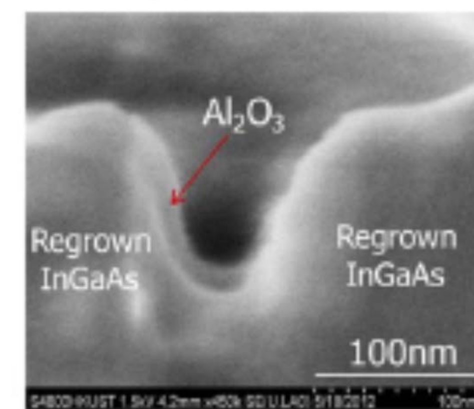


L_{ch}=55 nm InGaAs MOSFET:

R_{ON}=199 Ω.µm

Egard, IEDM 2011





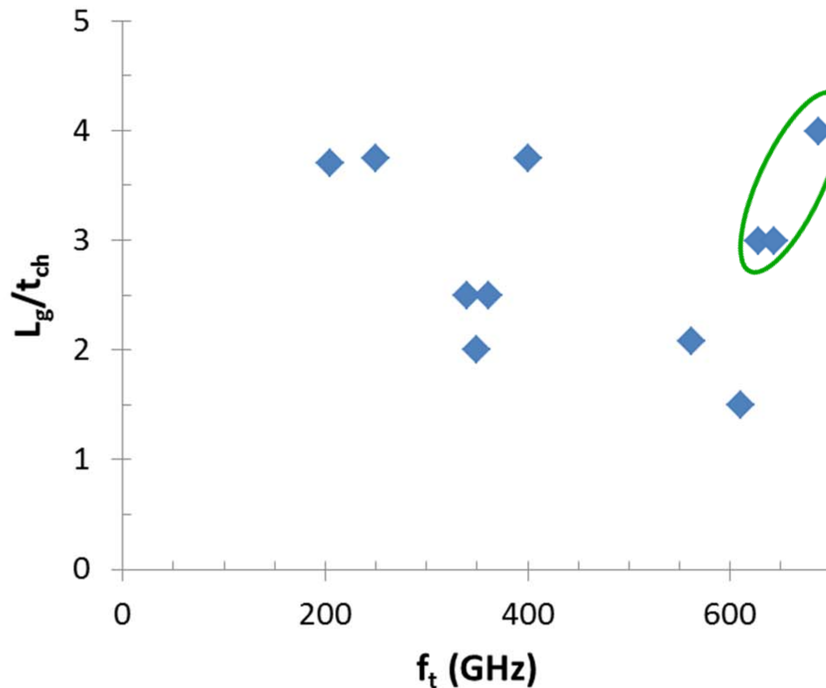
L_{ch}=30 nm InGaAs MOSFET:

R_{ON}=133 Ω.µm

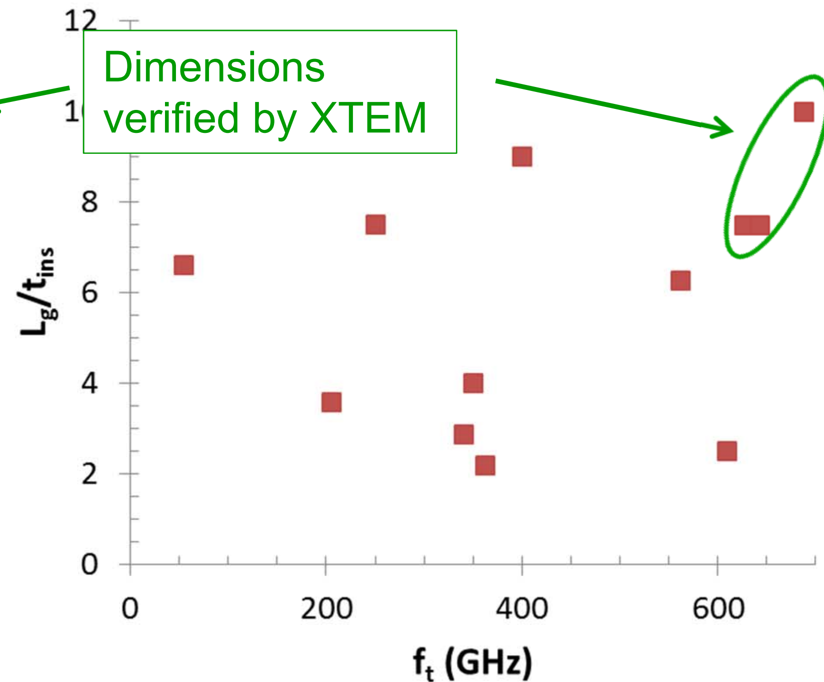
Zhou, EDL 2012

Harmonious scaling: aspect ratio of record f_t devices

Channel Aspect Ratio: L_g/t_{ch}



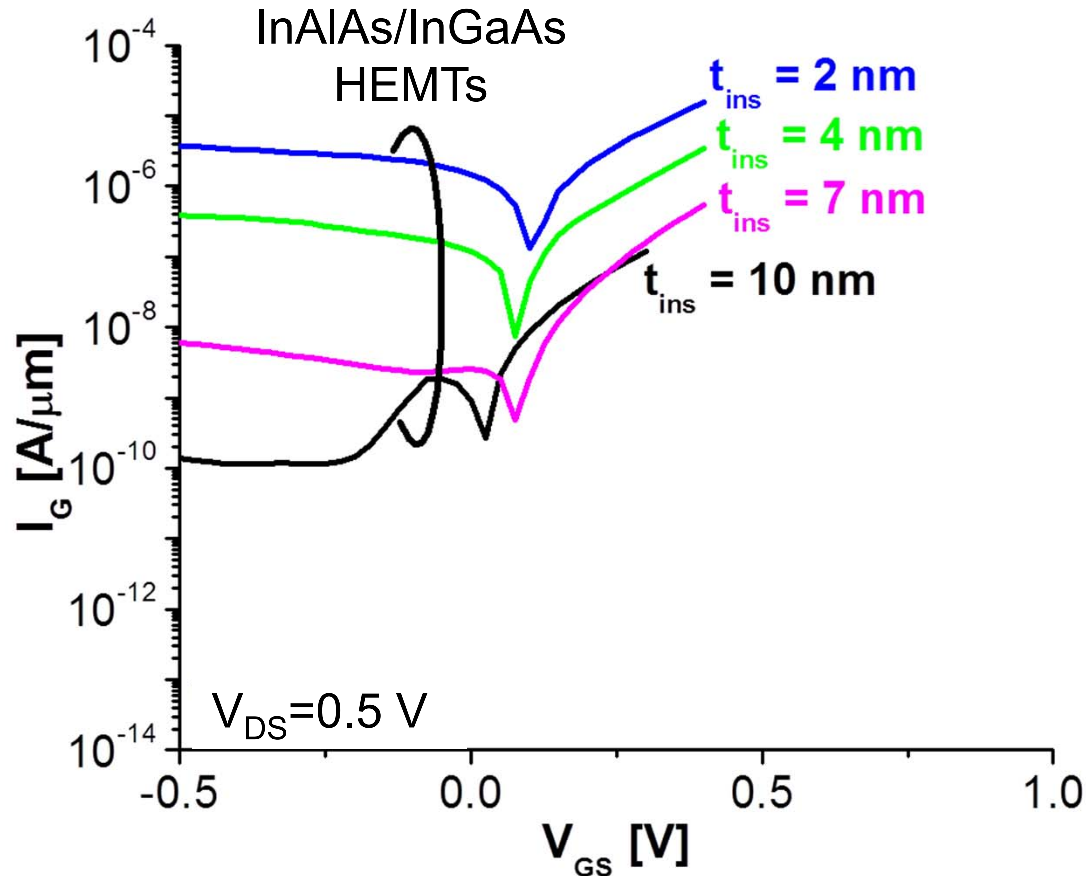
Insulator Aspect Ratio: L_g/t_{ins}

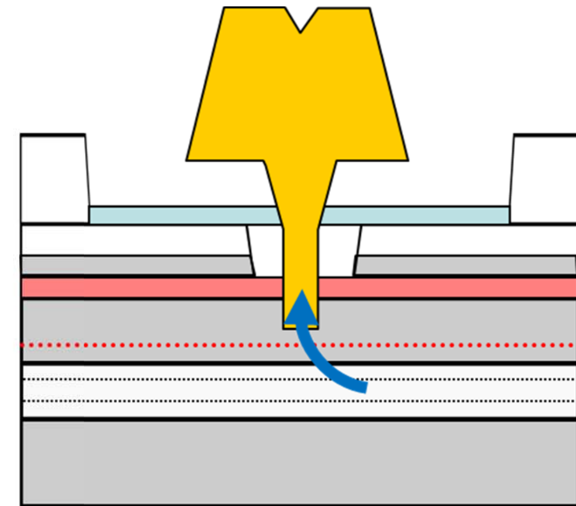


- *Channel AR*: 3 ~ 4
- *Insulator AR: 7 ~ 10*

For L_g=25 nm
→ t_{ch}~ 7 nm, t_{ins}~ 3 nm

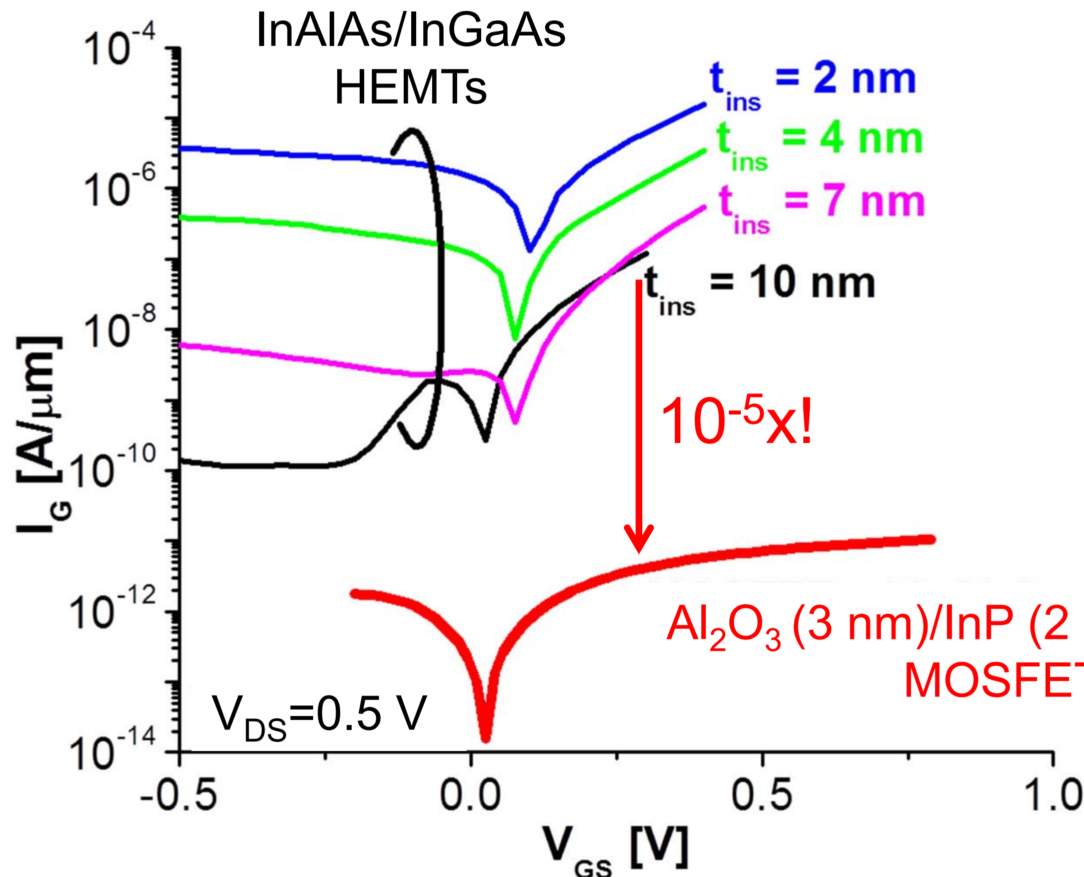
Limit to HEMT barrier scaling: gate leakage current

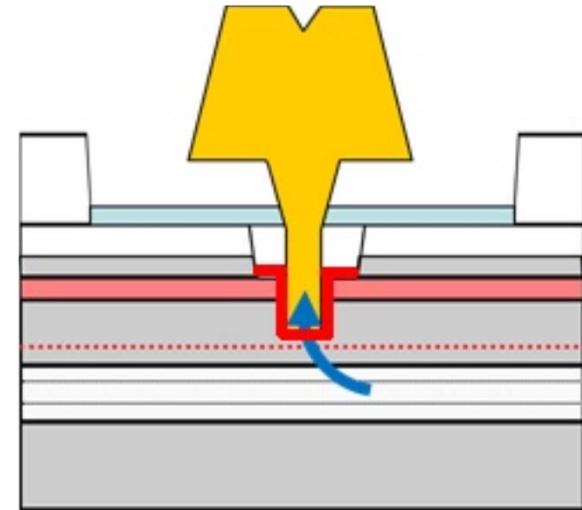




At L_g=30 nm, modern HEMTs are at the limit of scaling!

Limit to HEMT barrier scaling: gate leakage current





Need high-K gate dielectric: HEMT → MOSFET!

III-V MOSFET: deep scaling possible

InP (1 nm) + Al_2O_3 (0.4 nm) + HfO_2 (2 nm) → EOT ~ 0.9 nm

[*vs.* 4 nm InAlAs → EOT = 1.3 nm]

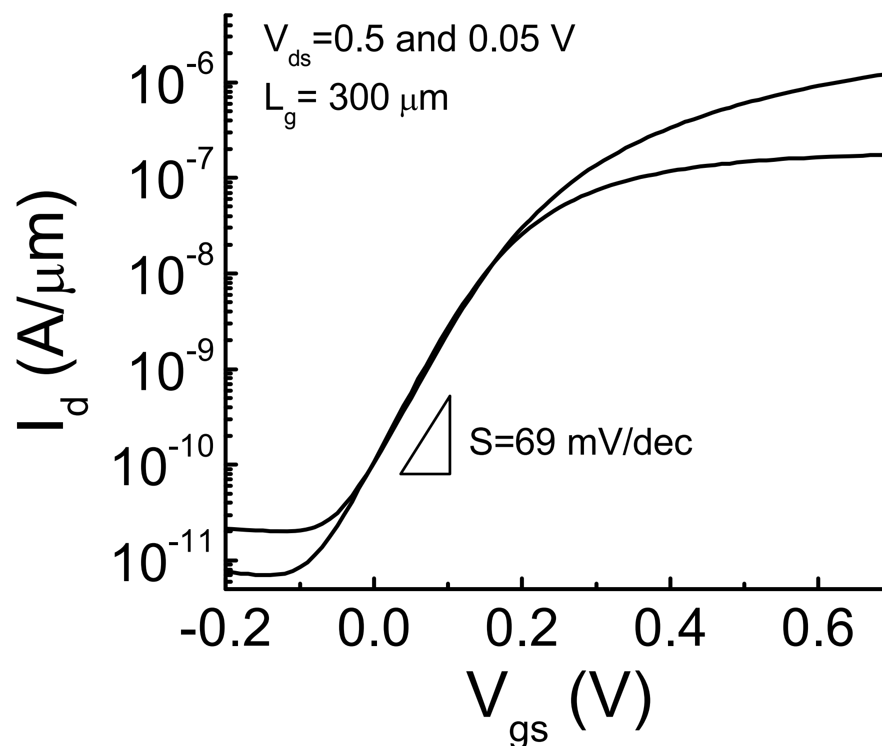
↑ Equivalent oxide thickness

→ should bring us to L_g=20 nm

Long-channel $In_{0.53}Ga_{0.47}As$ MOSFET

$\mu_e \approx 2700$ cm²/V.s

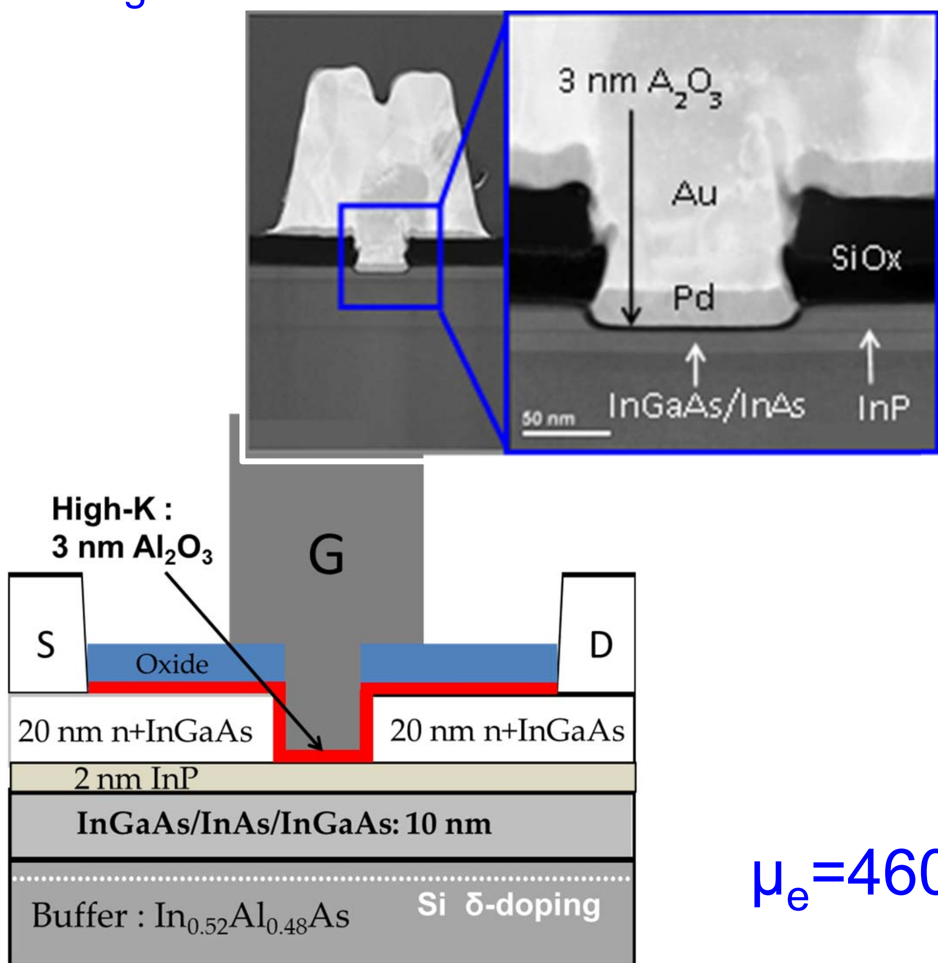
Lin, IEDM 2012



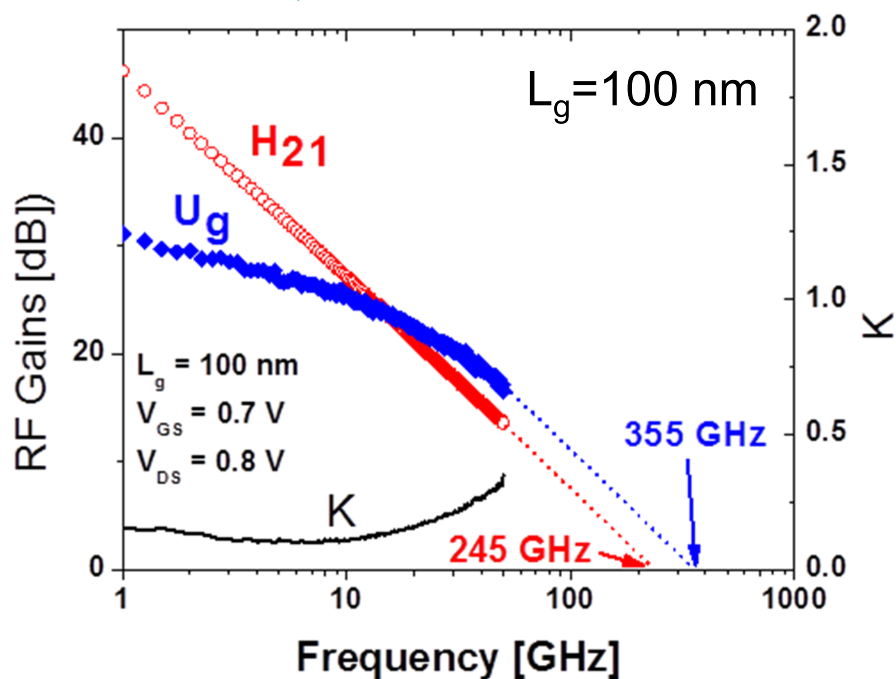
S=69 mV/dec → Low D_{it} at MOS interface demonstrated

High-frequency InGaAs MOSFETs

L_g=100 nm InGaAs MOSFET with L_{side}~5 nm, EOT=1.9 nm



Kim, VLSI Tech 2012



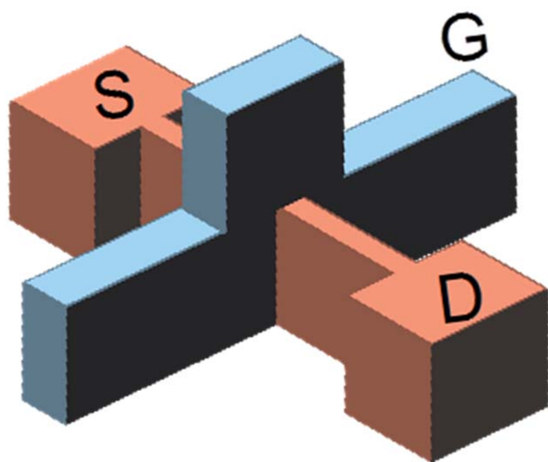
μ_e=4600 cm^2/V.s

f_t=245 GHz, R_{ON}=323 Ω.μm, g_m=1.7 mS/μm, S=105 mV/dec

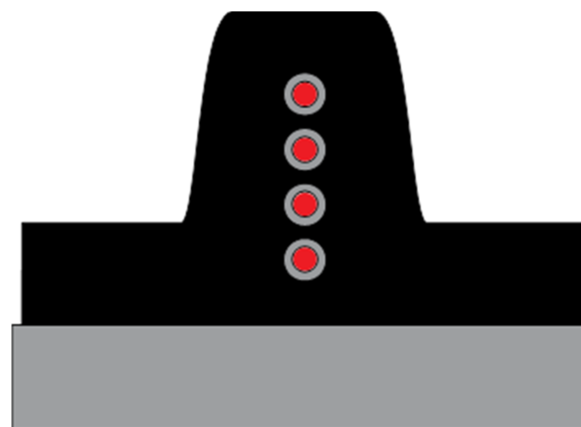
THz MOSFETs: possible designs

Etched S/D QW-MOSFET

Regrown S/D QW-MOSFET



FinFET



Gate-all-around nanowire FET

Conclusions

- THz III-V FETs just around the corner
  → need to reduce parasitics
  → need to scale harmoniously

- Exploding interest on III-V CMOS: huge opportunity for THz III-V electronics!
  → fast technology progress
  → new processes and tools
  → fundamental research on transport, interface, etc.
  → Si as substrate for THz electronics