InAs Quantum-Well MOSFET (L_g = 100 nm) for Logic and Microwave Applications

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Abstract

We report a recessed quantum-well (QW) InAs MOSFET with enhancement-mode operation down to 100 nm gate lengths. The device features a composite insulator consisting of an MBE-grown 2 nm InP barrier plus an ex-situ ALD-deposited 3 nm Al_2O_3 for an estimated EOT of 2 nm. Our devices exhibit excellent short-channel effects down to the L_g = 100 nm regime. InAs QW MOSFETs exhibit record transconductance g_m = 1.73 mS/μm and high-frequency performance (f_T = 245 GHz and f_{max} = 355 GHz). These are the highest values of f_T and f_{max} for any III-V MOSFET.

Introduction: III-V semiconductors have emerged as a promising channel material for future CMOS low power logic applications [1-2]. Their enhanced electron transport properties offer significant power reduction through aggressive supply power (V_{DD}) scaling. To maximize V_{DD} scaling for logic applications both transconductance ($g_{m,ext}$) and subthreshold slope (S) must be optimized. We report three significant advances towards these goals: first an InAs sub-channel to improve carrier transport, second an optimized gate stack process with thin EOT and low D_{it} to improve S, and third an improved layer structure with thin InP barrier (to reduce access resistance and surface depletion) and optimized Si δ-doping (to improve S and reduce R_{SD}).

Experimental: Fig. 1 and **Fig. 2** show a cross section of the device structure and a corresponding TEM image of an L_g = 100 nm device, respectively. From top to bottom, the epitaxial layer structure consists of a heavily doped cap (20 nm $In_{0.7}Ga_{0.3}As$) layer, 2-nm InP barrier, 10-nm $In_{0.53}Ga_{0.47}As/InAs/In_{0.53}Ga_{0.47}As$ composite channel, 5 nm $In_{0.52}Al_{0.48}As$ spacer, Si δ-doping, and 300-nm $In_{0.52}Al_{0.48}As$ buffer on InP substrate. The thin 2 nm InP barrier was introduced to reduce access resistance and improve charge control, EOT and immunity to short channel effects as well as to improve D_{it} [3]. The device also features a 5 nm thick InAs sub-channel to improve carrier transport and electron confinement in the channel. In a calibration sample, we measured $\mu_{e,Hall}$ = 11,200 cm^2/V-sec and $n_{s,ch}$ = 9 x $10^{11}/cm^2$ at 300 K.

Inverted Si δ-doping was used to supply carriers to the S/D access region and reduce R_{SD}. It is critical to carefully select the inverted Si δ-doping density to achieve the best trade-off of threshold voltage (V_T), subthreshold slope (S) and parasitics resistance (R_{SD}) [4]. **Fig. 3** shows channel carrier density as a function of gate potential for various Si δ-doping densities. The ability to modulate the channel carriers get worse as Si δ-doping increases, indicating that Si δ-doping needs to be carefully optimized, for acceptable subthreshold characteristics. In this work, we have chosen a value of 1 x $10^{12}/cm^2$, as the Si δ-doping, which resulted in both low R_{SD} and excellent electrostatic control. **Fig. 4** shows the corresponding conduction band profile with Si δ-doping = 1 x $10^{12}/cm^2$ at V_{GS} = 0 V.

Device fabrication was similar to that of a conventional HEMT [5], except for the deposition of a gate oxide prior to metal gate formation. After S/D ohmic contact with a 2 μm spacing, a gate pattern using single-layer ZEP-520A was defined by e-beam lithography. This was transferred to a passivating SiO_2 layer by CF_4 plasma. Subsequently, the cap was etched using a diluted citric acid based solution. After removing the e-beam resist, 3 nm of Al_2O_3 was deposited by ALD and the Pd/Au metal gate was evaporated. In this way, devices with L_g from 100 nm to 250 nm were fabricated.

Results and Discussion: Fig. 5 shows the device output characteristics demonstrating excellent pinch off and low R_{SD} (323 Ohm-μm). **Fig. 6** shows typical subthreshold characteristics with L_g from 100 nm to 250 nm. These devices show excellent subthreshold behavior and I_{ON}/I_{OFF} ratio (~10^4) down to L_g = 100 nm. The gate leakage (I_g) is lower than 0.1 nA/μm at all measured bias conditions. InAs QW MOSFET with L_g = 100 nm exhibits V_T = +0.2 mV (defined as I_D = 1μA/μm) and subthreshold swing (S) = 105 mV/dec at V_{DS} = 0.5 V. This results in an I_{OFF} = 5 X 10^{-8} A/μm at V_{GS} = 0 V and V_{DS} = 0.5 V. The attainment of this value in a device with low resistance parasitics and excellent subthreshold swing is significant because this is the first time that these three features are shown in combination in an III-V MOSFETs.

Fig. 7 shows typical transconductance characteristics at V_{DS} = 0.5 V. The InAs QW MOSFET exhibits $g_{m,max}$ > 1.73 mS/μm at V_{DS} = 0.5 V. This is a record transconductance for a III-V MOSFET of this gate length and V_T and is mainly due to the well optimized Si δ-doping density that contributes to reduced access resistance and the high electron mobility associated with the InAs subchannel.

Microwave performance was characterized from 0.5 GHz to 50 GHz. On-wafer open and short patterns were used to subtract pad parasitics from the measured device

S-parameters. **Fig. 8** plots h_{21}, U_g and stability-factor (k) against frequency InAs MOSFET with W_g = 2 x 20 µm and L_g = 100 nm, at V_{GS} = 0.7 and V_{DS} = 0.8 V. We obtain a current-gain cut-off frequency f_T = 245 GHz and a maximum oscillation frequency f_{max} = 355 GHz. These are record values among III-V MOSFETs of similar gate length. The device also exhibits f_T = 238 GHz at V_{DS} = 0.5 V. Small-signal parameter extraction from measured S-parameters gave good consistency between DC and RF transconductance.

Conclusions: We have demonstrated L_g=100 nm recessed enhancement-mode quantum-well InAs MOSFETs with a composite Al_2O_3/InP gate stack. L_g = 100 nm devices exhibit outstanding logic characteristics, with S = 105 mV/dec, V_T = 0.2 V, I_{OFF} = 5 X 10^{-8} A/µm and $g_{m,max}$ > 1.73 mS/µm at V_{DS} = 0.5 V. In addition, our devices show record f_T = 245 GHz and f_{max} = 355 GHz. These results emerge from a well optimized inverted Si δ-doping, ALD high-k deposition and high mobility InAs channel design.

Reference:

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[4] T.-W. Kim *et al.*, IEDM, p. 483 (2009).
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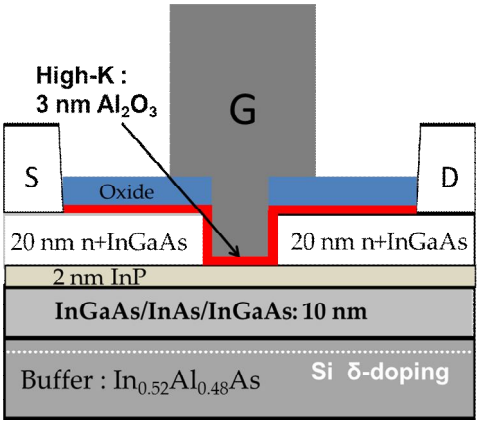

Fig. 1: Cross-sectional schematic of QW device with 3 nm ALD Al_2O_3, 2 nm InP barrier and InAs composite channel.

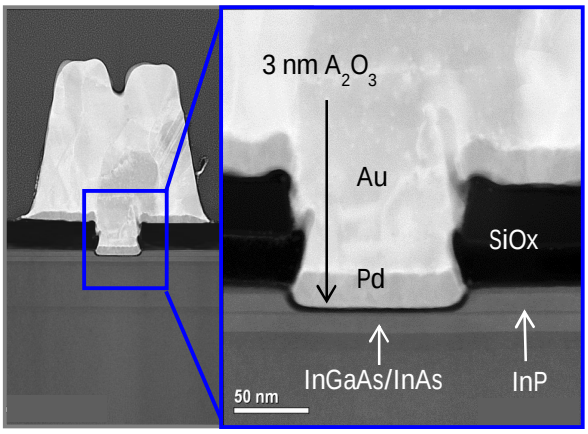

Fig. 2: TEM cross-section of fabricated device. Note well optimized recess with minimal L_{side}

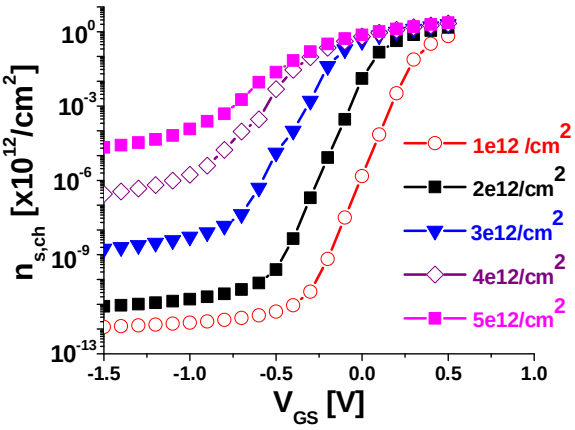

Fig. 3: 1D Poisson-Schrödinger simulations of channel electron density as a function of gate bias for different Si delta-doping concentrations. High δ-doping density limits charge modulation.

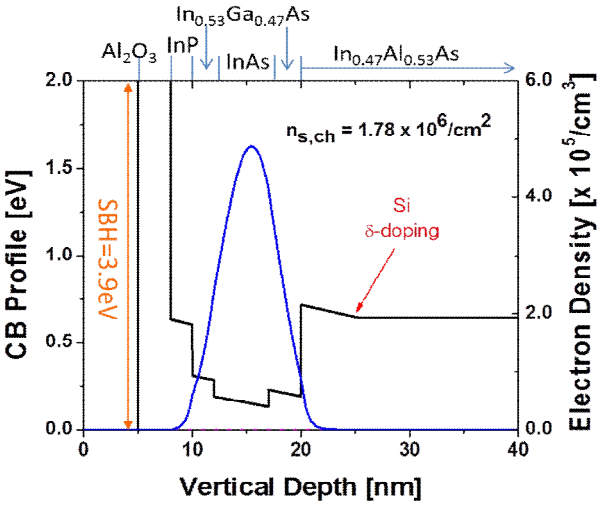

Fig. 4: 1D Poisson-Schrödinger simulation of conduction band profile and electron wave-function at VGS=0 V.

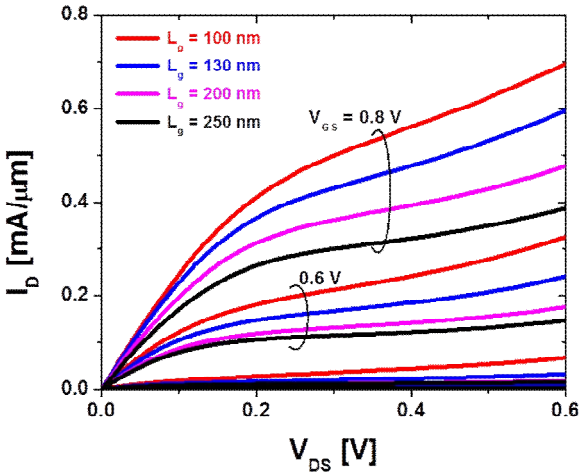

Fig. 5: I_dV_d output characteristics showing excellent charge control and low series resistance (323 Ω-μm).

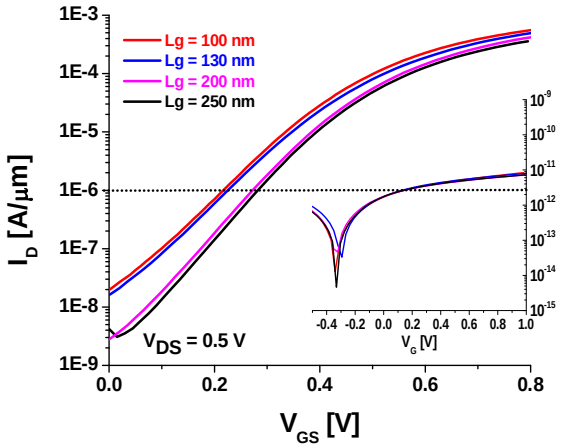

Fig. 6: Semi-log scale I_dV_g L_g = 100 nm device has SS of 105 and I_{on}/I_{off} >1000.

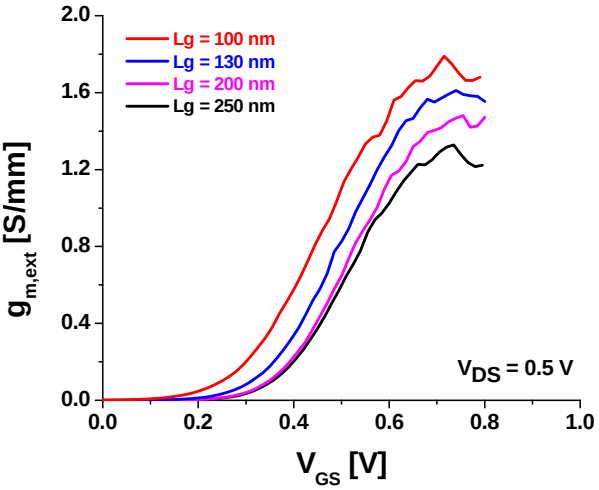

Fig. 7 $g_{m,ext}$ vs. V_G. L_g = 100 nm device has $g_{m,max}$ = 1.73 mS/μm

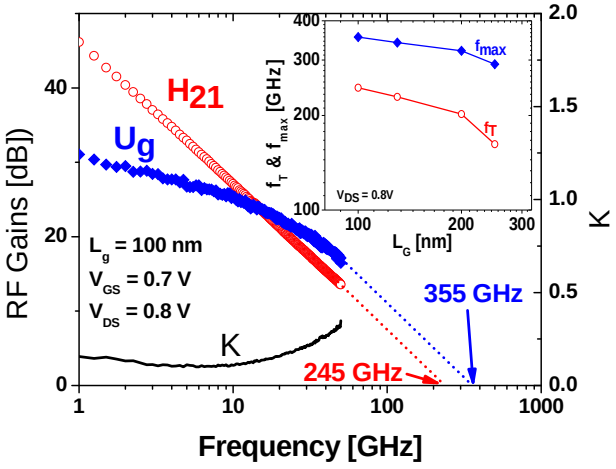

Fig. 8 Microwave characteristics of Lg = 100 nm InAs MOSFET with the highest fT = 245 GHz and fmax = 355 GHz of any III-V MOSFET