Proceedings of the 2012 24th International Symposium on Power Semiconductor Devices and ICs
3-7 June 2012 - Bruges, Belgium

Mechanisms responsible for dynamic ON-resistance in GaN high-voltage HEMTs

Donghyun Jin and Jesús A. del Alamo
Electrical Engineering and Computer Science
Massachusetts Institute of Technology
Cambridge, MA, USA 02139
jinnara@mit.edu

***Abstract*—We have developed a new methodology to study the dynamic ON-resistance (R_{ON}) of high-voltage GaN High-Electron-Mobility Transistors (HEMTs). With this technique, we have investigated dynamic R_{ON} transients over a time span of 11 decades. In OFF to ON time transients, we observe a fast release of trapped electrons through a temperature-independent tunneling process. We attribute this to border traps at the AlGaN barrier/AlN spacer interface. Over a longer time scale, we observe conventional thermally activated electron detrapping from traps at the surface of the device or inside the AlGaN barrier. These findings provide a path for power switching device engineering with minimum dynamic R_{ON}.**

Keywords- dynamic ON-resistance, GaN, HEMT, border traps

I. INTRODUCTION

The GaN HEMT is a very promising device for power-switching applications due to the outstanding breakdown electric field of GaN and the high sheet electron density attainable at the AlGaN/GaN interface. A critical requirement in power electronics is obtaining a very low ON resistance (R_{ON}) immediately after switching from a high-voltage OFF state to a low-voltage ON state. In the much more mature RF power GaN HEMTs, dynamic switching problems such as current collapse, gate lag and drain lag are often present and detract from RF power performance [1]. In power switching applications, these same issues would manifest themselves as a dynamic ON resistance in which after an OFF-ON switching event, R_{ON} remains high for a period of time [2]. To date, there has been little research on this important issue [3].

In this work, we have performed a fundamental study of dynamic R_{ON} on high-voltage GaN HEMTs with the goal of elucidating the key mechanisms. We find that on a short time scale, dynamic R_{ON} is limited by a mechanism that is consistent with detrapping of border traps in the AlGaN barrier close to the GaN channel. These traps release their electrons through a tunneling process and are most likely interface states at the AlN spacer/AlGaN barrier interface. Dynamic R_{ON} on a longer time scale is limited by conventional energy activated detrapping processes from traps in the AlGaN or at the surface. These can be engineered through appropriate growth techniques.

II. PROPOSED TECHNIQUE

For this study, we have developed a new dynamic ON-resistance measurement methodology that is capable of collecting R_{ON} transients from 200 ns to any arbitrary length of time. For this we use two different instruments: an Auriga AU4750 pulsed IV system for short times and an Agilent B1500A semiconductor device analyzer (SDA) for longer times. In both cases, synchronous switching of V_{GS} and V_{DS} is performed. With the pulsed IV system, we successively switch from an OFF-state quiescent (Q) bias to an ON state given by V_{GS}=1 V and V_{DS} between 0.05 and 0.6 V and we measure the linear drain current. The duty cycle is 10%. Fig. 1 shows a typical measured I_D waveform. The instantaneous R_{ON} can be extracted from the slope of I_D vs. V_{DS} (inset). In this way, we measure R_{ON} transients from 200 ns up to 3 ms. The synchronous pulsed mode of the B1500A allows us to complete the transient from 3 ms to any arbitrary time. Fig. 2 shows two examples of transients

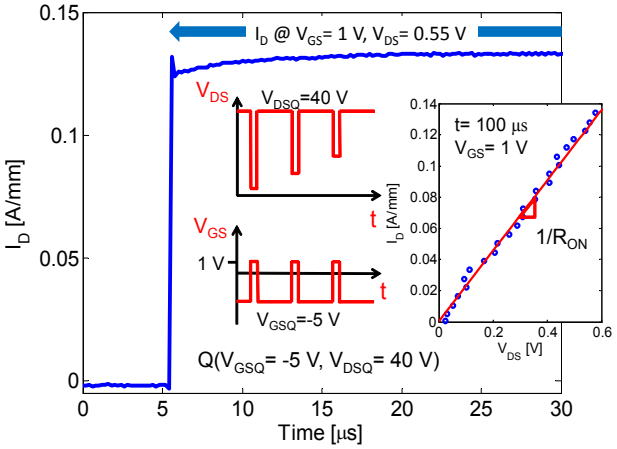

Fig. 1 I_D waveform measured by pulsed IV system. The device is synchronously switched from an OFF-state quiescent bias of V_{GSQ}=-5 V, V_{DSQ}=40 V to an ON-state of V_{GS}=1 V and V_{DS} changing from 50 mV to 0.6 V. R_{ON} can be extracted from the slope of I_D vs V_{DS} as shown in the inset.

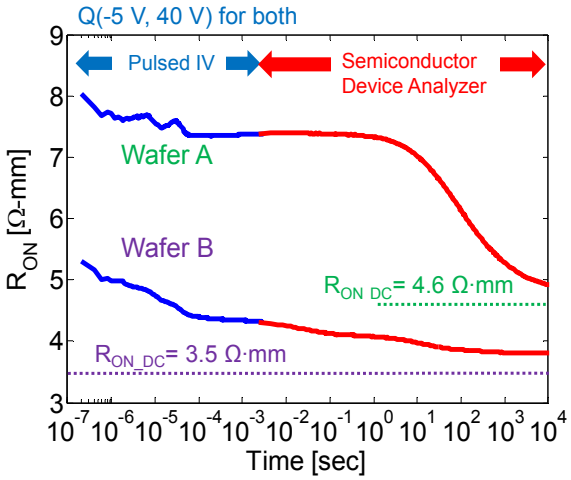

Fig. 2 R_{ON} transients from 200 ns up to 10,000 s on wafer A and B devices from V_{GSQ}=-5 V, V_{DSQ}=40 V. Blue lines are obtained from pulsed IV system (Auriga AU4750) and red lines from semiconductor device analyzer (Agilent B1500A). Also shown are the DC values of R_{ON} obtained after fully detrapping the device. Wafer A shows 73% higher R_{ON} at 200 ns than in DC (marked as $R_{ON\ DC}$) and Wafer B shows a 52% increase.

obtained over 11 decades in time. The blue lines are measured from the pulsed IV system and the red ones come from SDA. Also shown are the DC values of R_{ON} obtained after fully detrapping the device under visible light illumination. We analyze the time domain data by fitting it to a sum of exponentials and generating a time-constant spectrum [4].

III. Experiments

In our experiments, we have characterized industrially prototyped AlGaN/GaN HEMTs fabricated on two nominally identical epitaxial wafers (labeled A and B) grown by MOCVD on SiC by two different commercial epitaxial vendors. The heterostructure includes a GaN cap and an AlN spacer. Both wafers were processed in the same lot. The device features an integrated field plate and a source-connected field plate. The breakdown voltage of devices on wafer A is around 160 V and for wafer B is higher than 200 V.

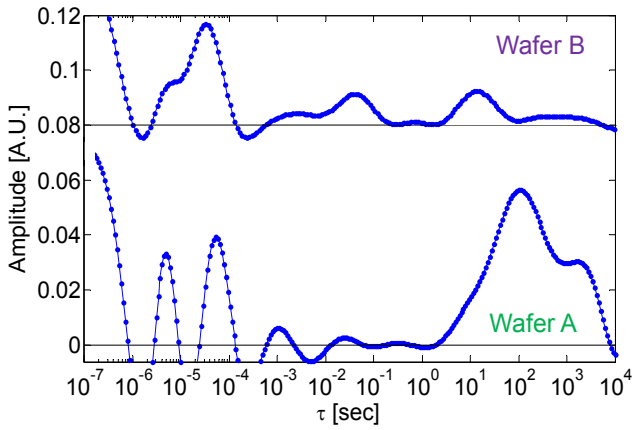

Fig. 3 Time-constant spectra for R_{ON} transients in Fig. 2. A sum of exponential terms with time constants ranging from 10^{-7}s to 10^{4}s is used to fit the measurement data. Wafer A device exhibits prominent time constants in the 10 to 1000 s range. These are much weaker in wafer B. In both devices, there are prominent time constants in the sub-us to ms range.

Fig. 2 shows R_{ON} transients when the devices are switched from an OFF-state with V_{GSQ}=-5 V and V_{DSQ}=40 V. In wafer A, R_{ON} at 200 ns is about 73% higher than in DC. Such a high dynamic R_{ON} represents a big problem for power switching applications. For wafer B, R_{ON}(200 ns) is about 52% higher than R_{ON_DC}. The pattern of recovery of R_{ON} is also very different in both wafers. Wafer A exhibits a very slow transient in the s-ks time range, while wafer B recovers on a us-s time scale.

Fig. 3 shows the time constant spectrum for both samples [4]. The wafer A device exhibits two prominent time constants in the 10 to 1000 s range. These are much weaker in wafer B. Both wafers show multiple time constants in the sub-us to ms range.

We have performed dynamic R_{ON} measurements at ambient temperatures between 5 C and 200 C (Figs. 4 and 5). On wafer A, the dominant transients substantially speed up as T is increased. On wafer B, the transients change little with T. We have plotted the evolution of the dominant time constants with T in Arrhenius plots (Fig. 6 and 7). For both wafers, two distinct patterns emerge: a set of long time constants with thermally activated behavior and another set of short time constants that are independent of temperature. The long thermally-activated time

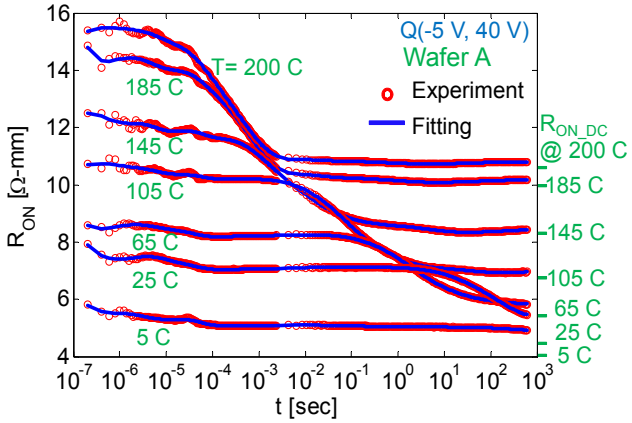

Fig. 4 R_{ON} transients on wafer A device at different ambient temperatures for V_{GSQ}=-5 V and V_{DSQ}=40 V. Red dots indicate measurement data and the blue solid lines are fitting curves generating the time constant spectrum. R_{ON_DC} on the right hand side indicates fully detrapped R_{ON} value. On wafer A, the dominant transients substantially speed up as T increases.

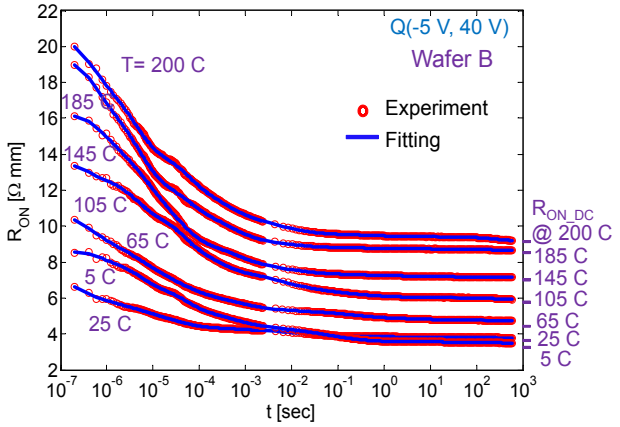

Fig. 5 R_{ON} transients on wafer B device at different ambient temperatures for V_{GSQ}=-5 V and V_{DSQ}=40 V. R_{ON_DC} on the right hand side indicates the fully detrapped R_{ON} value. On wafer B, the transients depend little on temperature.

constants can be associated with conventional traps. On wafer A, the dominant traps are at 0.79 eV, 0.82 eV, and 0.76 eV below the conduction band edge. On wafer B, a much weaker but richer spectrum of traps with energies between 0.57 and 1.12 eV is observed. Traps at similar energies have been reported by other authors in similar structures [5-6].

These results suggest that there are at least two distinct mechanisms that dominate dynamic R_{ON} transients at short times and at long times. The long time transients are associated with conventional traps. The noticeable differences in wafers A and B indicate that these can be engineered through proper growth protocols. The short time transients are associated with a different mechanism and both wafers suffer from it in a similar amount. This suggests that they might be associated with an intrinsic aspect of the heterostructure.

We have also carried out OFF to ON transients from different quiescent V_{DS} values, as shown in Fig. 8 for wafer B. As V_{DSQ} increases, the dynamic R_{ON} increases in a prominent manner in both devices presumably as a result of the increased extension of the high-field region into the drain. The inset shows that the relative increase of R_{ON} at 200 ns is similar in both wafers.

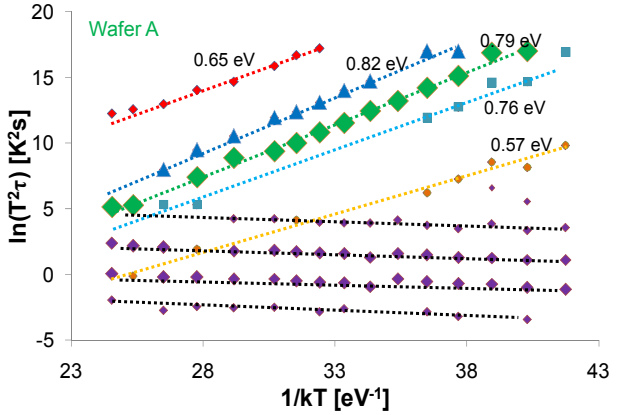

Fig. 6 Arrhenius plot of time constant spectrum extracted from wafer A device. The size of the symbols is proportional to the height of the time constant peak. Dominant traps at 0.79 eV, 0.82 eV, and 0.76 eV are identified. A set of short time constants which are independent of temperature is also observed. They are responsible for the fast transients.

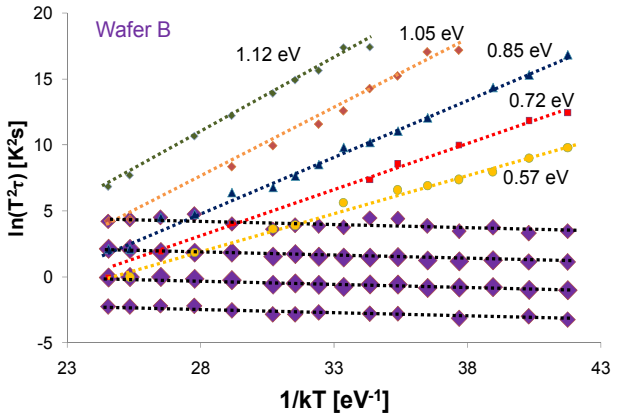

Fig. 7 Arrhenius plot of time constant spectrum extracted from wafer B device. The size of the symbols indicates the height of the time constant peak. A rich spectrum of traps with activation energies between 0.57 eV and 1.12 eV is observed but their concentration is much lower than in wafer A. The dominant time constants in wafer B are short and do not exhibit any temperature dependence.

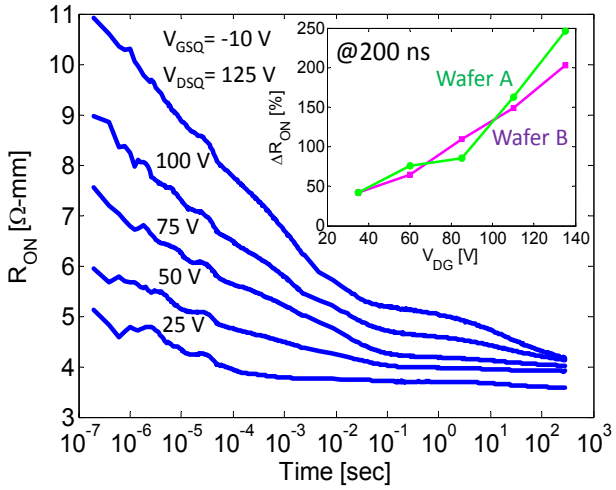

Fig. 8 OFF to ON state transients from different quiescent V_{DS} conditions from V_{DSQ}=25 V up to 125 V in 25 V increments (wafer B device). As V_{OFF} increases, the dynamic R_{ON} increases too but the time constants do not change. The inset indicates the % increase of dynamic Ron with V_{DSQ} at 200 ns on both wafers.

To further clarify the physics, we have also performed high-power (HP) to ON transients. Figs. 9 and 10 illustrate R_{ON} transients from a quiescent bias of V_{GS}=2 V, V_{DS}=7 V (5.4 W/mm) at different ambient temperatures. In both wafers, the transients are T independent and dominated by fast time constants. There is no hint of slow thermally-activated transients. This rules out any kind of buffer trapping. It also shows that the slow thermal detrapping that is most visible in wafer A during OFF-ON transients is not accessible in this mode.

We have also performed HP to ON transients at different V_{DG} but same power dissipation (Fig. 11). These reveal that the fast transients are not related to thermal cooling of the device but are strongly enhanced by the quiescent voltage V_{DGQ}. In fact, R_{ON} at 200 ns follows a hot-electron type law (inset in Fig. 11) suggesting that the electrons that are released during these fast transients became trapped after acquiring kinetic energy from the high field in the channel.

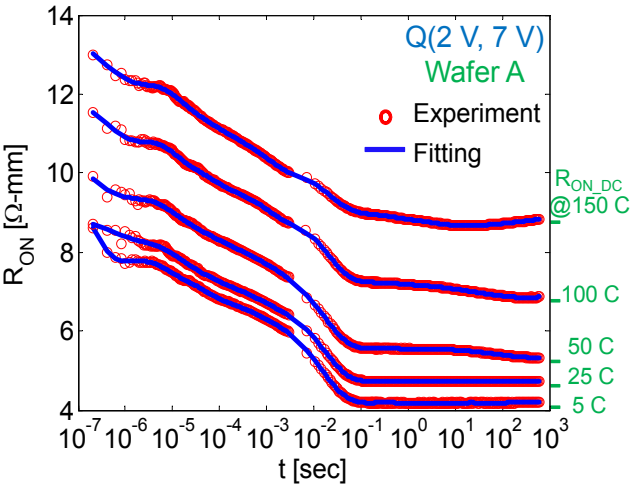

Fig. 9 High power to ON-state transients on wafer A devices at different ambient temperatures. The high power state bias is V_{GSQ}=2 V and V_{DSQ}=7 V (5.4 W/mm). The transients are dominated by T-independent fast time constants. No thermally activated slow-transients are observed.

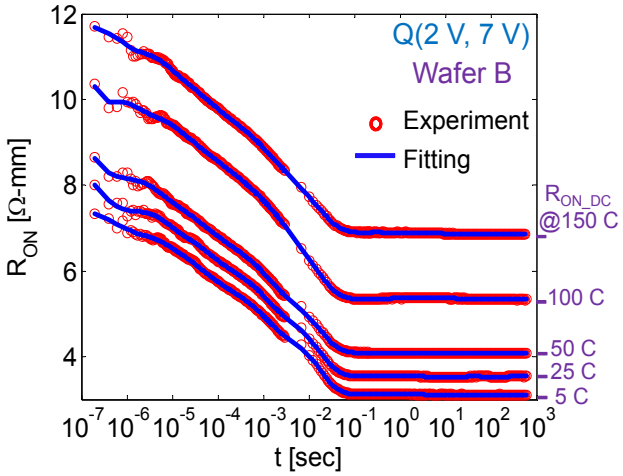

Fig. 10 High power to ON-state transients on wafer B devices vs ambient temperature. The high power state is V_{GSQ}=2 V and V_{DSQ}=7 V. As in Fig. 9, the transients are dominated by T-independent fast time constants.

IV. Mechanisms Responsible for Dynamic R_{ON}

A consistent picture thus emerges (Fig. 12). In a short time scale, the R_{ON} transient is dominated by a temperature independent release of electrons, most likely detrapping through a tunneling process. These traps can be charged in the OFF state through the gate current and in the high-power state through hot electrons from the channel. These traps exist in a similar amount in both wafers. A most likely origin for these traps that is consistent with all observations is interface states at the AlGaN/AlN spacer interface. This interface is known to harbor interface states [7]. Traps that are physically located inside a barrier but very close to the channel and that release their electrons through a tunneling process are known as *border traps* [8]. We postulate that AlGaN/AlN interface states behave as border traps as the AlN layer is very thin. The longer thermally-activated time transients are associated with conventional traps at the surface or inside the AlGaN barrier. These are accessible from the gate in the OFF state but not from the channel in the high-power state because of the energy barrier associated with the AlGaN. To some extent, these traps can be engineered through proper growth procedures.

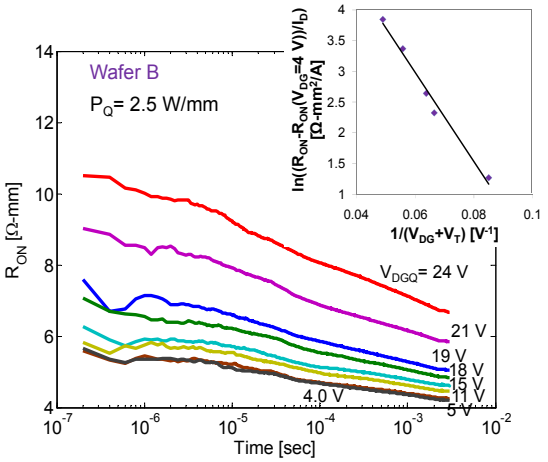

Fig. 11 HP to ON transients from quiescent points at different V_{DGQ} but with the same power dissipation. Dynamic R_{ON} at 200 ns increases exponential following a hot-electron type law as shown in the inset.

V. Conclusions

In summary, we have investigated dynamic R_{ON} transients over 11 decades of time in high-voltage GaN HEMTs. In OFF-ON time transients, we have identified two distinct mechanisms. On a short time scale, we observe the fast release of electrons from border traps that we postulate are associated with the AlGaN barrier/AlN spacer interface. On a longer time scale, conventional thermally assisted detrapping is observed from traps at the surface or inside the AlGaN barrier. These can be engineered through the epi growth process. These findings provide a path for power switching device engineering with minimum dynamic R_{ON} problems.

Acknowledgment

This research is supported in part by U.S. Department of Energy in the context of the ARPA-E ADEPT program, by the Semiconductor Research Corporation and by the DRIFT MURI under an ONR Grant.

References

[1] S. C. Binari, *et al.*, "Trapping effects in GaN and SiC microwave FETs," Proc. IEEE, vol. 90, No.6, pp. 1048-1058, June 2007.

[2] W. Saito, *et al.*, "Suppression of dynamic on-resistance increase and gate charge measurements in high-voltage GaN-HEMTs with optimized field-plate structure," IEEE Trans. Electron Devices, vol. 54, No.8, pp. 1825-1830, August 2007.

[3] R. Chu, *et al.*, "1200-V normally off GaN-on-Si field-effect transistors with low dynamic on-resistance," IEEE Electron Dev. Lett., vol. 32, No.5, pp. 632-634, May 2011.

[4] J. Joh and J. A. del Alamo, "A current-transient methodology for trap analysis for GaN high electron mobility transistors," IEEE Trans. Electron Devices, vol. 58, No. 1, pp. 132-140, January 2011.

[5] A. R. Arehart, *et al.*, "Spatially-discriminating trap characterization methods for HEMTs and their application to RF-stressed AlGaN/GaN HEMTs," in IEDM Tech. Dig., 2010, pp. 464-467.

[6] A. Sozza, *et al.*, "Evidence of traps creation in GaN/AlGaN/GaN HEMTs after a 3000 hour on-state and off-state hot-electron stress," in IEDM Tech. Dig., 2005, pp. 589-593.

[7] S. A. Vitusevich *et al.*, "Low-frequency noise in AlGaN/GaN HEMT structures with AlN thin film layer," Phys. Stat. Sol. (c), Vol. 3, No. 6, pp. 2329-2332, May 2006.

[8] D. M. Fleetwood, *et al.*, "Estimating oxide-trap, interface-trap, and border-trap charge densities in metal-oxide-semiconductor transistors," Appl. Phys. Lett, Vol. 64, No. 15, pp. 1965-1967, April 1994.

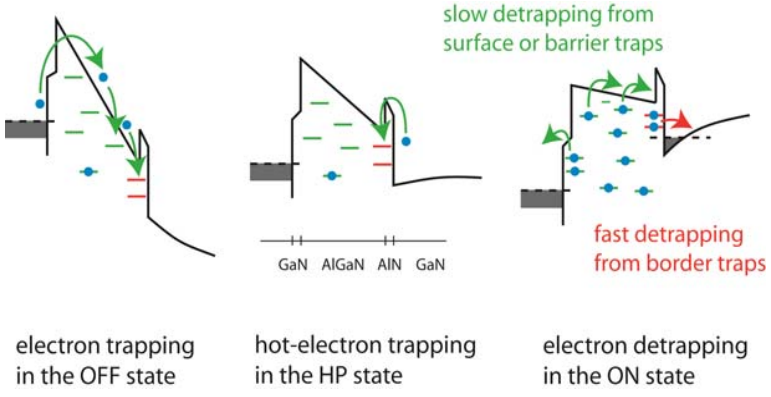

Fig. 12 Mechanisms responsible for dynamic R_{ON} in GaN HEMTs. In the OFF state, trapping at the surface, in the AlGaN and at the AlGaN/AlN interface takes place through I_G. In the HP state, hot electrons from the channel are trapped at AlGaN/AlN interface states. In the ON state, electron detrapping takes place thermally for traps in the AlGaN or at the surface and through a tunneling process for AlGaN/AlN interface traps (border traps).