REVIEW

doi:10.1038/nature10677

Nanometre-scale electronics with III–V compound semiconductors

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For 50 years the exponential rise in the power of electronics has been fuelled by an increase in the density of silicon complementary metal–oxide–semiconductor (CMOS) transistors and improvements to their logic performance. But silicon transistor scaling is now reaching its limits, threatening to end the microelectronics revolution. Attention is turning to a family of materials that is well placed to address this problem: group III–V compound semiconductors. The outstanding electron transport properties of these materials might be central to the development of the first nanometre-scale logic transistors.

The microelectronics revolution might best be characterized by the motto 'smaller is better'. A unique attribute of the silicon metal–oxide–semiconductor field-effect transistor (MOSFET), the workhorse of the industry, is that its logic characteristics improve as its dimensions are reduced[1]. When it comes to logic operations, a transistor behaves as a switch, and its most important qualities, after its footprint, are switching speed and switching energy. Because MOSFETs have decreased in size following a geometrical law, switching speed and transistor density have increased exponentially, while switching energy has decreased in a similar fashion[2,3]. These 'triple dividends' of MOSFET scaling have powered the microelectronics revolution.

Modern logic circuits are based on a pair of transistors with complementary characteristics. They are referred to as n-type and p-type MOSFETs (or simply NMOS and PMOS transistors). Together they are known as complementary metal–oxide–semiconductor (CMOS) transistors and have been the dominant logic family because their simplicity and unique low-power characteristics have allowed the synthesis of very dense circuits.

Recently, MOSFET scaling entered a phase of 'power-constrained scaling' as the power density dissipated by logic chips hit about 100 W cm^{-2} (ref. 4). Power density cannot increase much further without incurring substantial packaging and cooling costs that make these chips impractical for most applications. Continued progress in transistor density will require a reduction in the operating voltage[3–5], but this will compromise switching speed. This problem is partly why the operating voltage for CMOS transistors has bottomed out at around 1 V for some time[3]. Without further reductions, future scaling may not be feasible.

One possible solution is to introduce a new channel material in which charge carriers travel at a much higher velocity than in silicon. This would allow a reduction in voltage without a loss of performance. And this is why attention is turning to III–V compound semiconductors.

The III–V compound semiconductors, such as GaAs, AlAs, InAs, InP and their ternary and quaternary alloys, combine elements in columns III and V of the periodic table. Some III–V compounds have unique optical and electronic properties. Their ability to efficiently emit and detect light means they are often used in lasers, light-emitting diodes and detectors for optical communications, instrumentation and sensing. A few, notably GaAs, InGaAs and InAs, exhibit outstanding electron transport properties. Transistors based on these materials are at the heart of many high-speed and high-frequency electronic systems[6]. In fact, there is a large and mature industry manufacturing III–V integrated circuits in great volumes for applications as diverse as smart phones, cellular base stations, fibre-optic systems, wireless local-area networks, satellite communications, radar, radioastronomy and defence systems. The recent widespread use of handheld devices and their enormous consumption of data has been a boon to the III–V integrated-circuit industry, which is now characterized by highly automated and rigorous large-scale manufacturing, relatively large-area wafers, sophisticated device and circuit design tools, well-established device reliability, and a rich and competitive industrial ecosystem. No other family of materials currently being considered to replace the silicon channel in a MOSFET has such an impressive list of attributes.

Today, III–V CMOS technology is a mainstream part of semiconductor research. Their future role has recently been recognized in the *International Technology Roadmap for Semiconductors*[7].

Here I outline the case for III–V CMOS technology, discuss the most critical problems that remain to be overcome, and summarize recent progress made in the field.

The rationale for using III–V compounds

The case for III–V CMOS technology is often made by drawing attention to the extraordinary electron mobility of certain III–V compounds (Fig. 1). In InGaAs or InAs, the electron mobility is more than 10 times higher than in silicon at a comparable sheet density. The outstanding frequency response of III–V transistors is also frequently invoked. For example, current-gain and power-gain cutoff frequencies of InGaAs-based high-electron-mobility transistors (HEMTs) — a well-established transistor design in its own right — exceed 600 GHz and 1 THz, respectively[8–10]. Impressive as these attributes are, such arguments do not address what really matters for a logic transistor.

A logic transistor operates as a switch that toggles between an 'on' state and an 'off' state. For fast switching, a high on current (I_{ON}) is desired. To limit standby power consumption, the off current (I_{OFF}) must be minimized. It is in terms of I_{ON} and I_{OFF} that the suitability of a transistor for logic should be assessed (for these and other definitions, see Fig. 2 in the Review by Colinge and colleagues[1]).

In an NMOS transistor in saturation, I_{ON} is determined by the product of the sheet electron concentration and the electron injection velocity, v_{inj}, at the 'virtual source'[11], the location on the channel that presents the highest energy barrier in the conduction band. This is the bottleneck to electron flow.

We can learn about the injection velocity of future III–V transistors by

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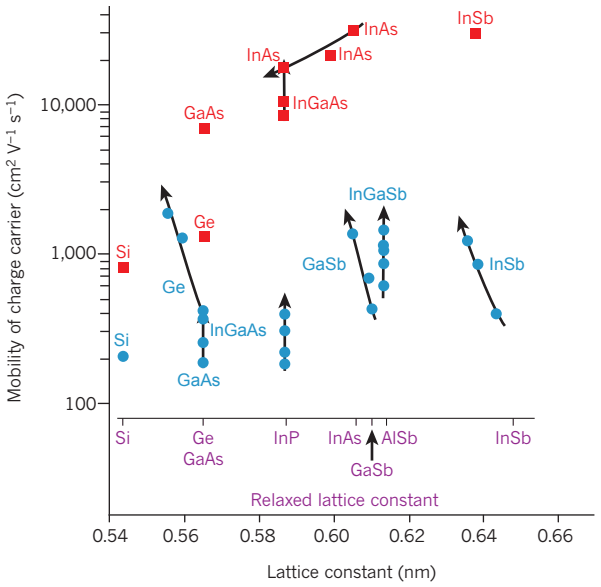

Figure 1 | Electron and hole mobility of group III–V compound semiconductors. The highest room-temperature mobility of electrons (red) and holes (blue) in inversion layers and quantum wells is shown as a function of the actual semiconductor lattice constant (side length of a cubic unit cell of a semiconductor crystal). The mobilities are reported for any sheet carrier concentration. For relaxed layers, under no strain, the lattice constant is its natural one, as shown on the scale. For pseudomorphic layers, which are perfectly strained on a substrate with a different lattice constant, the lattice constant is that of the substrate. As a result, points marked with the same label may appear in different locations in the figure. The impact of biaxial strain is indicated by an arrow representing increasing compressive biaxial strain. There is a wide gap between electron and hole mobilities among III–V compound semiconductors at any lattice constant, and compressive biaxial strain plays a large role in bridging this gap.

examining III–V HEMTs. In this regard, HEMTs provide an excellent model system to study issues of importance in future III–V MOSFETs[12].

Measurements in InGaAs and InAs HEMTs[13] have revealed values for v_{inj} that approach 4×10^7 cm s^{-1} at 0.5 V (Fig. 2). This value of voltage has been selected to compare future technology options because it delivers a sizeable reduction in power dissipation from the present supply of 1 V. In the III–V HEMTs in Fig. 2, v_{inj} is more than twice that of comparable silicon MOSFETs at less than half the voltage[14]. For devices shorter than about 50 nm, the injection velocity becomes independent of gate length. Monte Carlo simulations indicate that electron transport through the channel takes place in a ballistic fashion, that is, with almost no collisions[15]. In this instance, the injection velocity is determined by the band structure of the channel material (Fig. 2), and v_{inj} increases with InAs composition in the channel as a result of a lower electron effective mass[13].

Sheet carrier concentration also affects I_{ON}. Concerns have been expressed about the limitation that a low effective mass imposes on the maximum sheet electron concentration that can be obtained[16]. Recent measurements in InGaAs and InAs HEMTs suggest that the electron effective mass is significantly greater than the bulk value[17]. This is explained by the strong non-parabolicity of the conduction band of these materials, coupled with electron quantization in the thin channel and biaxial compressive stress from lattice mismatch with the InP substrate.

The combination of a high v_{inj} and reasonable channel density of states confers InGaAs and InAs 'quantum-well' FETs with the potential to deliver outstanding I_{ON} at a low supply voltage, V_{DD}, something essential in future CMOS transistors.

But I_{OFF} is just as important as I_{ON}. In quantum-well devices without source and drain junctions, such as HEMTs, I_{OFF} is set by the subthreshold swing, S, which quantifies the sharpness of the drop of the drain current below threshold. In InAs and InGaAs HEMTs, the quantum nature of the channel effectively confines electrons and yields a steep subthreshold behaviour with respect to comparable silicon MOSFETs[18]. The thinner the channel, the closer the subthreshold swing approaches its ideal value of ~60 mV per decade (that is, the current increases by a factor of 10 for every 60-mV increase in gate voltage) at room temperature.

Thinning down the channel is not without drawbacks, however, as scattering tends to increase degrading transport. Measurements of mobility show this. When the thickness of the channel of an InAs HEMT is reduced from 10 nm to 5 nm, the electron mobility degrades from ~13,000 cm^2 V^{-1} s^{-1} to ~10,000 cm^2 V^{-1} s^{-1} (ref. 18). However, the injection velocity of short-gate-length transistors is affected much less[19]. This makes sense because ballistic transport should be expected when transistors are short enough. A thin quantum-well architecture has the potential to scale to very small dimensions.

An important goal of scaling is to maximize I_{ON} while maintaining an acceptable I_{OFF}. When discussing the suitability of different device technologies for logic applications, both values should be considered. A simple way is to refer to the I_{ON} that can be obtained for a set value of I_{OFF} at a certain V_{DD}. This figure can be unambiguously defined in any device with reasonable characteristics even if it does not have the 'correct' threshold voltage, V_T, as is often the case in experimental devices. A standard value for I_{OFF} in high-performance logic devices is 100 nA μm^{-1}. Figure 3 shows the I_{ON} of different devices at this value of I_{OFF} and a V_{DD} of 0.5 V. It includes InAs HEMTs from my own laboratory[20], as well as commercial silicon CMOS transistors scaled to 0.5 V (ref. 12). In addition, projections for future silicon CMOS transistors based on the *International Technology Roadmap for Semiconductors*[7] are also shown. Figure 3 indicates that when appropriately balancing performance and short-channel effects, InAs FETs substantially outperform silicon MOSFETs of similar gate length. The gap is more startling when you consider that the silicon MOSFETs have a source resistance of about 80 Ω μm, compared with 230 Ω μm for the InAs HEMTs. If this shortcoming can be addressed, much better performance can be expected from a future InAs quantum-well FET technology[21].

Underpinning the phenomenal electrical characteristics of III–V FETs is heterostructure growth technology with monoatomic layer precision and an ability to synthesize perfectly specular interfaces. Molecular beam epitaxy (MBE) and, increasingly, metalorganic vapour-phase epitaxy (MOVPE) are at the heart of 'bandgap engineering' in III–V heterostructures. Perhaps the most dramatic testament to these technologies is the electron mobility of 36 million cm^2 V^{-1} s^{-1} obtained at low temperatures in the AlGaAs/GaAs system[22]. This could be the most perfect artificial structure ever made.

The III–V HEMTs have helped make the case for III–V CMOS technology. By themselves, they are not suitable for use in logic because of their high gate leakage current. Nevertheless, HEMTs have provided valuable design features for a future III–V MOSFET, including a junctionless design with a thin, undoped, InAs-rich quantum well that extends under the extrinsic portion of the device, over which is placed raised source and drain regions.

Critical issues

The barriers facing the take-up of a new channel material for CMOS technology are huge. By the time the technology will be ready for deployment, the transistor gate length will need to be shorter than 10 nm. To compound the challenge, a disruptive technology, such as one that incorporates III–V compounds, will need to deliver substantially better performance (at least 30–50% better) than the silicon alternative. It must also promise to deliver more than one future scaled generation. All this must be achieved with cost-effective manufacturing and unprecedented reliability. Before this can happen, several critical problems have to be addressed. These are discussed here.

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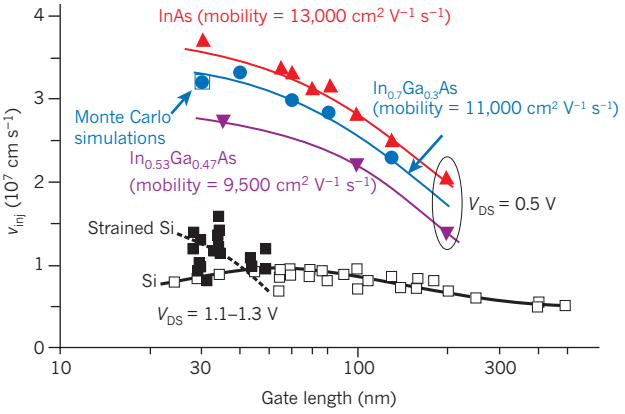

Figure 2 | Electron injection velocity in III–V HEMTs. Electron injection velocity, v_{inj}, is shown for InGaAs and InAs HEMTs with different channel compositions and for silicon MOSFETs as a function of gate length[13,14]. The III–V HEMTs are measured at a drain–source voltage (V_{DS}) of 0.5 V, the silicon MOSFETs at a V_{DS} of 1.1–1.3 V. Despite this discrepancy in voltage, the injection velocity of InGaAs channels is more than twice that of the silicon MOSFETs. The saturation tendency of the injection velocity of InGaAs channels suggests that ballistic (collision-free) transport is occurring; this is confirmed by ballistic Monte Carlo simulations that fall right on the experimental point[15].

The gate stack

At the heart of a MOSFET is the gate stack (Fig. 4). It is composed of a metal gate, a high-permittivity (high-κ) dielectric barrier and the semiconductor channel. It must have a dielectric free of trapped charge and other defects, a smooth interface with few interfacial imperfections, and high stability. One of the miracles of silicon technology is the existence of a native oxide, SiO_2, that meets these requirements. No such native oxides exist for III–V compounds. In fact, exposure of a III–V surface to oxygen results in 'Fermi-level pinning', which is an inability to modulate the electrostatic potential inside the semiconductor[23]. This makes it impossible to use in a MOSFET. In GaAs, the most advanced III–V compound, oxidation creates a rich menu of Ga and As oxides and suboxides, elemental As, As–As dimers and Ga dangling bonds, among other defects[24]. Associated with these is a high density of interface states that prevents the effective modulation of the surface Fermi level[25]. Because of the difficulty of avoiding surface oxidation, early attempts to fabricate GaAs MOSFETs yielded devices with poor performance and low stability[26,27].

In 1995, Ga_2O_3 deposited *in situ* on GaAs was shown to yield an interface that approached the quality of the AlGaAs/GaAs system[28–30]. This led to both n- and p-channel GaAs MOSFETs[31,32] and suggested that dielectric/III–V interfaces with unpinned Fermi levels were indeed possible.

A major step forward was taken in 2003 when a GaAs MOSFET using Al_2O_3 deposited by atomic layer deposition (ALD) was demonstrated[33]. The ALD technique is *ex situ*, robust and highly scalable and is widely used in modern silicon manufacturing, so a high-quality ALD oxide/III–V interface opens the door to manufacturing III–V MOSFETs. This result was unexpected because the starting GaAs surface had been exposed to air. Transmission electron microscopy (TEM) and X-ray photoelectron spectroscopy (XPS) soon showed that during ALD, a kind of 'clean-up effect' takes place in which surface oxides are largely eliminated[34,35]. This happens in the very early stages of ALD[24,36], and subsequent exposure to the ALD oxidant does not regrow the III–V oxides[36]. Using ALD soon led to MOSFET demonstrations on other III–V compounds, such as InGaAs[37], InAs[38] and InP[39].

Progress in the electrical characteristics of III–V MOSFETs accrues from reductions in the interface state density, D_{it}. As their name suggests, interface states are electronic states that arise from disruptions to the ideal bonding structure of a semiconductor at its interface with a dielectric. They affect device operation in several ways. Interface states below the edge of the conduction band increase the subthreshold swing, whereas those inside the conduction band trap electrons. Both effects reduce I_{ON} for a given I_{OFF}. Interface states can also shift the threshold voltage, degrade the channel mobility and be a source of instability.

Insight into the origin of interface states can be gained from density functional theory (DFT) simulations[25,40,41], which allow the construction of detailed bonding models for oxide/III–V interfaces and the computation of the density of states across the band structure. A perfect reconstructed GaAs surface is free of defect states[25]. When the surface is oxidized, interface states appear as a result of As–As bonds, As dangling bonds, Ga vacancies and perhaps Ga–O and As–O bonds[25,40]. Interestingly, GaO-passivated surfaces are seen to be clean of any gap states[42], which is consistent with clear manifestations of unpinned Fermi levels in the Ga_2O_3/GaAs system[43].

According to DFT calculations, several interfacial defects appear when HfO_2 or Al_2O_3, two common ALD high-κ dielectrics, are placed on top of GaAs. Perhaps the most abundant is the As–As dimer, a bonding structure that should not exist in a perfect interface and that is characterized by a near-midgap state[40,41]. In experiments, XPS shows that As–As dimers remain at the interface past the early stages of ALD[24]. A second prominent defect is the Ga dangling bond, which DFT calculations place close to the edge of the conduction band[40,41]. The high density of these defects and their location in the band structure is consistent with experiments and makes the prospect of high-quality GaAs MOSFETs based on ALD oxides problematic[43].

There are several ways to deal with this problem. The first is to engineer the interface through pre-deposition cleaning treatments[44,45], the use of interfacial layers[46,47], the deposition chemistry[48], post-deposition treatments[44,49] or alternative dielectrics[50,51]. The second involves changing the surface crystalline orientation. The most common orientation is (100), but better device results have been reported on the GaAs (111)A surface[52] (this is also the case in InGaAs[53] and InP[54]). This can be explained by DFT as the high-κ/GaAs bonding structure at the interface lacks As–As dimer states[41].

The third approach is to use compounds containing indium. The device characteristics of MOSFETs improve significantly when the InAs mole fraction in the InGaAs channel is increased[55]. InP has also yielded

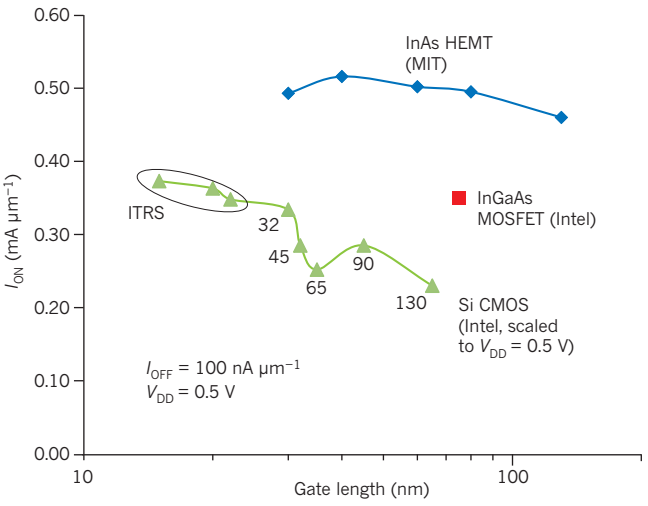

Figure 3 | High 'on' currents in III–V HEMTs. The graph shows how 'on' current, I_{ON}, varies with gate length for InAs HEMTs and silicon MOSFETs at 0.5 V for a fixed 'off' current of 100 nA μm^{-1}. The silicon data correspond to 0.5 V and are obtained from models of published experimental data at higher voltages[12]. The data points labelled ITRS represent projections for future scaling from the *International Technology Roadmap for Semiconductors*[7]. The red square corresponds to an InGaAs MOSFET[59]; the fact that it already exceeds the performance of silicon MOSFETs at 0.5 V is very encouraging. MIT, Massachusetts Institute of Technology. Image modified, with permission from ref. 13.

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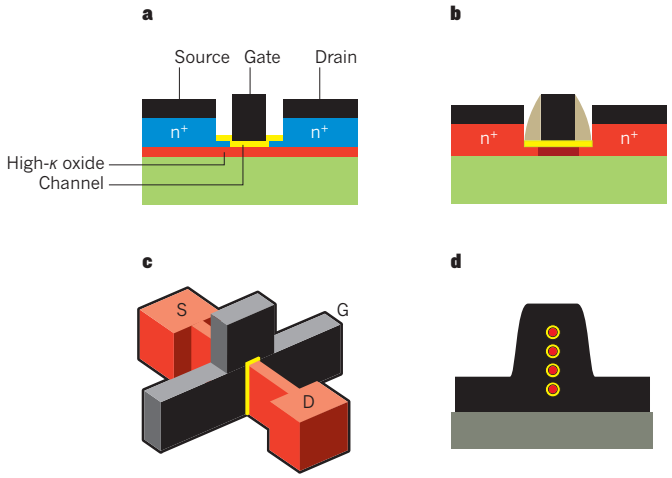

Figure 4 | Possible future MOSFETs using a III–V compound semiconductor channel. **a**, Etched source-and-drain quantum-well MOSFET. **b**, Regrown source-and-drain quantum-well MOSFET. **c**, III–V FinFET, in which the channel charge is electrostatically controlled by a gate that wraps around three sides of a very thin channel. **d**, 'Gate-all-around' nanowire MOSFET, which has an array of very short and thin nanowires with the gate wrapped around them. S, source; G, gate; D, drain.

good results[39]. According to DFT, in these materials the interface states associated with group-V dimers and group-III dangling bonds are predicted to lie well inside the conduction band[41].

A separate consideration in high-κ/III–V MOS structures is the channel mobility. The ideal gate stack from a scaling point of view is a surface-channel device in which the oxide sits directly on top of the channel. The problem is that interface roughness and Coulomb scattering associated with interface states, as well as remote phonon scattering from the high-κ oxide, severely degrade the mobility[56,57]. For InGaAs MOS structures with scaled gate stacks at realistic sheet carrier concentrations, a mobility in excess of 1,000 $cm^2 V^{-1} s^{-1}$ is difficult to obtain[57].

A possible solution to this problem is a buried-channel device. In this approach, a thin wide-bandgap semiconductor is placed between the channel and the oxide. This mitigates the impact of interface roughness and reduces Coulomb scattering from the charged interface and bulk oxide states, as well as remote phonon scattering from oxide phonons. All this yields a higher mobility. However, this approach only goes so far, as the need to manage short-channel effects forces the oxide/semiconductor composite barrier structure to remain very thin. At the moment, this limits electron mobility in InGaAs channels to the 1,000–3,000 $cm^2 V^{-1} s^{-1}$ range[58]. The effect of this level of mobility degradation on the injection velocity in very short devices is not known.

So far, the best III–V MOSFETs have been obtained on InGaAs buried-channel structures equipped with an InP barrier layer using ALD TiSiO as the dielectric[59]. A device with a gate length of 75 nm displays an impressive combination of current drive and subthreshold characteristics, as shown in Fig. 3. This is the only III–V MOSFET I know of with characteristics that entitle it to appear in this figure. Remarkably, its performance exceeds that of state-of-the-art silicon MOSFETs.

Self-aligned transistor design

Using group III–V compounds in CMOS technology only makes sense if they allow further transistor scaling and provide better performance than any of the alternatives. The challenge in making small transistors is twofold. First, it is important to maintain adequate electrostatic integrity. This means that the gate exerts a greater degree of electrostatic control over the electron concentration in the channel than in the drain, which calls for a high geometric aspect ratio for the channel. The second challenge is maintaining low parasitic capacitance and resistance from one part of the structure to another.

Parasitic capacitance is unlikely to be very different in scaled III–V and silicon MOSFETs. Group III–V compounds have slightly higher permittivity than silicon (about 10% higher for GaAs), but this should have only a minor role because parasitic fringe capacitance associated with the gate sidewalls is quickly becoming dominant as devices continue to scale down in size[60].

Parasitic resistance is a significant concern. Future generations of transistors will require a source resistance below 50 Ω μm. State-of-the-art InGaAs HEMTs have a source resistance of about 150–250 Ω μm. The gap is larger than it seems because InGaAs HEMTs feature relatively large contacts (of the order of micrometres). Modelling has shown that when the contact dimensions are appropriately scaled, the contact resistance is more than two orders of magnitude higher than the required value[61]. How is this problem to be solved?

There are several ingredients to the solution. First, the device structure needs to be self-aligned. This means that the contacts are placed without requiring an optical alignment to the gate, as commonly done in HEMTs. Self-alignment allows a gate–contact distance of only a few nanometres. Self-aligned III–V HEMTs have been demonstrated with promising results[61,62].

A very low ohmic contact resistance is also required. Fundamentally, InGaAs should not be at a disadvantage compared with silicon. Doping levels of silicon (the preferred n-type dopant) in InGaAs easily reach the mid-10^{19} cm^{-3} range with an electron mobility that exceeds 1,000 $cm^2 V^{-1} s^{-1}$ at room temperature[63]. This yields a resistivity that beats that of As-doped silicon with doping levels in the mid-10^{20} cm^{-3} range with one-tenth of the mobility. Refractory ohmic contacts to n^+-InGaAs with contact resistivities of around 1–2 Ω $μm^2$ have been demonstrated using different metals[63]. These values are comparable to the best contacts to n^+-Si and are in the range required for fully scaled devices.

The biggest concern about scaled III–V transistors is attaining adequate electrostatic integrity. This refers to the tight control of the channel charge by the gate, a key requirement for sharp subthreshold swing. In a planar quantum-well design, this demands a very thin channel and an extremely thin gate barrier.

Two possible planar quantum-well designs are shown in Fig. 4. Figure 4a shows a device architecture with source and drain regions grown with the original heterostructure and recessed to accommodate a self-aligned gate. In this design, the quantum well extends underneath the source and drain, and high-mobility transport is preserved in the extrinsic device. A second advantage is that the dielectric/III–V interface is formed relatively late in the process, providing substantial process flexibility. The InGaAs MOSFET illustrated in Fig. 3 has a structure like this[59].

A second possible device design is shown in Fig. 4b. In this architecture, the gate stack is formed early in the process. Using the gate as a mask, the channel is etched away from the extrinsic portion of the heterostructure, and then the source and drain regions are grown epitaxially in a self-aligned way. A potential advantage of this approach is the ability to introduce uniaxial strain in the channel. Prototype devices have been fabricated exhibiting promising electrical characteristics[64,65].

Should the planar design fail to meet the requirements, alternative device structures exist. Recently, Intel announced the use of a trigate FET[66] for the 22-nm CMOS generation. The trigate, also known as a FinFET, is in essence a MOSFET in which the channel charge is electrostatically controlled by a gate that wraps around three sides of a very thin channel. This approach yields improved electrostatic control and scalability. Similar devices based on III–V compounds (Fig. 4c) have already been demonstrated with improved short-channel effects over planar designs[67,68]. An important concern is dry-etching damage, which is difficult to anneal in compound semiconductors[69].

Higher electrostatic integrity and scaling potential are expected from nanowire FETs (Fig. 4d). These consist of an array of very short and thin nanowires with the gate wrapped around them. Silicon nanowire

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FETs have been studied for some time[70,71] and constitute an alternative CMOS technology in their own right. For III–V compounds, horizontal and vertical nanowire FETs with impressive characteristics have been demonstrated in the InAs system[72,73].

The p-type MOSFET

Both NMOS and PMOS transistors with reasonably matched performance are required for CMOS logic circuits. The PMOS transistors are based on holes and tend to be inferior to NMOS transistors because of their generally lower mobility. Circuit designers have learned to work with a silicon PMOS transistor that has about one-third of the current density of the NMOS transistor. A future III–V CMOS technology should strive for a performance gap that is no worse than this.

Although hole mobility offers limited guidance in the selection of a suitable p-type channel material, the large imbalance between electron and hole mobilities in III–V compounds is a serious problem, as Fig. 1 shows. It depicts the highest electron and hole mobilities at room temperature that have been reported in inversion layers or quantum wells in various semiconductors as a function of the heterostructure lattice constant (the actual lattice constant, as opposed to the relaxed lattice constant). These mobilities typically come from buried-channel heterostructures (such as HEMTs) at relatively low carrier concentrations.

In Fig. 1, not one semiconductor features both an electron mobility above 5,000 $cm^2 V^{-1} s^{-1}$ and a hole mobility above 1,500 $cm^2 V^{-1} s^{-1}$. In most cases the hole mobility is significantly lower than this. There is not even a pair of materials with a similar lattice constant that exhibit mobilities in those ranges. Perhaps the closest is GaAs for the NMOS transistor and Ge for the PMOS transistor, but I have already discussed the difficulty in obtaining high-quality high-κ/GaAs interfaces by ALD.

It seems inevitable then to conclude that a future III–V CMOS technology will feature NMOS and PMOS transistors made of different materials with different lattice constants. This has important implications for their co-integration on a common substrate, as discussed below.

The hole mobility can be increased by introducing compressive biaxial strain. This can be accomplished through pseudomorphic growth on a material with a smaller lattice constant. Figure 1 illustrates this through the arrows, which indicate increasing compressive biaxial strain. The gains can be substantial. A hole mobility approaching 2,000 $cm^2 V^{-1} s^{-1}$ has been reported in compressively strained Ge[74], with around 1,500 $cm^2 V^{-1} s^{-1}$ in InGaSb[75], more than 1,300 $cm^2 V^{-1} s^{-1}$ in GaSb[76], and over 1,200 $cm^2 V^{-1} s^{-1}$ in InSb[77]. These are now the most promising materials for PMOS transistors.

There are other ways of improving hole mobility. In Si and Ge, uniaxial compressive strain also increases the hole mobility[78]. Through uniaxial strain, silicon PMOS transistors have recently narrowed the performance gap with n-type MOSFETs[60]. Uniaxial strain also represents a promising approach for III–V compounds[79–81]. An interesting recent finding is that the superposition of uniaxial strain and biaxial strain yields nonlinear mobility gains[80,82].

There have already been demonstrations of PMOS transistors in GaAs[32], InGaAs[83], GaSb[84] and InGaSb[84]. Most of the issues discussed above for NMOS transistors also apply to PMOS transistors, but their development lags behind. At the moment, it does not seem that any III–V PMOS transistor will have a performance advantage over a Ge device, a technology that is much more mature[85]. For this reason, at the present time, the leading PMOS contender for a III–V CMOS technology is based on Ge.

Co-integration of NMOS and PMOS transistors on silicon

Perhaps progress is most needed in the side-by-side integration of III–V NMOS and PMOS transistors on a silicon substrate. Economics dictates the use of silicon wafers for at least two reasons. First, a large wafer is essential to achieving the cost structure central to Moore's law. An additional consideration is the effective use of the tool base that will be in place when the new technology moves into advanced development.

The fabrication of III–V heterostructures on silicon has been under investigation for some time. The interest was fuelled by the integration of optical devices and CMOS logic circuits, multijunction solar cells, and the heterogeneous integration of CMOS circuitry and III–V electronic devices, among other applications. Nanometre-scale III–V CMOS transistors pose some unique requirements for heterogeneous integration. One is the need for a very thin buffer structure that converts the silicon lattice constant into the desired one. The thickness of the buffer layer matters for economic reasons, because long growth times limit process throughput, and for thermal reasons, because heat produced in the transistors must be effectively dissipated. Most buffer layers are made of ternary compound semiconductors, such as InAlAs or AlGaAs, which have poor thermal conductivity[86].

InGaAs MOSFETs with the lattice constant of InP have been fabricated on silicon by MBE using a 1.5-μm-thick composite GaAs/graded-InAlAs buffer layer[59]. Thinner buffers have been demonstrated for InGaAs HEMTs on silicon[87]. MOVPE, a more practical technique for manufacturing, is also being used. Excellent results have been obtained using an InP/InAlAs composite buffer around 1 μm thick[88].

A separate approach to the integration of III–V compounds on silicon is the transfer of a III–V device layer onto a silicon substrate that is covered by a thin dielectric[89,90]. This is similar to silicon-on-insulator (SOI), a well-established substrate in the silicon industry. The III–V-on-insulator approach even allows strain engineering of the transferred device layer[91]. The challenge for all transfer layer techniques is scaling up to large wafers.

Another silicon 'hetero-integration' technique is aspect ratio trapping (ART)[92]. This consists of the selective growth of lattice-mismatched material inside trenches with high aspect ratio and submicrometre dimensions. The trenches trap threading dislocations, yielding high-quality device layers. Ge, GaAs and InP films have been grown using ART. When combined with epitaxial lateral overgrowth (ELO), uniform high-quality films can be achieved[92]. GaAs MOSFETs with electrical characteristics comparable to those fabricated on GaAs substrates have been demonstrated using ART–ELO[93].

Although detailed studies of defect control have yet to be reported, it currently seems feasible to fabricate high-quality III–V-layer structures on silicon in a reasonably scalable manner. The greatest challenge is the preparation of a hybrid substrate for NMOS and PMOS transistors that incorporates islands of two different materials with different lattice constants, placed side by side with minimum overhead and yielding a planar surface. This is a critical problem that does not seem to be receiving sufficient attention.

Afterword

Moore's law is not a physical law in the manner of Gauss's law or Newton's laws of motion. It does not describe nature. Moore's law was formulated from observations of the exponential increase in transistor density in the early days of integrated electronics[94], but it has remained valid for 50 years. Moore's true insight was the understanding of the economics behind microelectronics[95]. The driver is not shrinking transistor size per se, but diminishing transistor cost. Transistor footprint scaling makes this possible, but only up to the point at which increased complexity starts eroding manufacturing yields. Moore's law is all about economics and human innovation, and silicon integrated electronics is a dramatic manifestation of the human spirit. But there is nothing unique about silicon. In the not too distant future it may no longer make economic sense to shrink silicon transistors further. It is then that III–V compounds could become the key for continuing Moore's law. Here I have reviewed some of the most pressing technical challenges that need to be overcome to make this happen and discussed some of the remarkable progress already made. ■

1. Ferain, I., Colinge, C. A. & Colinge, J.-P. Multigate transistors as the future of classical metal–oxide–semiconductor field-effect transistors. *Nature* **479,** 310–316 (2011).
2. Chau, R., Doyle, B., Datta, S., Kavalieros, J. & Zhang, K. Integrated nanoelectronics for the future. *Nature Mater.* **6,** 810–812 (2007).
3. Iwai, H. Roadmap for 22 nm and beyond. *Microelectron. Eng.* **86,** 1520–1528 (2009).

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4. Frank, D. J. Power-constrained CMOS scaling limits. *IBM J. Res. Dev.* **46,** 235–244 (2002).
5. Theis, T. N. & Solomon, P. M. In quest of the "next switch": prospects for greatly reduced power dissipation in a successor to the silicon field-effect transistor. *Proc. IEEE* **98,** 2005–2014 (2010).
6. del Alamo, J. A. The high-electron mobility transistor at 30: impressive accomplishments and exciting prospects. *Int. Conf. Compound Semicond. Manuf. Technol.* 17–22 (CS ManTech, 2011).
7. ITRS, International Technology Working Groups *International Technology Roadmap for Semiconductors* ⟨http://www.itrs.net/Links/2010ITRS/Home2010.htm⟩ (ITRS, 2010).
8. Kim, D.-H. *et al.* 50-nm E-mode $In_{0.7}Ga_{0.3}As$ PHEMTs on 100-mm InP substrate with $f_{max} > 1$ THz. *IEEE Int. Electron Devices Meet.* 692–695 (IEEE, 2010).
9. Kim, D.-H. & del Alamo, J. A. 30-nm InAs PHEMTs With $f_T = 644$ GHz and $f_{max} = 681$ GHz. *IEEE Electron Device Lett.* **31,** 806–808 (2010).
10. Leuther, A. *et al.* 20 nm Metamorphic HEMT with 660 GHz f_T. *Int. Conf. Indium Phosphide Relat. Mater.* (IEEE, 2011).
11. Jeong, C., Antoniadis, D. A. & Lundstrom, M. S. On backscattering and mobility in nanoscale silicon MOSFETs. *IEEE Trans. Electron Devices* **56,** 2762–2769 (2009).
12. del Alamo, J. A., Kim, D.-H., Kim, T.-W., Jin, D. & Antoniadis, D. A. III–V CMOS: what have we learned from HEMTs? *Int. Conf. Indium Phosphide Relat. Mater.* (IEEE, 2011).
13. Kim, D. H., del Alamo, J. A., Antoniadis, D. A. & Brar, B. Extraction of virtual-source injection velocity in sub-100 nm III–V HFETs. *IEEE Int. Electron Devices Meet.* 861–864 (IEEE, 2009).
This paper reports that the electron injection velocity in InGaAs and InAs HEMTs is more than double that in Si MOSFETs of similar gate length at half the voltage.
14. Khakifirooz, A. & Antoniadis, D. A. MOSFET performance scaling — part I: historical trends. *IEEE Trans. Electron Devices* **55,** 1391–1400 (2008).
15. Liu, Y. *et al.* in *Fundamentals of III–V Semiconductor MOSFETs* (eds Oktyabrsky, S. & Ye, P. D.) 31–50 (Springer, 2010).
16. Fischetti, M. V. & Laux, S. E. Are GaAs MOSFETs worth building? A model-based comparison of Si and GaAs n-MOSFETs. *IEEE Int. Electron Devices Meet.* 481–484 (IEEE, 1989).
17. Jin, D., Kim, D.-H., Kim, T. & del Alamo, J. A. Quantum capacitance in scaled down III–V FETs. *IEEE Int. Electron Devices Meet.* 495–498 (IEEE, 2009).
18. Kim, T.-W., Kim, D.-H. & del Alamo, J. A. Logic characteristics of 40 nm thin-channel InAs HEMTs. *Int. Conf. Indium Phosphide Relat. Mater.* 496–499 (IEEE, 2010).
19. Kim, T.-W. & del Alamo, J. A. Injection velocity in thin-channel InAs HEMTs. *Int. Conf. Indium Phosphide Relat. Mater.* (IEEE, 2011).
20. Kim, D.-H. & del Alamo, J. A. 30 nm E-mode InAs PHEMTs for THz and future logic applications. *IEEE Int. Electron Devices Meet.* 719–722 (IEEE, 2008).
21. Dewey, G. *et al.* Logic performance evaluation and transport physics of Schottky-gate III–V compound semiconductor quantum well field effect transistors for power supply voltages (V_{CC}) ranging from 0.5 V to 1.0 V. *IEEE Int. Electron Devices Meet.* 487–490 (IEEE, 2009).
22. Umansky, V. *et al.* MBE growth of ultra-low disorder 2DEG with mobility exceeding $35 \times 10^6 cm^2/Vs$. *J. Cryst. Growth* **311,** 1658–1661 (2009).
23. Spicer, W. E., Lindau, I., Skeath, P. & Su, C. Y. Unified defect model and beyond. *J. Vac. Sci. Technol.* **17,** 1019–1027 (1980).
24. Hinkle, C. L. *et al.* GaAs interfacial self-cleaning by atomic layer deposition. *Appl. Phys. Lett.* **92,** 071901 (2008).
25. Scarrozza, M. *et al.* A theoretical study of the initial oxidation of the GaAs(001)-β2(2×4) surface. *Appl. Phys. Lett.* **95,** 253504 (2009).
26. Becke, H., Hall, R. & White, J. Gallium arsenide MOS transistors. *Solid State Electron.* **8,** 813–818 (1965).
27. Mimura, T., Odani, K., Yokoyama, N., Nakayama, Y. & Fukuta, M. GaAs microwave MOSFETs. *IEEE Trans. Electron Devices* **25,** 573–579 (1978).
28. Passlack, M. *et al. In-situ* Ga_2O_3 process for GaAs inversion/accumulation device and surface passivation applications. *IEEE Int. Electron Devices Meet.* 383–386 (IEEE, 1995).
29. Passlack, M., Hong, M. & Mannaerts, J. P. Quasistatic and high frequency capacitance–voltage characterization of Ga_2O_3–GaAs structures fabricated by *in situ* molecular beam epitaxy. *Appl. Phys. Lett.* **68,** 1099–1101 (1996).
30. Passlack, M., Hong, M., Mannaerts, J. P., Kwo, J. R. & Tu, L. W. Recombination velocity at oxide–GaAs interfaces fabricated by *in situ* molecular beam epitaxy. *Appl. Phys. Lett.* **68,** 3605–3607 (IEEE, 1996).
31. Ren, F. *et al.* Enhancement-mode p-channel GaAs MOSFETs on semi-insulating substrates. *IEEE Int. Electron Devices Meet.* 943–945 (IEEE, 1996).
32. Ren, F. *et al.* Demonstration of enhancement-mode p- and n-channel GaAs MOSFETS with $Ga_2O_3(Gd_2O_3)$ As gate oxide. *Solid State Electron.* **41,** 1751–1753 (1997).
33. Ye, P. D. *et al.* GaAs MOSFET with oxide gate dielectric grown by atomic layer deposition. *IEEE Electron Device Lett.* **24,** 209–211 (2003).
34. Frank, M. M. *et al.* HfO_2 and Al_2O_3 gate dielectrics on GaAs grown by atomic layer deposition. *Appl. Phys. Lett.* **86,** 152904 (2005).
35. Huang, M. L. *et al.* Surface passivation of III–V compound semiconductors using atomic-layer-deposition-grown Al_2O_3. *Appl. Phys. Lett.* **87,** 252104 (2005).
36. Milojevic, M. *et al.* Half-cycle atomic layer deposition reaction studies of Al_2O_3 on $(NH_4)_2S$ passivated GaAs(100) surfaces. *Appl. Phys. Lett.* **93,** 252905 (2008).
37. Xuan, Y., Lin, H. C., Ye, P. D. & Wilk, G. D. Capacitance–voltage studies on enhancement-mode InGaAs metal-oxide-semiconductor field-effect transistor using atomic-layer-deposited Al_2O_3 gate dielectric. *Appl. Phys. Lett.* **88,** 263518 (2006).
38. Li, N. *et al.* Properties of InAs metal-oxide-semiconductor structures with atomic-layer-deposited Al_2O_3 dielectric. *Appl. Phys. Lett.* **92,** 143507 (2008).
39. Wu, Y. Q., Xuan, Y., Ye, P. D., Cheng, Z. & Lochtefeld, A. Inversion-type enhancement-mode InP MOSFETs with ALD Al_2O_3, HfO_2 and HfAlO nanolaminates as high-κ gate dielectrics. *IEEE Device Res. Conf.* 117–118 (IEEE, 2007).
40. Wang, W., Xiong, K., Wallace, R. M. & Cho, K. Impact of interfacial oxygen content on bonding, stability, band offsets, and interface states of GaAs:HfO_2 interfaces. *J. Phys. Chem. C* **114,** 22610–22618 (2010).
41. Lin, L. & Robertson, J. Defect states at III–V semiconductor oxide interfaces. *Appl. Phys. Lett.* **98,** 082903 (2011).
This paper provides density-functional theory calculations of interface defect states between high-κ oxides and GaAs, InAs and InP that are consistent with experimental observation.
42. Wang, W., Lee, G., Huang, M., Wallace, R. M. & Cho, K. First-principles study of GaAs(001)-β2(2×4) surface oxidation and passivation with H, Cl, S, F, and GaO. *J. Appl. Phys.* **107,** 103720 (2010).
43. Passlack, M., Droopad, R. & Brammertz, G. Suitability study of oxide/gallium arsenide interfaces for MOSFET applications. *IEEE Trans. Electron Devices* **57,** 2944–2956 (2010).
This experimental study of oxide–GaAs interfaces for MOSFET applications finds that whereas *in situ*-deposited Ga_2O_3 leads to excellent interfacial quality, *ex situ* ALD-deposited Al_2O_3 on GaAs leads to Fermi-level pinning.
44. Trinh, H. D. *et al.* The influences of surface treatment and gas annealing conditions on the inversion behaviors of the atomic-layer-deposition Al_2O_3/n-$In_{0.53}Ga_{0.47}As$ metal-oxide-semiconductor capacitor. *Appl. Phys. Lett.* **97,** 042903 (2010).
45. O'Connor, E. *et al.* A systematic study of $(NH_4)_2S$ passivation (22%, 10%, 5%, or 1%) on the interface properties of the $Al_2O_3/In_{0.53}Ga_{0.47}As$/InP system for n-type and p-type $In_{0.53}Ga_{0.47}As$ epitaxial layers. *J. Appl. Phys.* **109,** 024101 (2011).
46. Ok, I. & Lee, J. C. in *Fundamentals of III–V Semiconductor MOSFETs* (eds Oktyabrsky, S. & Ye, P. D.) 307–348 (Springer, 2010).
47. Wu, Y. D. *et al.* Engineering of threshold voltages in molecular beam epitaxy-grown $Al_2O_3/Ga_2O_3(Gd_2O_3)/In_{0.2}Ga_{0.8}As$. *J. Vac. Sci. Technol. B* **28,** C3H10–C3H13 (2010).
48. Cheng, C.-W., Apostolopoulos, G. & Fitzgerald, E. A. The effect of interface processing on the distribution of interfacial defect states and the C–V characteristics of III–V metal-oxide-semiconductor field effect transistors. *J. Appl. Phys.* **109,** 023714 (2011).
49. Chen, Y.-T. *et al.* Fluorinated HfO_2 gate dielectric engineering on $In_{0.53}Ga_{0.47}As$ metal-oxide-semiconductor field-effect-transistors. *Appl. Phys. Lett.* **96,** 103506 (2010).
50. Engel-Herbert, R., Hwang, Y., Cagnon, J. I. & Stemmer, S. Metal-oxide-semiconductor capacitors with ZrO_2 dielectrics grown on $In_{0.53}Ga_{0.47}As$ by chemical beam deposition. *Appl. Phys. Lett.* **95,** 062908 (2009).
51. Liu, Y., Xu, M., Heo, J., Ye, P. D. & Gordon, R. G. Heteroepitaxy of single-crystal $LaLuO_3$ on GaAs(111)A by atomic layer deposition. *Appl. Phys. Lett.* **97,** 162910 (2010).
52. Xu, M. *et al.* New insight into Fermi-level unpinning on GaAs: impact of different surface orientations. *IEEE Int. Electron Devices Meet.* 865–868 (IEEE, 2009).
53. Ishii, H. *et al.* High electron mobility metal–insulator–semiconductor field-effect transistors fabricated on (111)-oriented InGaAs channels. *Appl. Phys. Express* **2,** 121101 (2009).
54. Wang, C., Xu, M., Colby, R., Stach, E. A. & Ye, P. D. "Zero" drain-current drift of inversion-mode NMOSFET on InP (111)A surface. *IEEE Device Res. Conf.* 93–94 (IEEE, 2011).
55. Ye, P. D., Xuan, Y., Wu, Y. Q. & Xu, M. Inversion-mode $In_xGa_{1-x}As$ MOSFETs ($x = 0.53, 0.65, 0.75$) with atomic-layer-deposited high-κ dielectrics. *ECS Trans.* **19,** 605–614 (2009).
This paper reports significant improvements in ALD oxide InGaAs MOSFET transistor characteristics as the InAs mole fraction in the channel is increased.
56. Sonnet, A. M. *et al.* On the calculation of effective electric field in $In_{0.53}Ga_{0.47}As$ surface channel metal-oxide-semiconductor field-effect-transistors. *Appl. Phys. Lett.* **98,** 193501 (2011).
57. Sonnet, A. M. *et al.* Remote phonon and surface roughness limited universal electron mobility of $In_{0.53}Ga_{0.47}As$ surface channel MOSFETs. *Microelectron. Eng.* **88,** 1083–1086 (2011).
58. Oktyabrsky, S. *et al.* Electron scattering in buried InGaAs/high-κ MOS channels. *ECS Trans.* **35,** 385–395 (2011).
59. Radosavljevic, M. *et al.* Advanced high-κ gate dielectric for high-performance short-channel $In_{0.7}Ga_{0.3}As$ quantum well field effect transistors on silicon substrate for low power logic applications. *IEEE Int. Electron Devices Meet.* 319–322 (IEEE, 2009).
This paper reports the best logic performance of a III–V MOSFET so far, exceeding that of state-of-the-art silicon MOSFETs at 0.5 V.
60. Kuhn, K. J., Liu, M. Y. & Kennel, H. Technology options for 22 nm and beyond. *Int. Workshop Junct. Technol.* 1–6 (IEEE, 2010).
61. Waldron, N., Kim, D.-H. & del Alamo, J. A. A self-aligned InGaAs HEMT architecture for logic applications. *IEEE Trans. Electron Devices* **57,** 297–304 (2010).
62. Kim, T.-W., Kim, D.-H. & del Alamo, J. A. 60 nm Self-aligned-gate InGaAs HEMTs with record high-frequency characteristics. *IEEE Int. Electron Devices Meet.* 696–699 (IEEE, 2010).
63. Singisetti, U. *et al.* Ultralow resistance *in situ* ohmic contacts to InGaAs/InP. *Appl. Phys. Lett.* **93,** 183502 (2008).

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This paper reports Mo/n+–InGaAs ohmic contacts with contact resistance comparable to state-of-the-art silicon technology.
64. Chin, H.-C., Gong, X., Liu, X. & Yeo, Y. Lattice-mismatched $In_{0.4}Ga_{0.6}As$ source/drain stressors with *in situ* doping for strained $In_{0.53}Ga_{0.47}As$ channel n-MOSFETs. *IEEE Electron Device Lett.* **30,** 805–807 (2009).
65. Terao, R. *et al.* InP/InGaAs composite metal–oxide–semiconductor field-effect transistors with regrown source and Al_2O_3 gate dielectric exhibiting maximum drain current exceeding 1.3 mA/μm. *Appl. Phys. Express* **4,** 054201 (2011).
This paper reports that a 100-nm gate length InGaAs MOSFET with raised epitaxially grown source and drain regions has excellent electrical characteristics.
66. Doyle, B. S. *et al.* High performance fully-depleted tri-gate CMOS transistors. *IEEE Electron Device Lett.* **24,** 263–265 (2003).
67. Wu, Y. Q., Xu, M., Wang, R. S., Koybasi, O. & Ye, P. D. High performance deep-submicron inversion-mode InGaAs MOSFETs with maximum G_m exceeding 1.1 mS/μm: new HBr pretreatment and channel engineering. *IEEE Int. Electron Devices Meet.* 323–326 (IEEE, 2009).
68. Radosavljevic, M. *et al.* Non-planar, multi-gate InGaAs quantum well field effect transistors with high-κ gate dielectric and ultra-scaled gate-to-drain/gate-to-source separation for low power logic applications. *IEEE Int. Electron Devices Meet.* 126–129 (IEEE, 2010).
69. Pearton, S. J. & Norton, D. P. Dry etching of electronic oxides, polymers, and semiconductors. *Plasma Process. Polym.* **2,** 16–37 (2005).
70. Hashemi, P., Gomez, L., Canonico, M. & Hoyt, J. L. Electron transport in gate-all-around uniaxial tensile strained-Si nanowire n-MOSFETs. *IEEE Int. Electron Devices Meet.* 1–14 (IEEE, 2008).
71. Suk, S. D. *et al.* High performance 5nm radius twin silicon nanowire MOSFET (TSNWFET): fabrication on bulk Si wafer, characteristics, and reliability. *IEEE Int. Electron Devices Meet.* 717–720 (IEEE, 2005).
72. Do, Q. T., Blekker, K., Regolin, I., Prost, W. & Tegude, F. J. Single n-InAs nanowire MIS-field-effect transistor: experimental and simulation results. *IEEE Int. Indium Phosphide Relat. Mater.* 392–395 (IEEE, 2007).
73. Egard, M. *et al.* Vertical InAs nanowire wrap gate transistors with $f_t > 7$ GHz and $f_{max} > 20$ GHz. *Nano Lett.* **10,** 809–812 (2010).
74. Hock, G., Hackbarth, T., Erben, U., Kohn, E. & Konig, U. High performance 0.25 μm p-type Ge/SiGe MODFETs. *Electron. Lett.* **34,** 1888–1889 (1998).
75. Bennett, B. R., Ancona, M. G., Boos, J. B. & Shanabrook, B. V. Mobility enhancement in strained p-InGaSb quantum wells. *Appl. Phys. Lett.* **91,** 042104 (2007).
76. Bennett, B., Ancona, M., Boos, J., Canedy, C. & Khan, S. Strained GaSb/AlAsSb quantum wells for p-channel field-effect transistors. *J. Cryst. Growth* **311,** 47–53 (2008).
77. Radosavljevic, M. *et al.* High-performance 40 nm gate length InSb p-channel compressively strained quantum well field effect transistors for low-power (V_{CC} = 0.5 V) logic applications. *IEEE Int. Electron Devices Meet.* 1–4 (IEEE, 2008).
78. Kuhn, K. J., Murthy, A., Kotlyar, R. & Kuhn, M. Past, present and future: SiGe and CMOS transistor scaling. *ECS Trans.* **33,** 3–17 (2010).
79. Xia, L., Boos, J. B., Bennett, B. R., Ancona, M. G. & del Alamo, J. A. Hole mobility enhancement in $In_{0.41}Ga_{0.59}Sb$ quantum-well field-effect transistors. *Appl. Phys. Lett.* **98,** 053505 (2011).
80. Xia, L. V. T., Oktyabrsky, S. & del Alamo, J. A. Mobility enhancement of two-dimensional hole Gas in an $In_{0.24}Ga_{0.76}As$ quantum well by <110> uniaxial strain. *Int. Symp. Compound Semicond. 2011* (IEEE, in the press).
81. Nainani, A. *et al.* Engineering of strained III–V heterostructures for high hole mobility. *IEEE Int. Electron Devices Meet.* 857–860 (IEEE, 2009).
82. Gomez, L., Chleirigh, C. N., Hashemi, P. & Hoyt, J. L. Enhanced hole mobility in high Ge content asymmetrically strained-SiGe p-MOSFETs. *IEEE Electron Device Lett.* **31,** 782–784 (2010).
83. Passlack, M. *et al.* Self-aligned GaAs p-channel enhancement mode MOS heterostructure field-effect transistor. *IEEE Electron Device Lett.* **23,** 508–510 (2002).
84. Nainani, A. *et al.* Development of high-κ dielectric for antimonides and a sub 350 °C III–V pMOSFET outperforming germanium. *IEEE Int. Electron Devices Meet.* 138–141 (IEEE, 2010).
This paper describes p-type InGaSb MOSFETs with an ALD Al_2O_3 gate dielectric and excellent characteristics.
85. Pillarisetty, R. *et al.* High mobility strained germanium quantum well field effect transistor as the p-channel device option for low power (V_{cc} = 0.5 V) III–V CMOS architecture. *IEEE Int. Electron Devices Meet.* 150–153 (IEEE, 2010).
86. Nakwaski, W. Thermal conductivity of binary, ternary, and quaternary III–V compounds. *J. Appl. Phys.* **64,** 159–166 (1988).
87. Hudait, M. K. *et al.* Heterogeneous integration of enhancement mode $In_{0.7}Ga_{0.3}As$ quantum well transistor on silicon substrate using thin (≤ 2 μm) composite buffer architecture for high-speed and low-voltage (0.5 V) logic applications. *IEEE Int. Electron Devices Meet.* 625–628 (2007).
88. Tang, C. W., Li, H., Zhong, Z., Ng, K. L. & Lau, K. M. Hetero-epitaxy of III–V compounds lattice-matched to InP by MOCVD for device applications. *IEEE Int. Conf. Indium Phosphide Relat. Mater.* 136–139 (IEEE, 2009).
89. Yokoyama, M. *et al.* Extremely-thin-body InGaAs-on-insulator MOSFETs on Si fabricated by direct wafer bonding. *IEEE Int. Electron Devices Meet.* 46–49 (2010).
90. Ko, H. *et al.* Ultrathin compound semiconductor on insulator layers for high-performance nanoscale transistors. *Nature* **468,** 286–289 (2010).
This paper reports on thin-channel InAs-on-insulator MOSFETs with excellent electrical characteristics fabricated on a silicon substrate by a layer-transfer process.
91. Fang, H. *et al.* Strain engineering of epitaxially transferred, ultrathin layers of III–V semiconductor on insulator. *Appl. Phys. Lett.* **98,** 012111 (2011).
92. Fiorenza, J. *et al.* Aspect ratio trapping: a unique technology for integrating Ge and III–Vs with silicon CMOS. *ECS Trans.* **33,** 963–976 (2010).
93. Wu, Y. Q. *et al.* Atomic-layer-deposited Al_2O_3/GaAs metal-oxide-semiconductor field-effect transistor on Si substrate using aspect ratio trapping technique. *Appl. Phys. Lett.* **93,** 242106 (2008).
94. Moore, G. E. Cramming more components onto integrated circuits. *Electronics* **38,** 114–117 (1965).
95. Hutcheson, G. D. in *Into the Nano Era: Moore's Law Beyond Planar Silicon CMOS* (ed. Huff, H.) 11–38 (Springer, 2009).

Acknowledgements I have enjoyed stimulating discussions with students, collaborators and colleagues. I am particularly thankful to D. Antoniadis, R. Chau, S. Datta, J. Hoyt, D. Jin, D.-H. Kim, T.-W. Kim, A. Kummel, J. Lin, M. Lundstrom, S. Oktyabrsky, M. Passlack, M. Radosavljevic, E. Vogel, N. Waldron, R. Wallace, L. Xia and P. Ye. Research on III–V CMOS transistors at my lab at MIT has been funded by the Materials, Structures and Devices FCRP Center and Intel Corporation.

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