Multiscale Metrology and Optimization of Ultra-Scaled InAs Quantum Well FETs

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***Abstract*—A simulation methodology for ultra-scaled InAs quantum well field-effect transistors (QWFETs) is presented and used to provide design guidelines and a path to improve device performance. A multiscale modeling approach is adopted, where strain is computed in an atomistic valence-force-field method, an atomistic $sp^3d^5s^*$ tight-binding model is used to compute channel effective masses, and a 2-D real-space effective mass-based ballistic quantum transport model is employed to simulate three-terminal current-voltage characteristics including gate leakage. The simulation methodology is first benchmarked against experimental I–V data obtained from devices with gate lengths ranging from 30 to 50 nm. A good quantitative match is obtained. The calibrated simulation methodology is subsequently applied to optimize the design of a 20 nm gate length device. Two critical parameters have been identified to control the gate leakage current of the QWFETs, i) the geometry of the gate contact (curved or square) and ii) the Schottky barrier height at the gate metal contact. In addition to pushing the threshold voltage toward an enhancement mode operation, a higher Schottky barrier at gate metal contact can help suppress the gate leakage and enable aggressive insulator scaling.**

***Index Terms*—High electron mobility transistor (HEMT), InAs, InGaAs, nonequilibrium Greens function (NEGF), nonparabolicity, quantum well field effect transistor (QWFET), tight-binding.**

I. Introduction

As Si CMOS technology approaches the end of the ITRS roadmap, the semiconductor industry faces a formidable challenge to continue transistor scaling according to Moore's law [1]. Several industry and academic research groups have recently demonstrated high mobility III-V quantum well field-effect transistors (QWFETs), which can achieve high-speed operation at low supply voltage for applications beyond the reach of Si CMOS technology [2]–[8]. In particular, InGaAs and InAs channel QWFETs scaled down to 30 nm gate lengths have been shown to exhibit superior performance compared to Si MOSFETs and their heterogeneous integration on Si substrate has already been demonstrated [3]–[8].

Device simulations provide useful insights into the operation of QWFETs and might guide experimentalists in the process of scaling their gate length below 30 nm [9], [10]. In this paper, the performance of Schottky-gated InAs QWFETs is analyzed using quantum mechanical simulations.

Classical approximations such as the drift-diffusion model can neither capture the quantization of the energy levels resulting from the strong confinement of the electrons in a quantum well (QW) nor the tunneling currents in nano-scale devices. To address these limitations quantum mechanical approaches based on the effective mass approximation [10] and on the tight-binding method [9] have already been pursued. While both approaches agree well with experimental data above threshold, they are not able to reproduce the OFF-current region where gate leakage currents dominate. The absence of a real dielectric layer between the channel and the gate contact, contrary to MOSFETs, makes the III-V QWFETs very sensitive to gate leakage currents. To properly account for this effect, a multi-port, two-dimensional (2-D) real-space Schödinger-Poisson solver based on the effective mass approximation [11] has been developed. Band-to-band tunneling leakage and impact ionization do not have significant effect on the I–V's of the QWFETs in the operating range considered in this work and they are not included in the transport model. Hence, the OFF- and gate leakage currents are equivalent.

This paper is an expanded version of a recent conference proceeding [11]. A detailed discussion of the simulation methodologies and mechanisms behind the reported scaling trends in [11] are provided. The paper is organized as follows: in Section II, the device structure and its analysis through a decomposition into intrinsic and extrinsic simulation domains are introduced. Section III describes the core techniques used in this work: the 2-D real-space effective mass-based Schrödinger-Poisson solver, the tight-binding technique used to calculate the channel effective masses [12]–[14], and the Newton scheme employed to calibrate the simulator to experimental data. In Section IV, the simulator is benchmarked against the measured characteristics of InAs QWFETs with gate lengths ranging from 30 to 50 nm [7]. The calibrated simulator is subsequently used to optimize the logic performance of an InAs QWFET with a gate length scaled to 20 nm. The conclusions and outlook of this work are presented in Section V.

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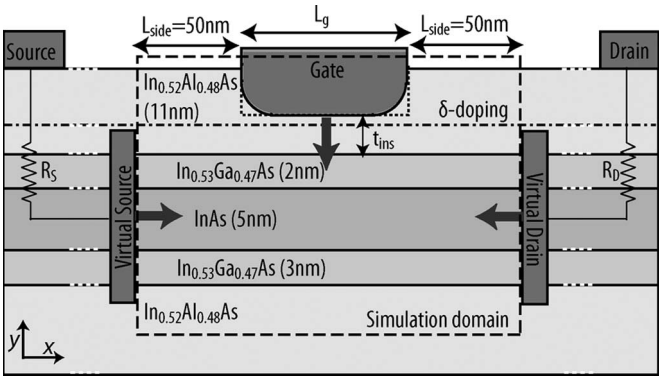

Fig. 1. Schematic view of an InAs QWFET. The dashed black rectangle encloses the quantum transport simulation domain i.e., the intrinsic device. Thick black arrows depict the direction of the electron injection from the virtual contacts into the simulation domain. Two gate contact geometries curved (solid line) and flat (dotted line) are investigated.

II. Device Description

The InAs QWFET [7] considered in this work is schematically shown in Fig. 1. The channel region is composed of a 10 nm $In_{0.53}Ga_{0.47}As$/InAs/$In_{0.53}Ga_{0.47}As$ (2/5/3 nm, from top to bottom) QW grown on a 500 nm thick $In_{0.52}Al_{0.48}As$ layer lattice matched to InP. The $In_{0.52}Al_{0.48}As$ layer between the QW channel and the gate contact acts as an insulator or barrier. A Si δ-doped layer of concentration 3×10^{12} cm^{-2} situated 0.3 nm below the gate contact supplies the channel conduction electrons. The source/drain contacts are located on the top of the device almost 1 μm away from the gated region.

To reduce the computational burden, this structure is analyzed by breaking it into two distinct domains. The intrinsic simulation domain is restricted to the region under the gate contact and an extension $L_{\rm side}$ of 50 nm on each side. The ideal contacts, labeled as virtual source/drain in Fig. 1, are placed at the two ends of the intrinsic device. The part of device outside the intrinsic domain is labeled as the extrinsic domain, which is modeled via two series resistances R_S and R_D following the procedure described in [15]. Due to the idealized contact assumption, phenomena such as source starvation are not included in our simulations [16].

Two gate contact geometries, curved and flat, resulting from different gate-stack fabrication processes are considered. The edges of the curved gate contact are quarter circles with the radius of curvature equal to $t_{\rm InAlAs} - t_{\rm ins}$, where, $t_{\rm InAlAs}$ is the total thickness of the top InAlAs layer and $t_{\rm ins}$ is the thickness of the InAlAs layer between the gate contact and the QW channel. Experimentally, a curved gate contact geometry is expected from the isotropic wet chemical etching process that is used to recess the gate [7].

III. Approach

A three-step multiscale modeling approach is adopted to simulate the InAs QW FETs. First the strain arising from the growth of an InAs layer in the middle of two $In_{0.53}Ga_{0.47}As$ layers is computed by an atomistic valence-force-field (VFF) method [17]. Then an atomistic tight-binding method [12], [13] is used to calculate the electron dispersion in the QW channel and the corresponding electron effective masses. In a third step, these effective masses are inserted into a quantum transport simulator that yields the current-voltage characteristics of the devices [18], [19].

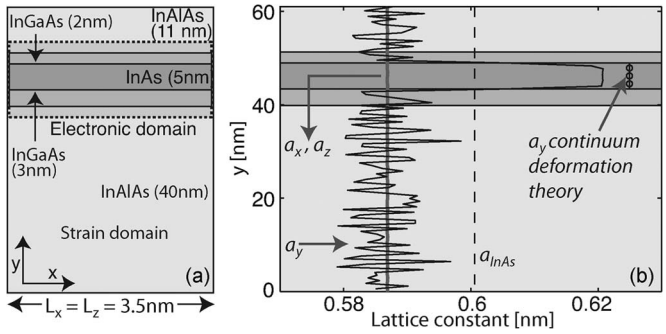

Fig. 2. (a) Schematic of the strain and electronic structure simulation domains. (b) In-plane lattice constant (a_x, a_z) through the center of the InAs QW and lattice constant along the growth direction (a_y). The unstrained lattice constant of InAs is labeled as $a_{\rm InAs}$.

A. Strain Relaxation

The InAs channel QWFETs are incorporated into an $In_{0.53}Ga_{0.47}As/In_{0.52}Al_{0.48}As$ heterostructure system as depicted in Fig. 2, which is epitaxially grown on an InP substrate. The $In_{0.53}Ga_{0.47}As$ and $In_{0.52}Al_{0.48}As$ layers are lattice matched to the InP substrate. InAs and InP, however, have a lattice mismatch of 3.2%, which gives rise to a biaxial compressive strain in the InAs channel region. Such biaxial compressive strain is known to increase the band gap of the InAs QW [9]. The valence-force-field (VFF) method with a modified Keating potential is used to compute the relaxed atom positions in the strained heterostructure [12], [13], [17]. The dimensions of the strain relaxation domain are given in Fig. 2(a). Since strain is a long-range effect, a 40 nm thick InAlAs layer below the InGaAs sub-channel is included. Periodic boundary conditions are applied to the axes perpendicular to the growth direction. Their dimensions are $L_x = L_z = 3.5$ nm. This domain contains 30 816 atoms and it is sufficiently large to model the random cations and disordered atom positions in the InGaAs and InAlAs layers [14] and to extract a transport and confinement effective mass, as shown later.

In Fig. 2(b), the lattice constants of the relaxed heterostructure are compared to the unstrained InAs lattice constant. The in-plane lattice constant along the center of the InAs QW (a_x, a_z) is compressed to the lattice constant of the InP substrate, causing an in-plane biaxial compressive strain of $\varepsilon_{\parallel} = a_x/a_{\rm InAs} - 1 = -0.031$. The lattice constant along the growth direction (a_y) is extended to 0.6207 nm in the InAs QW region, which corresponds to an orthogonal tensile strain $\varepsilon_{\perp} = 0.025$ and a Poisson ratio of $\nu = \varepsilon_{\perp}/\varepsilon_{\parallel} = 0.806$. The value of a_y estimated using the continuum deformation theory and the bulk value of the Poisson ratio $\nu = 1.088$ [20] is 0.6263 nm. The (a_y) fluctuations in the InGaAs and InAlAs regions are induced by the local bond length variation due to the random placement of the In, Ga, and Al cations and by the bi-modal In-As and Ga-As/Al-As bond length distribution [21], [22].

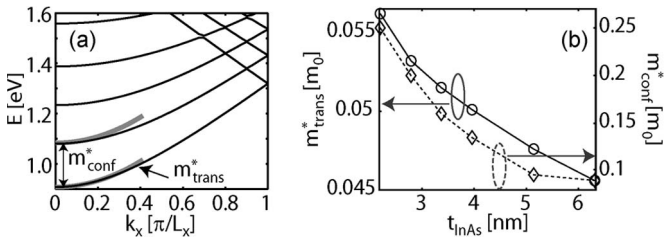

Fig. 3. (a) Bandstructure (at $k_z = 0$) of a 5 nm thick InAs QW embedded between InGaAs and InAlAs barriers. (b) Transport ($m^*_{\rm trans}$) and confinement ($m^*_{\rm conf}$) effective masses as function of the InAs QW thickness.

B. Tight-Binding Based Channel Effective Mass Extraction

An accurate computation of the channel effective mass is critical in devices subject to strain and strong bandstructure non-parabolicities, as is the case of InAs. The effective mass determines the channel properties such as injection velocity, source-to-drain tunneling, quantum capacitance, and density-of-states [23]. Here, the effective masses of the multi-quantum-well channel are extracted from a $sp^3d^5s^*$ tight-binding bandstructure that includes strain. The electronic structure simulator NEMO-3D [12]–[14] is used for this computation. The InAs, GaAs, and AlAs tight-binding parameters are taken from Refs. [12], [24]. The bulk parameters are fully transferable to nanostructures and have previously been benchmarked against complex experimental devices such as InAs/InGaAs/InAlAs quantum dots [22] and InAs QWFETs [9].

The tight-binding electronic structure calculation domain [Fig. 2(a)] is smaller than the strain relaxation domain. Only 2 nm thick portions of the InAlAs layers on the top and the bottom of the $In_{0.53}Ga_{0.47}As/InAs/In_{0.53}Ga_{0.47}As$ QW channel are included since the penetration of the wavefunction beyond this domain is negligible. The in-plane dimensions are the same as the strain relaxation domain. The electronic structure domain contains 7776 atoms. The bandstructure of the QW active region with a 5 nm thick InAs layer is shown in Fig. 3(a). The effect of strain and quantization due to band discontinuities at the InAs/InGaAs and InGaAs/InAlAs heterostructure interfaces are included in the tight-binding Hamiltonian. The bands shown in Fig. 3(a) are the Γ valley sub-bands. The L valley sub-bands (not shown) are at least 0.9 eV higher than the lowest Γ valley sub-band for the InAs channel thicknesses considered here. Due to the large energy separation and the low supply voltages that are applied to the devices ($V_{\rm DD} = 0.5$ V), the L valleys do not affect the operation of InGaAs based QWFETs [10] and are safely ignored in the transport calculations.

The Γ valley transport effective mass ($m^*_{\rm trans}$) is extracted by fitting a parabola to the lowest conduction sub-band. The transport effective mass may also be obtained directly from the wavefunctions using the method presented in [25], [26], which is capable of resolving bandstructure degeneracies more accurately than the parabolic fitting method. These degeneracies do not occur in the Γ-valley dominant materials such as InAs therefore the parabolic fitting method suffices for the calculations presented here. The confinement effective mass ($m^*_{\rm conf}$) is fitted to replicate the energy difference between the first two sub-bands [Fig. 3(a)]. The InGaAs and InAlAs layers around the InAs channel are included in the effective mass calculation since the band discontinuities at the interfaces and the wavefunction penetration into these layers affect the confinement in the channel. The values of the band-offsets at the heterostructure interfaces in the effective mass calculation are $\Delta E_{C,{\rm InGaAs/InAs}} = 0.4$ eV and $\Delta E_{C,{\rm InGaAs/InAlAs}} = 0.5$ eV, while the transport effective masses of $In_{0.53}Ga_{0.47}As$ and $In_{0.52}Al_{0.48}As$ are $0.041 \cdot m_0$ and $0.075 \cdot m_0$, respectively [27], [28]. The $In_{0.53}Ga_{0.47}As$ and $In_{0.52}Al_{0.48}As$ effective masses along the growth direction are used as fitting parameters to obtain the correct gate leakage current as explained later.

Such an elaborate, atomistic-based fitting procedure allows for an accurate determination of the channel transport and confinement effective masses. As shown in Fig. 3(b), both the transport and confinement effective masses in the InAs QW are significantly larger than their bulk value ($m^*_{\rm InAs} = 0.023 \cdot m_0$) due to the strong quantum confinement, the wavefunction penetration into the heavier effective mass InGaAs and InAlAs barrier layers, and the biaxial strain. The effective masses become heavier as the QW thickness is reduced emphasizing the strong non-parabolic dispersion of InAs.

C. 2-D Real Space Effective Mass Simulator

The Schrödinger and Poisson equations are solved self-consistently using the effective mass approximation on a 2-D finite-difference grid [18]. The grid is uniform and the spacing along the x and y-directions are $\Delta x = 0.25$ nm and $\Delta y = 0.2$ nm, respectively. The quantum transport simulation domain is shown in Fig. 1. In the Poisson calculation, Dirichlet boundary conditions are applied to the gate contact (the potential is fixed) while Von Neumann boundary conditions are applied to the remaining boundaries (the electric field is set to 0). Consequently, the potential in the source and drain extensions automatically adjusts itself to ensure charge neutrality and zero electric field at the boundaries [15]. In the ballistic transport model used here, electrons are injected into the device from the source, drain, and gate contacts at different energy values and the resulting contributions are summed up to obtain the carrier and current densities. The real space technique accurately accounts for the longitudinal (x-axis) and transverse (y-axis) mode coupling [18] and for gate leakage currents.

D. Calibration Methodology

To calibrate the simulator to the experimental data, five fitting parameters are used: i) L_g–the gate length, ii) $t_{\rm ins}$–the thickness of the InAlAs insulator layer between the QW channel and the gate contact, iii) $m^*_{\rm ins}$–the effective mass of the InAlAs insulator along the growth direction (y), iv) $m^*_{\rm buf}$–the effective mass of the InGaAs sub-channels along the growth direction (y), and (v) Φ_B–the Schottky barrier height at the gate metal contact. The leakage and sub-threshold (low $V_{\rm gs}$) regimes of the I_d–$V_{\rm gs}$ characteristics are chosen as fitting regions because the currents are very sensitive to the device dimensions and material parameters there, but they do not depend on the source and drain series resistances. As a result, the gate leakage current and the subthreshold slope are properly modeled. The currents

at high $V_{\rm gs}$ are mainly governed by the source and drain series resistances, which are not adjusted but set to the experimentally measured values, $R_S = 0.21\ \Omega \cdot$ mm and $R_D = 0.23\ \Omega \cdot$ mm.

The selection of the fitting parameters is based on two criteria: i) the fabrication process variability and ii) the sensitivity of the drain current. L_g and $t_{\rm ins}$ are respectively determined by lithography and wet chemical etching processes, which are prone to variability [7], [29]. Likewise, the difficulty of controlling the surface conditions before metal deposition induces process variability in Φ_B [6], [30]. The effective masses of the $In_{0.53}Ga_{0.47}As$ and $In_{0.52}Al_{0.48}As$ top layers along the growth direction ($m^*_{\rm buf}$ and $m^*_{\rm ins}$ respectively) are not accurately known from the experimental measurements and are also included in the fitting procedure. Their values, however, are allowed to vary only within the experimentally reported ranges [27], [28]. The 2-D electrostatics is governed by L_g and $t_{\rm ins}$, while $t_{\rm ins}$, $m^*_{\rm buf}$, $m^*_{\rm ins}$, and Φ_B control the electron tunneling probability from the gate into the InAs channel, which in turn determines the gate leakage current.

The thickness of the InAs channel and the InGaAs buffer are not included in the fitting procedure because they are determined by the Molecular Beam Epitaxy (MBE) growth, which is a precise atomic layer deposition technique. The electron affinity of the InAs channel ($\chi = 4.9$ eV [28]) and the conduction band offsets at the heterostructure interfaces ($\Delta E_{C,\rm InGaAs/InAs} = 0.4$ eV and $\Delta E_{C,\rm InGaAs/InAlAs} = 0.5$ eV [27], [28]) are not considered as fitting parameters because the drain current is weakly sensitive to them.

The drain current is parameterized as $I_d(L_g, t_{\rm ins}, m^*_{\rm ins}, m^*_{\rm buf}, \Phi_B)$. An iterative approach (Fig. 4) is used where, at each iteration, the subthreshold I_d–$V_{\rm gs}$ characteristics are computed and compared to the experimental data. If the deviation from the experimental data is larger than the tolerance, a new guess to the parameter vector is computed using a Newton-Raphson scheme [31]. The partial derivatives composing the Jacobian matrix are computed numerically. For example, the partial derivative with respect to the gate length L_g is $\partial I_d/\partial L_g = (I_d^{i,\delta L_g} - I_d^i)/\delta L_g$ where, i is the iteration count, I_d^i is the drain current of the reference device parameterized as $I_d^i(L_g^i, t_{\rm ins}^i, m_{\rm ins}^{*i}, m_{\rm buf}^{*i}, \Phi_B^i)$, δL_g is change in the gate length of a new device from the reference device, and $I_d^{i,\delta L_g}$ is the drain current of a new device parameterized as $I_d^{i,\delta L_g}(L_g^i + \delta L_g, t_{\rm ins}^i, m_{\rm ins}^{*i}, m_{\rm buf}^{*i}, \Phi_B^i)$. The same procedure is repeated to compute the partial derivatives with respect to $t_{\rm ins}$, $m^*_{\rm ins}$, $m^*_{\rm buf}$, and Φ_B. The parameter shifts used to compute the numerical derivatives are $(\delta L_g, \delta t_{\rm ins}, \delta m^*_{\rm ins}, \delta m^*_{\rm buf}, \delta \Phi_B) = (0.5\ \text{nm}, 0.2\ \text{nm}, 0.005 \cdot m_0, 0.005 \cdot m_0, 0.05\ \text{eV})$, where m_0 is the free electron mass. For each device, the voltage sweep shown in Fig. 4(a) requires typically 4 hours on 40 cores on a 2.5 GHz quad core AMD 2380 processor [32].

IV. Results

The methodology presented in Section III is first used to calibrate the simulator against experimental I_d–$V_{\rm gs}$ from devices with gate lengths ranging from 30 nm to 50 nm [7]. The calibration phase can be seen as a metrology experiment, where the actual gate lengths and material properties are estimated. The resulting calibrated simulator is then used to optimize the design of a 20 nm gate length device.

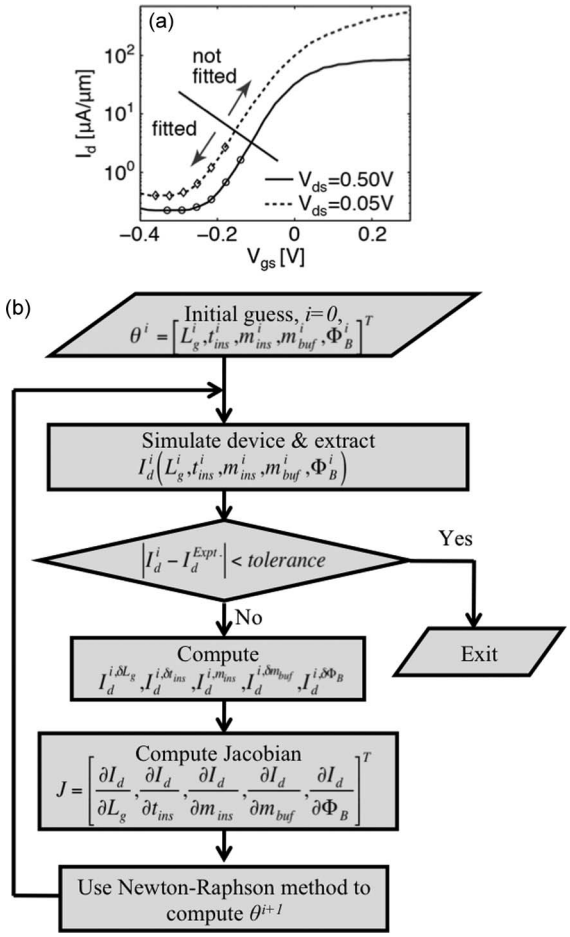

Fig. 4. (a) Experimental I_d–$V_{\rm gs}$ characteristics of the 30 nm gate length device. (b) Flow chart of the parameter fitting procedure.

A. Comparison to Experimental Data

Gate leakage currents are much larger in QWFETs than in conventional Si MOSFETs due to the absence of a proper insulator layer such as SiO_2 or HfO_2. Moreover, the gate contact geometry plays an important role in determining the magnitude of the gate leakage currents. The shape of the gate contact depends on the fabrication technique used to thin down the insulator before deposing the gate metal stack. Anisotropic etching and metal gate sinking ideally lead to a flat gate contact while isotropic etching leads to a curved gate contact (Fig. 1).

Flat or curved gate contact geometries act differently on the leakage current magnitude as illustrated in Fig. 5(a). Both devices perform similarly in the high $V_{\rm gs}$ regime. The flat gate device exhibits a lower subthreshold slope $SS = 83.5$ mV/dec as compared to the curved gate device ($SS = 89.7$ mV/dec), but its gate leakage current is about $2\times$ higher. The difference between the drain currents at low $V_{\rm gs}$ is the result of gate leakage (I_g) suppression in the curved gate contact device.

The current distribution in the gate leakage regime is shown in Fig. 5(b) and (c). Gate leakage currents are concentrated at

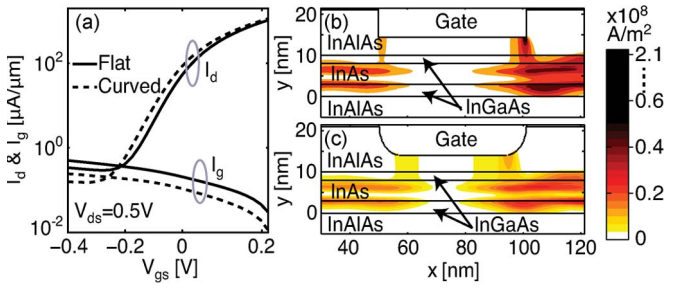

Fig. 5. (a) Intrinsic I_d–$V_{\rm gs}$ and I_g–$V_{\rm gs}$ characteristics of an InAs QWFET ($L_g = 51$ nm) with a flat (solid lines) and a curved (dashed lines) gate contact. OFF-state ($V_{\rm gs} = -0.4$ V and $V_{\rm ds} = 0.5$ V) current distribution in (b) a flat gate contact device and (c) a curved gate contact device.

TABLE I
DEVICE DIMENSIONS AND MATERIAL PARAMETERS OBTAINED FROM THE FITTING PROCEDURE

Parameter	Initial	Final parameter set		
		30 nm	40 nm	50 nm
L_g[nm]	30, 40, 50	34	42	51.25
t_{ins}[nm]	4	3.6	3.8	4.0
Φ_B[eV]	0.7	0.660	0.693	0.678
$m^*_{ins}[m_0]$	0.075	0.078		
$m^*_{buf}[m_0]$	0.045	0.041		

the edges of the contact due to lower tunneling barriers and higher electric fields there as compared to the central region of the gate contact [11]. The curved gate device is characterized by a thicker insulator at the edges of the gate contact, which leads to a suppression of the leakage current. Thus, an accurate description of the gate contact geometry is crucial to reproduce the experimental I_d–$V_{\rm gs}$, especially in the leakage and subthreshold regimes, and can be seen as a design parameter. A curved gate geometry is clearly seen in the TEM micrographs of [7]. A curved gate geometry, which resembles that of the experimental devices, is therefore used in the benchmarking procedure. As shown in Fig. 1, the shape of the edges of the curved gate contact is a quarter circle with the curvature radius equal to $t_{\rm InAlAs} - t_{\rm ins}$, which changes as $t_{\rm ins}$ changes in the fitting procedure.

The results of the device metrology for devices with gate lengths ranging from 30 nm to 50 nm are listed in Table I. Here, the transport and confinement effective mass values extracted from the tight-binding bandstructures are used in the InAs channel region, which for a 5 nm thick InAs channel amount to $m^*_{\rm trans} = 0.049 \cdot m_0$ and $m^*_{\rm conf} = 0.096 \cdot m_0$, respectively [Fig. 3(b)]. The parameter values at the end of the fitting procedure are close to the experimentally reported values, which are used as an initial guess [7]. The effective masses of the InGaAs buffer ($m^*_{\rm buf}$) and the InAlAs insulator ($m^*_{\rm ins}$) layers are not allowed to vary between the different devices since they are all fabricated side by side on the same heterostructure. The effective mass values after convergence of the fitting process are within the ranges reported in the literature, which are $0.038 \cdot m_0 - 0.044 \cdot m_0$ for $In_{0.53}Ga_{0.47}As$ and $0.070 \cdot m_0 - 0.083 \cdot m_0$ for $In_{0.52}Al_{0.48}As$ [27], [28]. The converged values for the gate length and insulator thickness are within the expected process variability of the wet chemical etching step used to thin

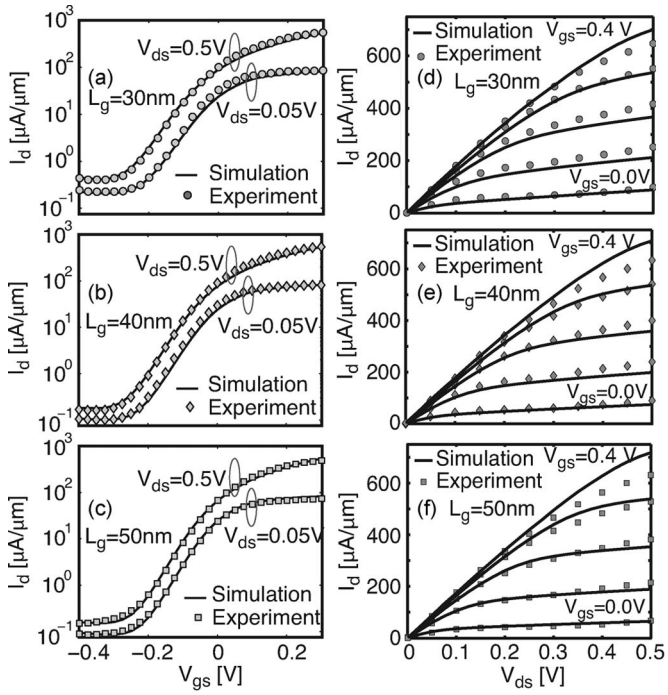

Fig. 6. Comparison between the experimental and simulated I_d–$V_{\rm gs}$ characteristics of (a) 30 nm, (b) 40 nm, and (c) 50 nm QWFETs and I_d–$V_{\rm ds}$ characteristics of (d) 30 nm, (e) 40 nm, and (f) 50 nm gate length InAs QWFETs. The I_d–$V_{\rm ds}$ characteristics in figures (d)-(f) are calculated at $V_{\rm gs}$ equal to 0.0 V, 0.1 V, 0.2 V, 0.3 V, and 0.4 V.

TABLE II
DEVICE PERFORMANCE PARAMETERS OF THE SIMULATED AND EXPERIMENTAL DEVICES

L_g [nm]		I_{OFF} [μA/μm]	SS [mV/dec]	$DIBL$ [mV/V]	I_{ON}/I_{OFF}	v_{inj} [cm/s]
30	Expt.	0.4077	106.9	168.9	0.47×10^3	
30	Sim.	0.4431	105.2	144.7	0.61×10^3	3.0×10^7
40	Expt.	0.1607	90.9	126.0	1.38×10^3	
40	Sim.	0.1789	89.4	99.3	1.86×10^3	3.11×10^7
50	Expt.	0.1696	85.1	97.2	1.80×10^3	
50	Sim.	0.1519	89.2	90.8	1.85×10^3	3.18×10^7

down the InAlAs insulator prior to gate metal deposition [7]. Slightly different values of Φ_B are justified because of the lack of precise control of the surface oxides, which modify its value from device to device [7].

The experimental transfer I_d–$V_{\rm gs}$ and output I_d–$V_{\rm ds}$ characteristics are compared to the simulation results in Fig. 6. It should be noted that only the low $V_{\rm gs}$ regime is used in the fitting procedure as described in Fig. 4. The performance parameters extracted from the experimental and simulated I_d–$V_{\rm gs}$ in Fig. 6 agree reasonably well, as shown in Table II. The injection velocity ($v_{\rm inj} = I_{\rm ON}/Q_{\rm top}$) is calculated at the top of the potential barrier in the InAs channel [23].

At high biases, the I–V characteristics are dominated by the source and drain contact resistances, which are modeled as two external series resistances R_S and R_D attached to the intrinsic device (Fig. 1). The I_d–$V_{\rm gs}$ and I_d–$V_{\rm ds}$ characteristics of the intrinsic device are calculated for the bias ranges $-0.4 \le V^{\rm int}_{\rm gs} \le 0.3$ V and $0 \le V^{\rm int}_{\rm ds} \le 0.5$ V. The extrinsic

device characteristics are then computed from the drain current, I_d, at given extrinsic terminal voltages ($V_{\rm gs}$ and $V_{\rm ds}$) using $V_{\rm gs} = V_{\rm gs}^{\rm int} + R_S I_d$ and $V_{\rm ds} = V_{\rm ds}^{\rm int} + (R_S + R_D) I_d$ [15]. The good quantitative agreement shown in Fig. 6 is enabled by the consideration of a curved gate contact geometry, an accurate estimation of the channel effective masses, as well as the parameter adjustments listed in Table I.

The simulated I_d–$V_{\rm ds}$ characteristics show a very good agreement with the experimental I_d–$V_{\rm ds}$ at low bias voltages while I_d is overestimated at high bias voltages (Fig. 6). The overestimation of I_d is related to the fact that scattering is not included in the ballistic quantum transport model. Electron-phonon, interface roughness, and alloy disorder scattering appear to play a non-negligible role at high biases. The deviation between the simulated and experimental I_d is larger in devices with a longer gate contact. In effect, electron transport in longer devices is more affected by scattering than in shorter devices, which operate closer to their ballistic limit.

B. Design Optimization of a 20 nm Device

After benchmarking the simulation approach and providing metrology insight into experimental devices, we explore the performance of a hypothetical 20 nm gate length device. The effects of the InAs channel thickness ($t_{\rm InAs}$), the InAlAs insulator thickness ($t_{\rm ins}$), and the Schottky barrier height at the gate metal contact (Φ_B) are investigated.

A flat gate contact geometry provides a superior gate control of the channel potential as compared to a curved contact (Fig. 5) at the price of higher gate leakage current. Since the leakage can be reduced through Schottky barrier engineering, as explained later, a flat gate geometry will be used in the performace evaluation of the 20 nm gate length device. A flat gate contact can be "easily" fabricated by replacing the isotropic wet chemical etching step used to thin down the InAlAs insulator layer by an anisotropic etching or by a metal gate sinking technique [6]. These advanced fabrication techniques will result in smaller radius of curvature or near ideal flat contact.

The performance parameters (SS, $DIBL$, and $I_{\rm ON}/I_{\rm OFF}$ ratio) are calculated by using the constant overdrive voltage method [33]. The threshold voltage V_T is determined from a linear extrapolation of the I_d–$V_{\rm gs}$ characteristics at the peak transconductance to zero I_d (maximum-g_m method [34]) and a supply voltage $V_{\rm DD}$ of 0.5 V is used. The ON-state is defined as $V_{\rm gs} = V_T + 2V_{\rm DD}/3$, $V_{\rm ds} = V_{\rm DD}$ while the OFF-state is defined as $V_{\rm gs} = V_T - V_{\rm DD}/3$, $V_{\rm ds} = V_{\rm DD}$. The capacitances are defined as i) the gate capacitance: $C_g = dQ_s/dV_{\rm gs}$, ii) the insulator capacitance: $C_{\rm ins} = \varepsilon_{\rm ins}/t_{\rm ins}$, and iii) the inversion layer capacitance: $C_{\rm inv} = dQ_s/d\psi_s$ [35]. Here, Q_s is the sheet charge density in the InGaAs/InAs/InGaAs composite channel, ε_{ins} is the dielectric constant of the InAlAs barrier, and ψ_s the surface potential at the interface between the barrier and the composite channel.

1) InAs Channel Thickness ($t_{\rm InAs}$): The effect of scaling down $t_{\rm InAs}$ can be analyzed by noting that the QWFET is electrostatically very similar to a fully depleted silicon on insulator (FD-SOI) MOSFET [29], [36], [37]. In a QWFET, the InAs channel thickness plays a role similar to the Si body thickness in a FD-SOI MOSFET. Higher gate length to channel thickness ratio in a thin InAs channel QWFET results in a stronger gate control of the channel surface potential, which improves SS and $DIBL$ [Fig. 7(a)].

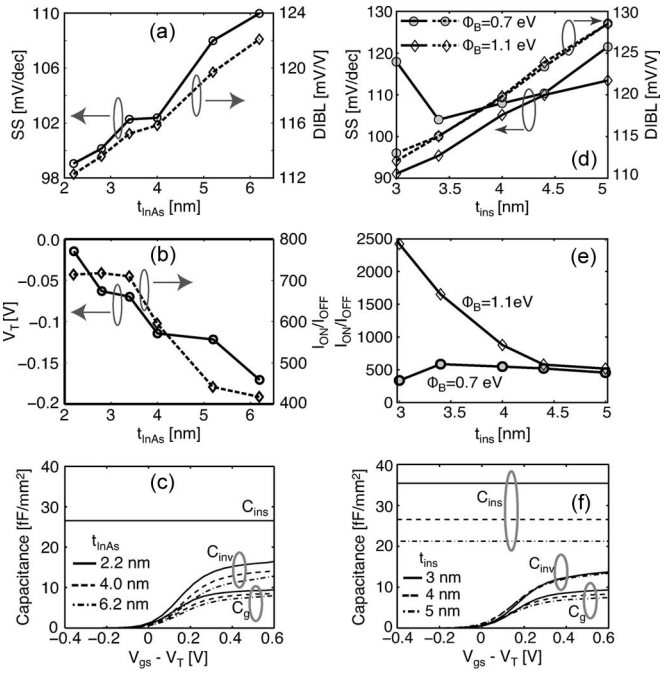

Fig. 7. (a)–(c) InAs QW thickness ($t_{\rm InAs}$) scaling. (a) SS and $DIBL$. (b) V_T and $I_{\rm ON}/I_{\rm OFF}$ ratio. (c) C_g and $C_{\rm inv}$ as function of the gate overdrive ($V_{\rm gs} - V_T$). The same device dimensions (except $t_{\rm InAs}$) as in Fig. 1 are used. $t_{\rm ins} = 4$ nm. $\Phi_B = 0.7$ eV. (d)–(f) InAlAs insulator thickness ($t_{\rm ins}$) scaling. (c) SS and $DIBL$ and (d) $I_{\rm ON}/I_{\rm OFF}$ ratio of devices with $\Phi_B = 0.7$ eV and 1.1 eV. (e) C_g and $C_{\rm inv}$ as function of ($V_{\rm gs} - V_T$). The same device dimensions (except $t_{\rm ins}$) as in Fig. 1 are used. $L_g = 20$ nm.

The strong electrostatic confinement of electrons in thin InAs QW devices pushes the channel conduction subbands to higher energies, which subsequently results in higher V_T and facilitates enhancement mode operation of such devices [Fig. 7(b)].

The channel effective mass along the transport direction increases as $t_{\rm InAs}$ decreases (Fig. 3), which leads to a lower electron injection velocity ($v_{\rm inj}$), but a higher carrier density ($N_{\rm inv}$) at the QWFET virtual source [38]. The net effect is a higher $I_{\rm ON}$ in thin InAs channel devices. The 2-D electron gas in thinner channel devices is located closer to the gate, resulting into a higher gate leakage and $I_{\rm OFF}$. As $t_{\rm InAs}$ is slightly reduced, the higher $I_{\rm ON}$ more than compensates the larger $I_{\rm OFF}$, so that the $I_{\rm ON}/I_{\rm OFF}$ ratio actually increases. However, if $t_{\rm InAs}$ is further reduced, the increase of $I_{\rm OFF}$ becomes more important and the $I_{\rm ON}/I_{\rm OFF}$ ratio starts to saturate [Fig. 7(b)].

The total gate capacitance, C_g, which is the series combination of $C_{\rm ins}$ and $C_{\rm inv}$, increases as $t_{\rm InAs}$ decreases due to the increase in $C_{\rm inv}$ [Fig. 7(c)]. The increase in $C_{\rm inv}$ in thin $t_{\rm InAs}$ devices is attributed to the increase of both its components, namely the quantum capacitance C_Q and the centroid capacitance $C_{\rm cent}$. C_Q increases because of a higher effective mass while $C_{\rm cent}$ increases because the electron gas is closer to the gate in thin $t_{\rm InAs}$ devices [39].

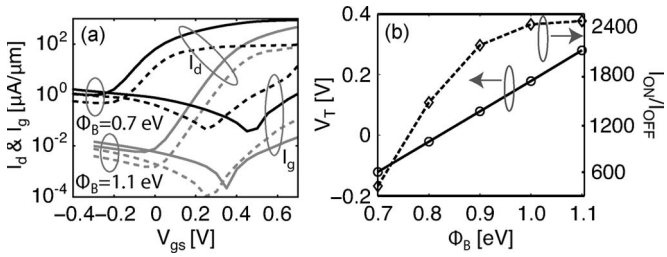

Fig. 8. (a) I_d–$V_{\rm gs}$ and I_g–$V_{\rm gs}$ characteristics of InAs QWFETs with $\Phi_B = 0.7$ eV and 1.1 eV. (b) V_T and $I_{\rm ON}/I_{\rm OFF}$ ratio as function of Φ_B. The device dimensions are the same as in Fig. 1 with $L_g = 20$ nm and $t_{\rm ins} = 3$ nm.

2) InAlAs Insulator Thickness ($t_{\rm ins}$): The scaling behavior of $t_{\rm ins}$ in devices with Φ_B of 0.7 eV and 1.1 eV is illustrated in Fig. 7(d)–(f). When $\Phi_B = 0.7$ eV, the performance metrics SS, $DIBL$, and $I_{\rm ON}/I_{\rm OFF}$ ratio improve as $t_{\rm ins}$ is scaled down until 3.4 nm. This can be attributed to a better electrostatic control of the channel in thin insulator devices. When $t_{\rm ins}$ is scaled below 3.4 nm, $DIBL$ keeps decreasing, while the SS and $I_{\rm ON}/I_{\rm OFF}$ ratio, which are affected by the electron tunneling across the InAlAs insulator, start degrading due to an excessive gate leakage. This degradation can be controlled by increasing Φ_B to 1.1 eV, which increases the tunneling barrier height between the gate and the InAs channel, reduces the gate leakage, and therefore improves the SS and $I_{\rm ON}/I_{\rm OFF}$ ratio even with the InAlAs layer scaled down to 3 nm [Fig. 7(d) and (e)].

Since III–V devices are characterized by a small density-of-states effective mass and therefore small $C_{\rm inv}$, the down scaling of $t_{\rm ins}$ does not significantly increase C_g [Fig. 7(f)]. Similar trends in C_g are observed in the experiments [39].

3) Schottky Barrier at the Gate Metal Contact (Φ_B): As shown in Fig. 7(d) and (e), a device with $\Phi_B = 1.1$ eV shows a significant improvement in SS and $I_{\rm ON}/I_{\rm OFF}$ ratio compared to a device with $\Phi_B = 0.7$ eV. To explain this effect the I_d–$V_{\rm gs}$ and I_g–$V_{\rm gs}$ characteristics of devices with the same $t_{\rm ins} =$ 3 nm, but different Φ_B (0.7 and 1.1 eV) are compared in Fig. 8. Under the same bias conditions, the device with $\Phi_B = 1.1$ eV shows a 100× smaller gate leakage current (I_g) as compared to the device with $\Phi_B = 0.7$ eV. The longitudinal and transverse band-diagrams of the same devices in the OFF-state ($V_{\rm ds} = V_{\rm DD}$, $V_{\rm gs} - V_T = -V_{\rm DD}/3$) are shown in Fig. 9. The same $V_{\rm ds}$ and $V_{\rm gs} - V_T$ result in almost the same band bending along the channel ensuring the same source to drain current in both devices. Electrons tunneling from the gate terminal into the channel experience a higher energy barrier in the $\Phi_B = 1.1$ eV device as compared to the $\Phi_B = 0.7$ eV device because of the metal gate Fermi level offset equal to the Schottky barrier difference ($\Delta\Phi_B = 0.4$ eV). With $\Phi_B = 0.7$ eV, the gate electrons must tunnel through the InAlAs insulator layer only to reach the InAs channel while they must tunnel through the InAlAs and InGaAs layers when $\Phi_B = 1.1$ eV, considerably reducing the gate leakage current.

Although I_g of the device with $\Phi_B = 1.1$ eV shows a 100× reduction, its $I_{\rm ON}/I_{\rm OFF}$ ratio shows only a 7× improvement compared to the device with $\Phi_B = 0.7$ eV [Fig. 7(e)]. This is due to the fact that the OFF-current, when $\Phi_B = 1.1$ eV, is no longer dominated by gate leakage currents, but by the thermionic emission of electrons from the source to the drain.

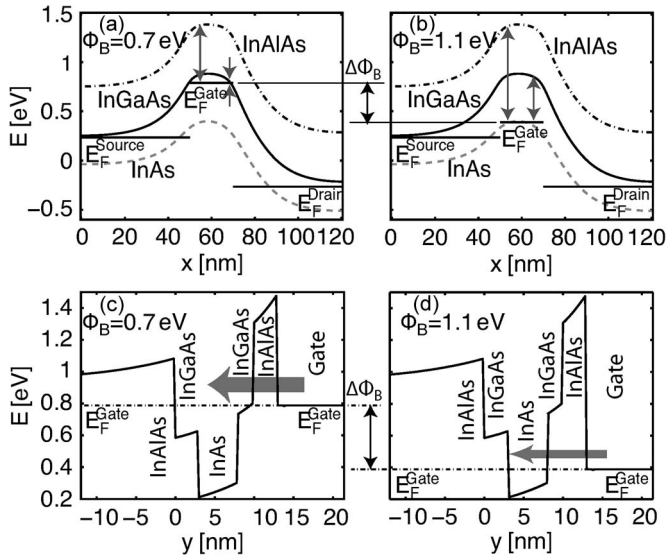

Fig. 9. (a) Conduction band diagrams along three horizontal lines through the center of i) the InAlAs insulator, ii) the top InGaAs barrier, and iii) the InAs channel of a $L_g = 20$ nm InAs QWFET with $\Phi_B = 0.7$ eV in the OFF-state. (b) Same as (a) but for $\Phi_B = 1.1$ eV. (c) Band diagram of the device in (a) along a vertical line near the drain side edge of the gate contact. (d) Same as (c) but for $\Phi_B = 1.1$ eV. The thickness of the arrows in [(c), (d)] schematically shows the direction and the magnitude of the electron tunneling current.

In addition to a larger $I_{\rm ON}/I_{\rm OFF}$ ratio, a higher Φ_B pushes the threshold voltage V_T toward positive values. In Fig. 8, the V_T values of the devices with $\Phi_B = 0.7$ eV and $\Phi_B = 1.1$ eV are -0.11 V and 0.29 V, respectively. The positive shift in V_T is equal to the Schottky barrier difference $\Delta\Phi_B = 0.4$ eV. Such a positive V_T shift is highly desirable for the enhancement mode operation of the n-type FET in CMOS logic applications [4], [6]. The variation of the $I_{\rm ON}/I_{\rm OFF}$ ratio and V_T for the intermediate values of Φ_B are shown in Fig. 8(b). A higher Φ_B linearly pushes V_T toward a positive value while the $I_{\rm ON}/I_{\rm OFF}$ ratio increases in a nonlinear fashion. Higher Φ_B values can be achieved by using higher work function metals and semiconductor surface treatments [6], [30], [40].

V. Conclusion

The performances of InAs QWFETs have been analyzed by using a multiscale device simulation approach. The effective mass of the InAs channel raises significantly from its bulk value due to strong confinement effects, which are included on the atomistic scale through a $sp^3d^5s^*$ tight-binding model. The gate tunneling is critical in the device analysis and is included in a 2-D Schrödinger-Poisson solver by injecting carriers from the gate contact in addition to the source and drain contacts. The simulation approach is calibrated against experimental devices with gate lengths ranging from 30 to 50 nm. A good quantitative match between the experimental and simulated current-voltage characteristics is reported. The accurate description of the shape of the gate contact is essential to replicate the experimental results.

The calibrated simulation methodology has been used to investigate the design optimizations of a hypothetical 20 nm gate length InAs QWFET. The scaling of the InAs channel thickness and the InAlAs insulator thickness improve the logic

performance due to a stronger gate control of the channel potential. An excessive scaling, however, leads to higher gate leakage current, which degrades the device performances. The gate leakage current can be suppressed by increasing the Schottky barrier height at the gate metal contact, which also pushes the threshold voltage toward the enhancement mode operation. As a result of the reduced gate leakage, devices with higher Schottky barrier can be scaled more aggressively compared to devices with lower Schottky barrier.

The simulation tool, OMEN_FET, that generated the results presented in this paper is available on nanoHUB.org [19].

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