InGaAs HEMT with InAs-rich InAlAs barrier spacer for reduced source resistance

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An InAlAs/InGaAs HEMT with an InAs-rich barrier spacer ($In_{0.52}Al_{0.48}As$) to reduce the parasitic resistance is reported. Devices were obtained with a source resistance of 170 Ω-μm. A 40 nm gate length $In_{0.7}Ga_{0.3}As$ HEMT with $L_{side} = 100$ nm and $t_{ins} = 10$ nm shows excellent transconductance and subthreshold characteristics including $g_m = 1.6$ mS/μm, DIBL = 122 mV/V and S = 80 mV/dec at $V_{DS} = 0.5$ V. In addition, this device exhibits an $f_T = 530$ GHz and $f_{max} = 445$ GHz at $V_{DS} = 0.7$ V. These excellent characteristics mainly arise from a reduction in the source resistance through the use of the InAs-rich InAlAs spacer.

Introduction: InP-based high electron transistors (HEMTs) have shown excellent high frequency performance including a current gain cutoff frequency f_T of 644 GHz and a maximum oscillation frequency (f_{max}) of over 1 THz [1, 2]. The current bottleneck for further improvement in frequency response is the reduction in parasitic elements, among which the source and drain resistance are particularly important [3]. Studies on the source resistance of HEMTs suggest that the barrier resistance associated with the cap/barrier/channel heterointerface ($R_{barrier}$) constitutes its major portion [4, 5]. Recently, we reported a reduced source resistance of 147 Ω-μm by using dual Si delta doping in the InAlAs barrier and self-aligned ohmic contacts [6]. In this Letter, we explore a separate approach to reduce the source resistance and that is the use of an InAs-rich InAlAs barrier spacer layer. This is expected to lower the barrier resistance by reducing the conduction band discontinuity between the channel and the barrier. A possible trade-off of this approach is an increased gate leakage current. We show that appropriate design minimises this problem.

Experiments: The epitaxial layer structure used in this work is similar to our previous report [1] except for the design of the InAlAs barrier above the channel and the channel itself. In the present design, the bottom 2 nm spacer of the barrier is made out of $In_{0.62}Al_{0.48}As$ while the rest of the barrier has a lattice matched composition with 48% InAs. The total thickness of the barrier is 11 nm. As the channel, we used a single 10 nm-thick $In_{0.7}Ga_{0.3}As$ layer. In an epi wafer with an identical heterostructure except for a simpler 10 nm InGaAs cap with 1×10^{18}/cm^3 Si doping, the Hall mobility ($\mu_{n,Hall}$) and carrier density (n_s) were 9,740 cm^2/V-s and 3.2×10^{12}/cm^2.

This layer design is expected to result in lower barrier resistance because one of the energy spikes in the conduction band under the contact regions is eliminated. A potential trade-off is an increased gate leakage current due to the reduced conduction band discontinuity between channel and barrier. However, if the gate voltage is not too forward biased, the highest energy barrier under the gate is the Schottky barrier of the gate itself and this is unchanged in the present approach. As a result, the gate leakage current over the useful operating range is not expected to increase.

Device fabrication closely follows our previous device demonstrations [1]. We used an evaporated and lifted off Mo/Ti/Mo/Au metal system to achieve low contact resistance [6], a two-step cap recess process and a T-shaped Ti/Pt/Au (20/20/300 nm) gate fabricated through a SiO_2-assisted process with a stem height of 150 nm to minimise parasitic capacitance. We have fabricated devices with L_g values in the range of 40 to 200 nm. The side-recess length (L_{side}) was set at about 100 nm to ensure optimum device performance included low OFF-state current and gate leakage characteristics.

Results and discussion: Fig. 1 shows output characteristics of the fabricated InGaAs HEMTs with gate lengths from 40 to 200 nm. The devices show excellent pinch-off and saturation current and very low ON resistance with the shortest device exhibiting $R_{ON} = 350$ Ω-μm. Fig. 2 shows subthreshold and gate current characteristics of an $L_g = 40$ nm InGaAs HEMT at $V_{DS} = 50$ mV and 0.5 V. The device shows excellent subthreshold characteristics. At a $V_{DS} = 0.5$ V, the subthreshold swing (S) is 80 mV/dec, the drain-induced-barrier-lowering (DIBL) is 122 mV/V and the I_{ON}/I_{OFF} ratio is 3×10^4. As expected, the device exhibits gate-leakage current and OFF-state current just as good as devices with a lattice-matched barrier of a similar thickness [7]. Fig. 3 shows transconductance characteristics at $V_{DS} = 0.5$ V. The device with $L_g = 40$ nm exhibits a maximum transconductance of 1.6 S/mm.

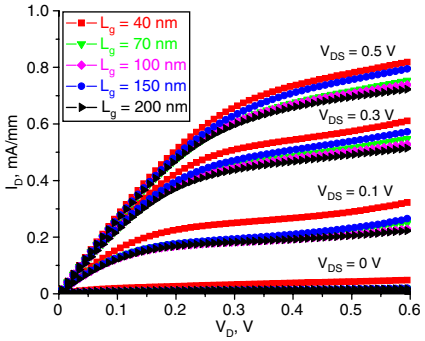

Fig. 1 *Output characteristics of fabricated InGaAs HEMTs with various gate lengths*

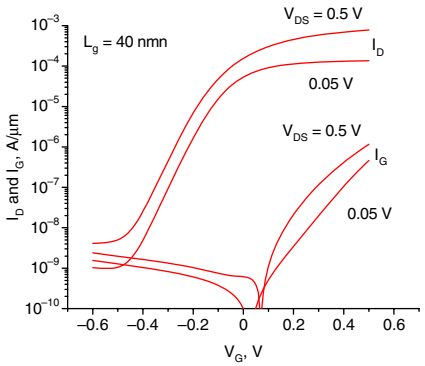

Fig. 2 *Subthreshold and gate current characteristics of 40 nm InGaAs HEMT at $V_{DS} = 50$ mV and $V_{DS} = 0.5$ V*

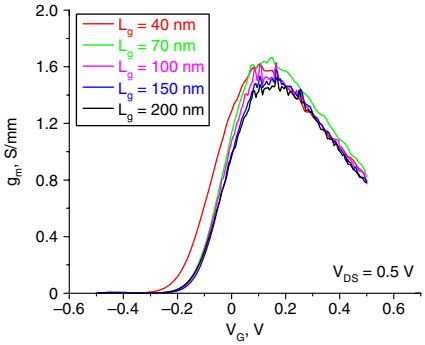

Fig. 3 *Transconductance characteristics of HEMTs with various gate lengths from 40 to 200 nm at $V_{DS} = 0.5$ V*

We have extracted the source resistance by means of the gate current injection technique [8]. The extracted R_s is 170 Ω-μm. From TLM measurements, we have extracted a contact resistance to the heavily-doped cap of 30 Ω-μm. This is identical to a recent value obtained using the same ohmic technology in a different heterostructure [6].

Microwave performance was characterised from 0.5 to 40 GHz. On-wafer open and short patterns were used to subtract pad capacitances and inductance from the measured device S-parameters. Fig. 4 plots current gain (H_{21}), MAG/MSG and unilateral gain (U_g), as well as the stability factor (K), against frequency, for the best bias conditions at $V_{GS} = 0.4$ V and $V_{DS} = 0.7$ V for an $L_g = 40$ nm device. Values of $f_T = 530$ GHz and $f_{max} = 445$ GHz have been obtained by extrapolation.

Our results compare well with earlier reports. Our R_s improves on a previously reported best value of 232 Ω-μm in a similar heterostructure with a lattice matched barrier and $L_{side} = 200$ nm [7]. The lower R_s reported here comes partly from the shorter L_{side} but also from the new spacer design. This is particularly the case because the heterostructures in [7] include a 5 nm-thick InAs subchannel that confers the channel with an outstanding mobility (13200 cm^2/V.s. A consequence of the reduced R_s is an improved transconductance in $L_g = 40$ nm

devices from 1.5 mS/μm in [7] to 1.6 mS/μm here. In terms of f_T, the results also improve on those in [7] where an $f_T = 390$ GHz was obtained at $V_{DS} = 0.5$ V on $L_g = 40$ nm devices.

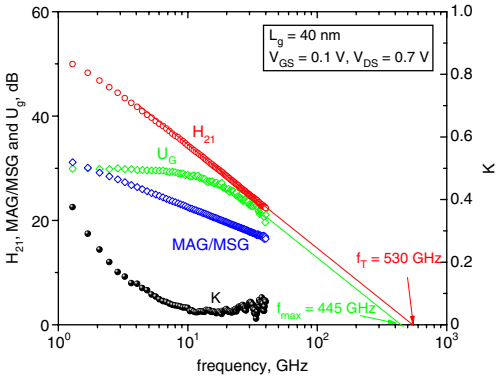

Fig. 4 *Microwave characteristics of 40 nm InGaAs HEMT at $V_{GS} = 0.1$ V and $V_{DS} = 0.7$ V. An $f_T = 530$ GHz and $f_{max} = 445$ GHz are extracted*

Conclusion: We have demonstrated a 40 nm InGaAs HEMT with an InAs-rich spacer in the InAlAs barrier to reduce the source resistance. The device shows excellent saturation characteristics, a low $R_{ON} = 350\ \Omega$-μm, as well as a transconductance of 1.6 S/mm at $V_{DS} = 0.5$ V. The source resistance is 170 Ω-μm. From the subthreshold characteristics, we have also obtained $S = 80$ mV/dec, DIBL = 122 mV/V and $I_{ON}/I_{OFF} = 3 \times 10^4$ at $V_{DS} = 0.5$ V. The proposed design in combination with a self-aligned ohmic contact technology has potential for reducing the parasitics of deeply scaled devices and substantially enhances their frequency response.

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One or more of the Figures in this Letter are available in colour online.

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