f_T = 688 GHz and f_{max} = 800 GHz in L_g = 40 nm $In_{0.7}Ga_{0.3}As$ MHEMTs with g_{m_max} > 2.7 mS/μm

D.-H. Kim, B. Brar and *J. A. del Alamo,

*Teledyne Scientific Company, *MIT*

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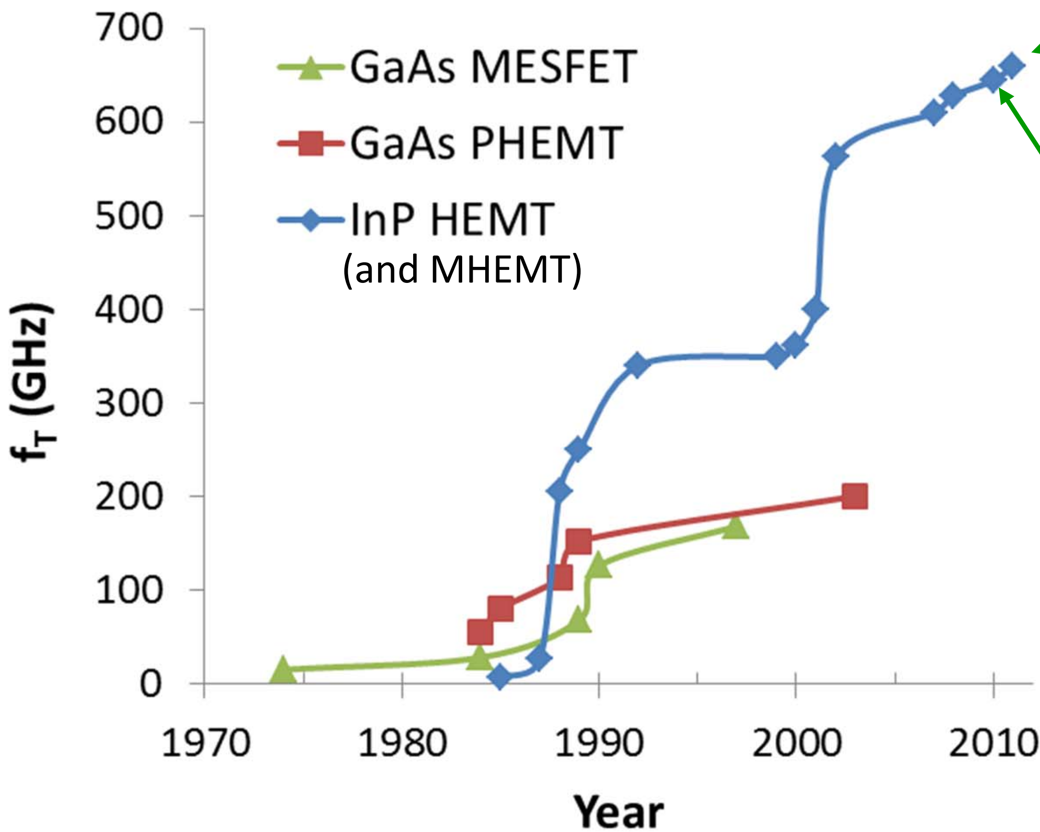
IEDM

December-6th, 2011

III-V HEMT: record f_T vs. time



Current record:
f_t=660 GHz
Leuther IPRM 2011
(Fraunhofer Inst.)

Well balanced devices:
f_t=644 GHz, f_{max}=680 GHz
at same bias point
Kim EDL 2010
(MIT)

For >20 years, record f_T obtained on InGaAs-channel HEMTs.

InGaAs-channel HEMTs offers record balanced f_T and f_{max}.

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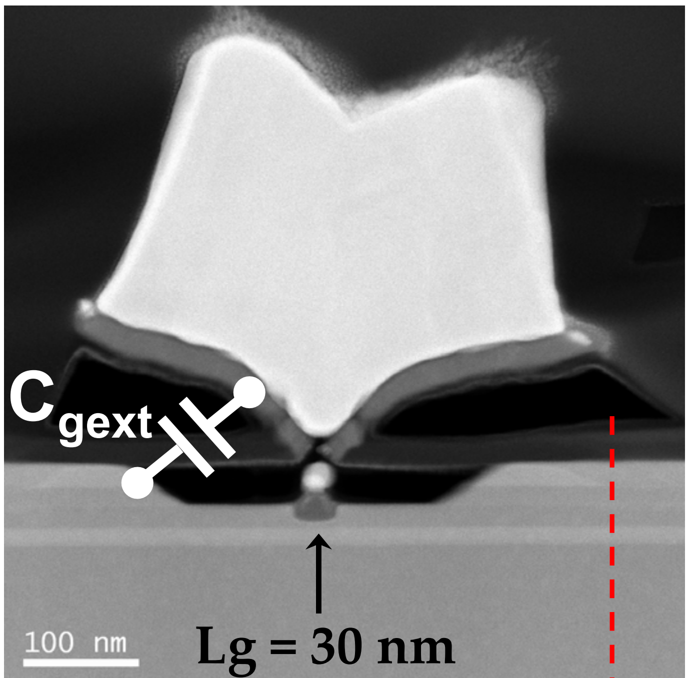
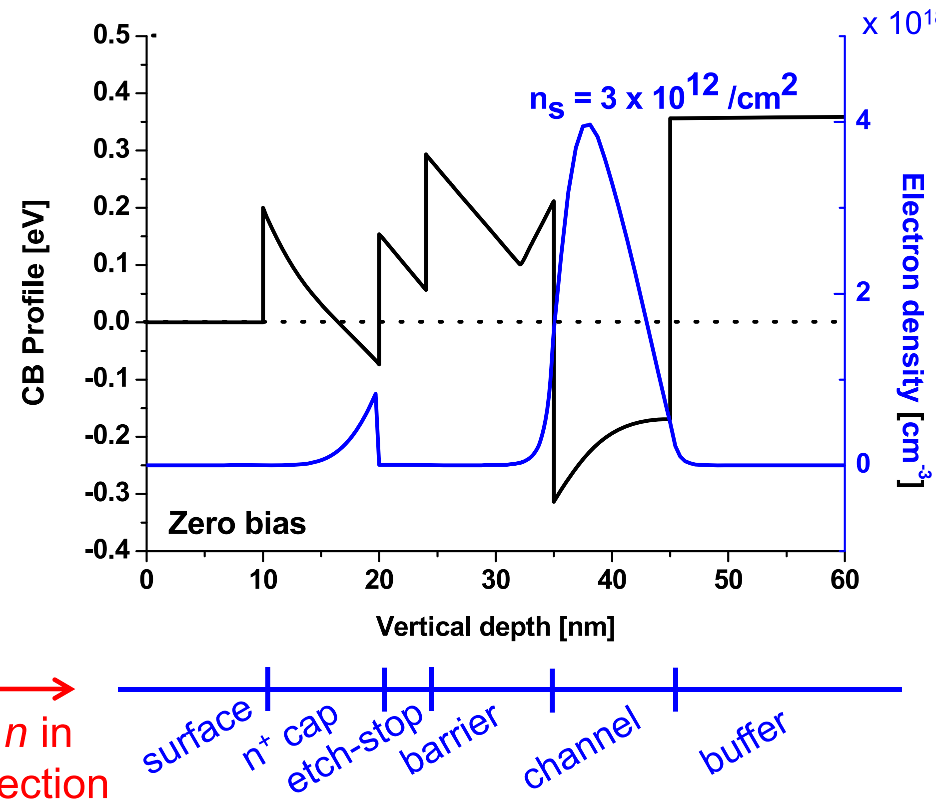
Strategy to improve f_T

- In typical HEMTs:
  - R_{ON}: 350 ~ 450 Ω-μm
  - T-Gate: Stem height = ~ 150 nm



R_{ON} ~ 420 Ohm-μm

E_C and n in cross section



Kim, EDL 2008

Contents

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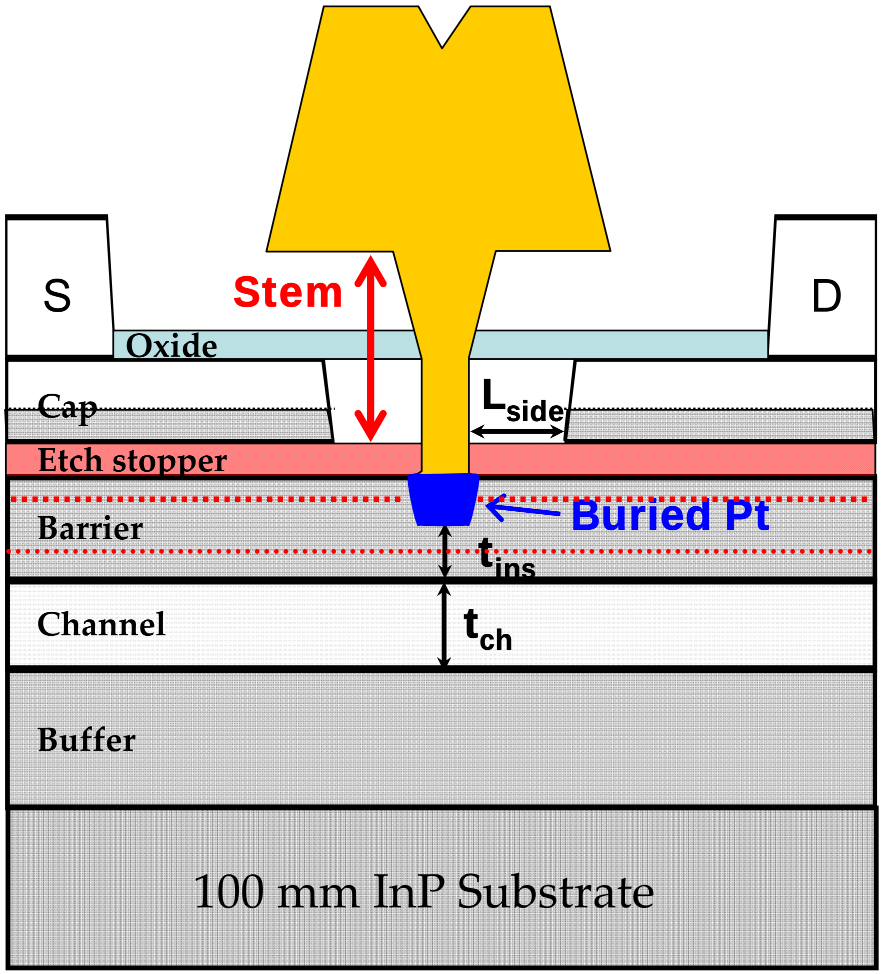
Device Technology



- SiO_2 assisted T-gate
  - → **L_g = 40 nm**
  - → **Gate-stem > 250 nm**
- Two-step recess (InP = 6 nm)
- **Pt (3 nm)**/Ti/Pt/Au Schottky
- QW: 10 nm $In_{0.7}Ga_{0.3}As$
  - → $\mu_{n,Hall}$ > 10,000 cm^2/V-s
- *$In_{0.52}Al_{0.48}As$/**$In_{0.7}Al_{0.3}As$** spacer
- ****Dual Si δ-doping**

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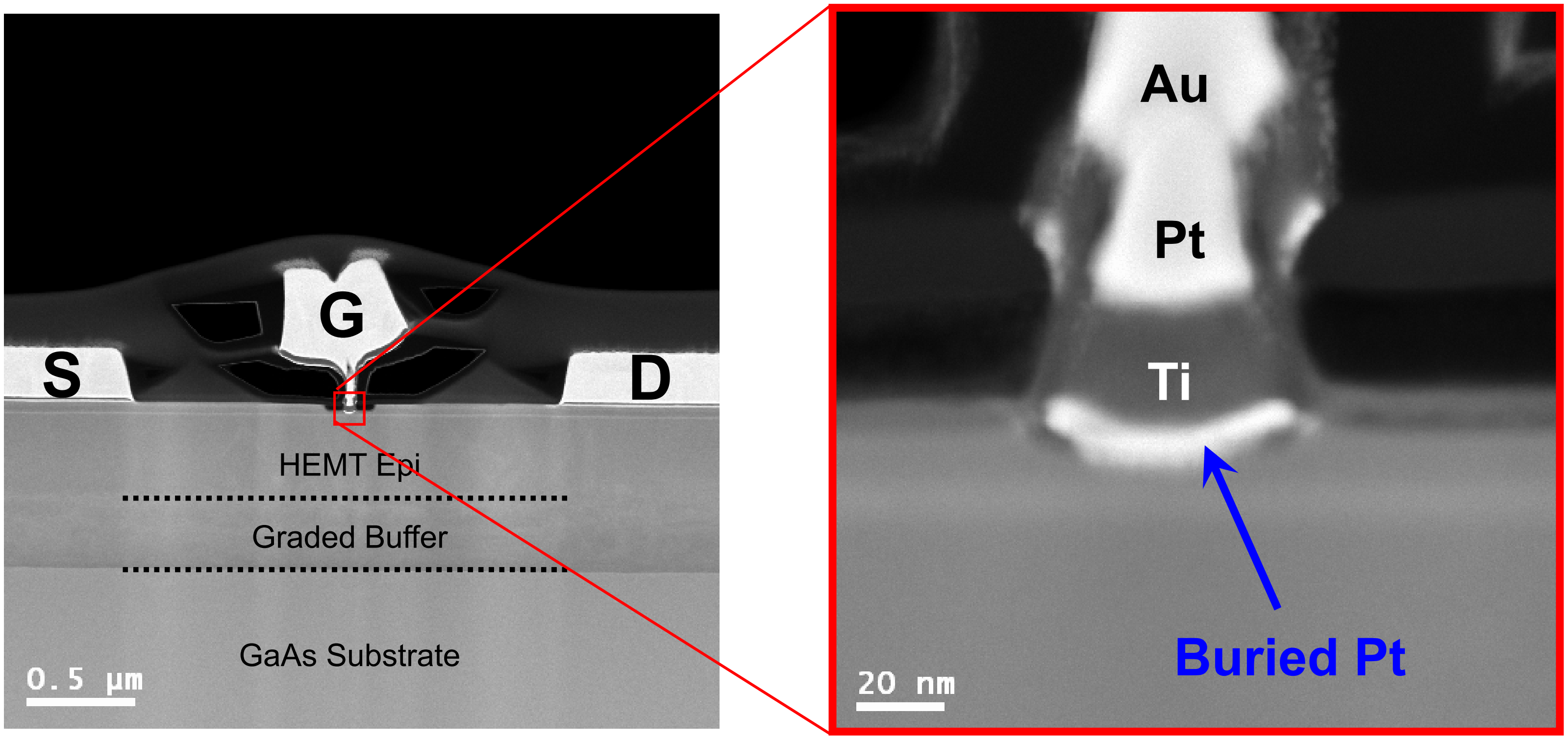
KIM, *Electron Lett 2011 ** IEDM 2010

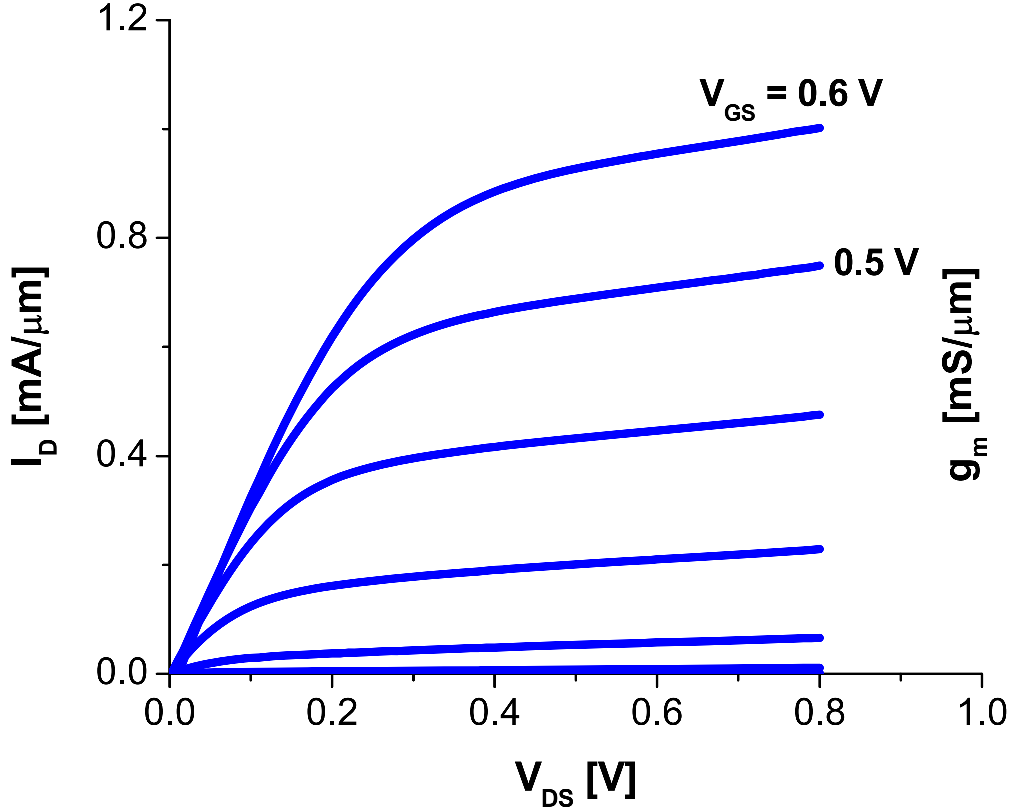
TEM Images



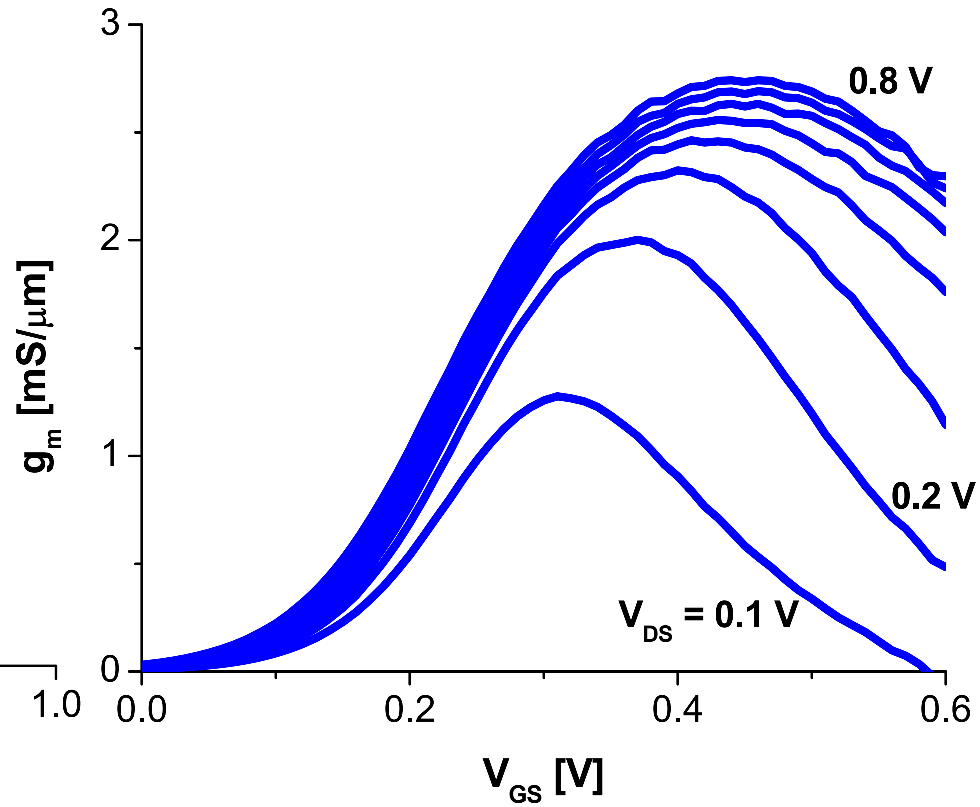
- Mo-based S/D with 2 μm
- Gate Stem > 250 nm
- L_g = 40 nm, L_{side} = 100 nm
- t_{ins} = ~ 4 nm

DC of L_g = 40 nm InGaAs MHEMTs

- Output characteristics -



- g_m characteristics -



- Maximum I_D > 1 mA/µm
- **R_{ON} = 280 Ω-µm**

- g_m > 2 mS/µm @ V_{DS} = 0.3 V
- **g_{m_max} = 2.75 mS/µm** @ V_{DS} = 0.8 V

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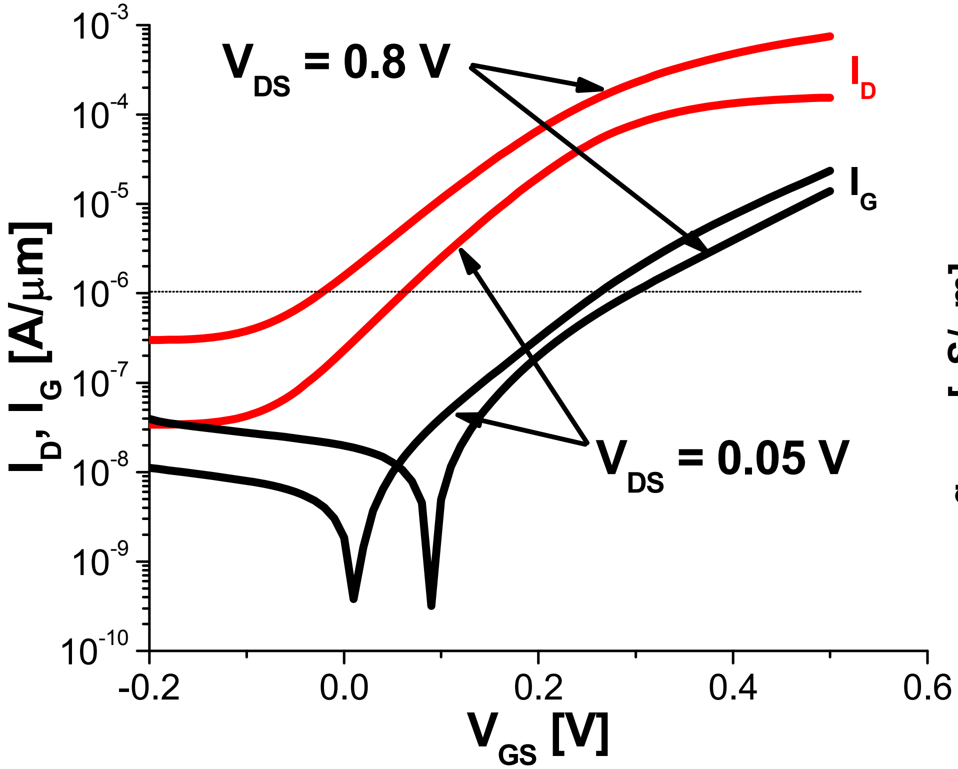
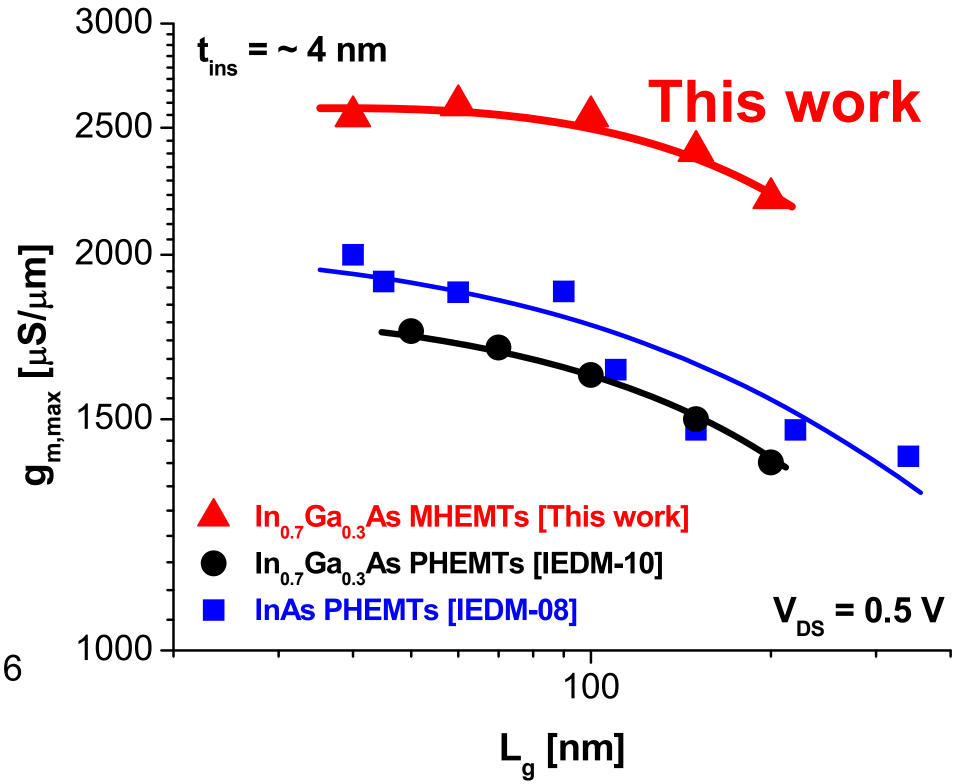
Subthreshold characteristics

- L_g = 40 nm -



- g_{m_max} scalability-



- V_T = 0.02 V @ V_{DS} = 0.5 V
- S = 100 mV/dec., DIBL = 105 mV/V

As $L_g \downarrow$,
$\rightarrow g_m$ saturates.

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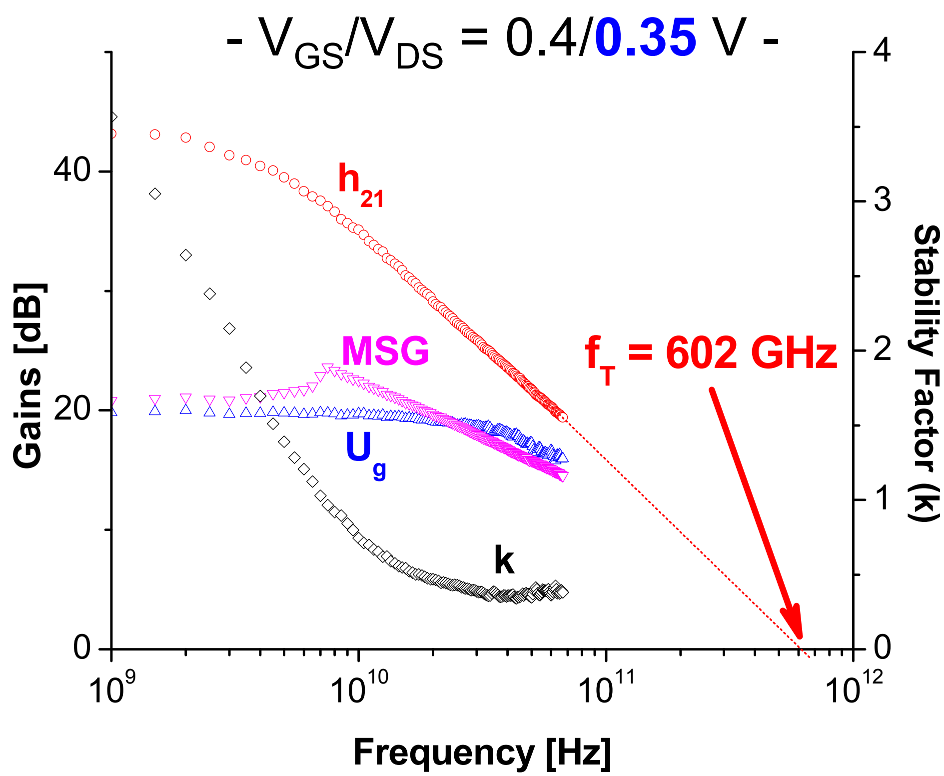
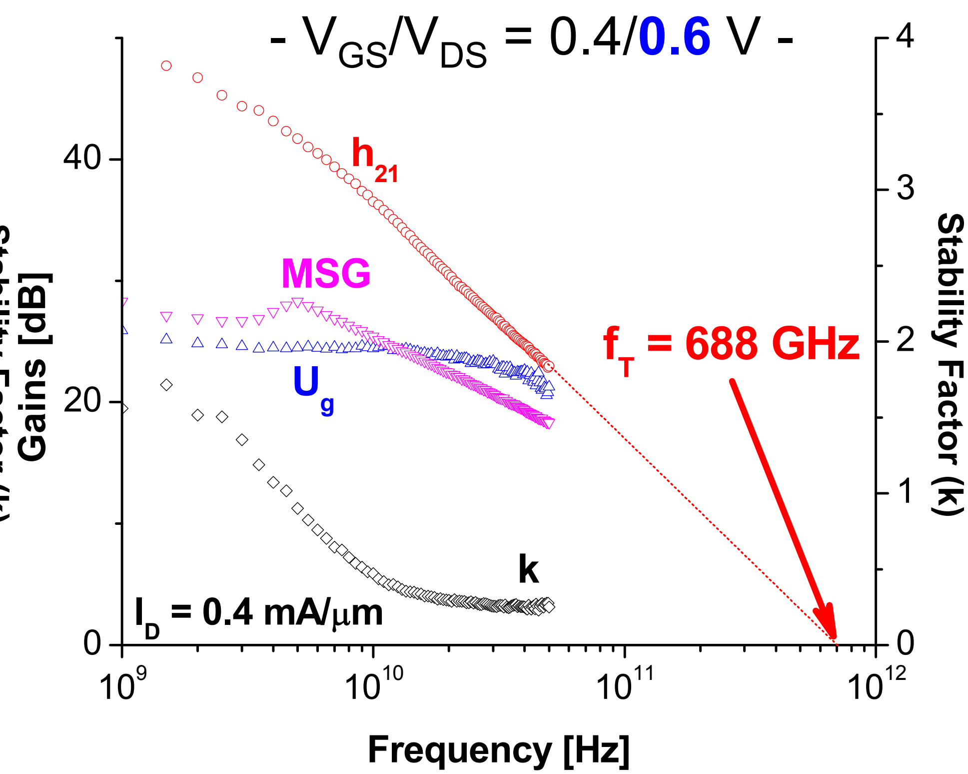
f_T & f_{max}: L_g = 40 nm, W_g = 2 x 20 μm

Calibration: LRRM, De-embedding: OPEN/SHORT





- f_T already approaches to 600 GHz @ V_{DS} = 0.35 V.
- **Record f_T = 688 GHz** @ V_{DS} = 0.6 V.

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Gummel technique for f_T extraction

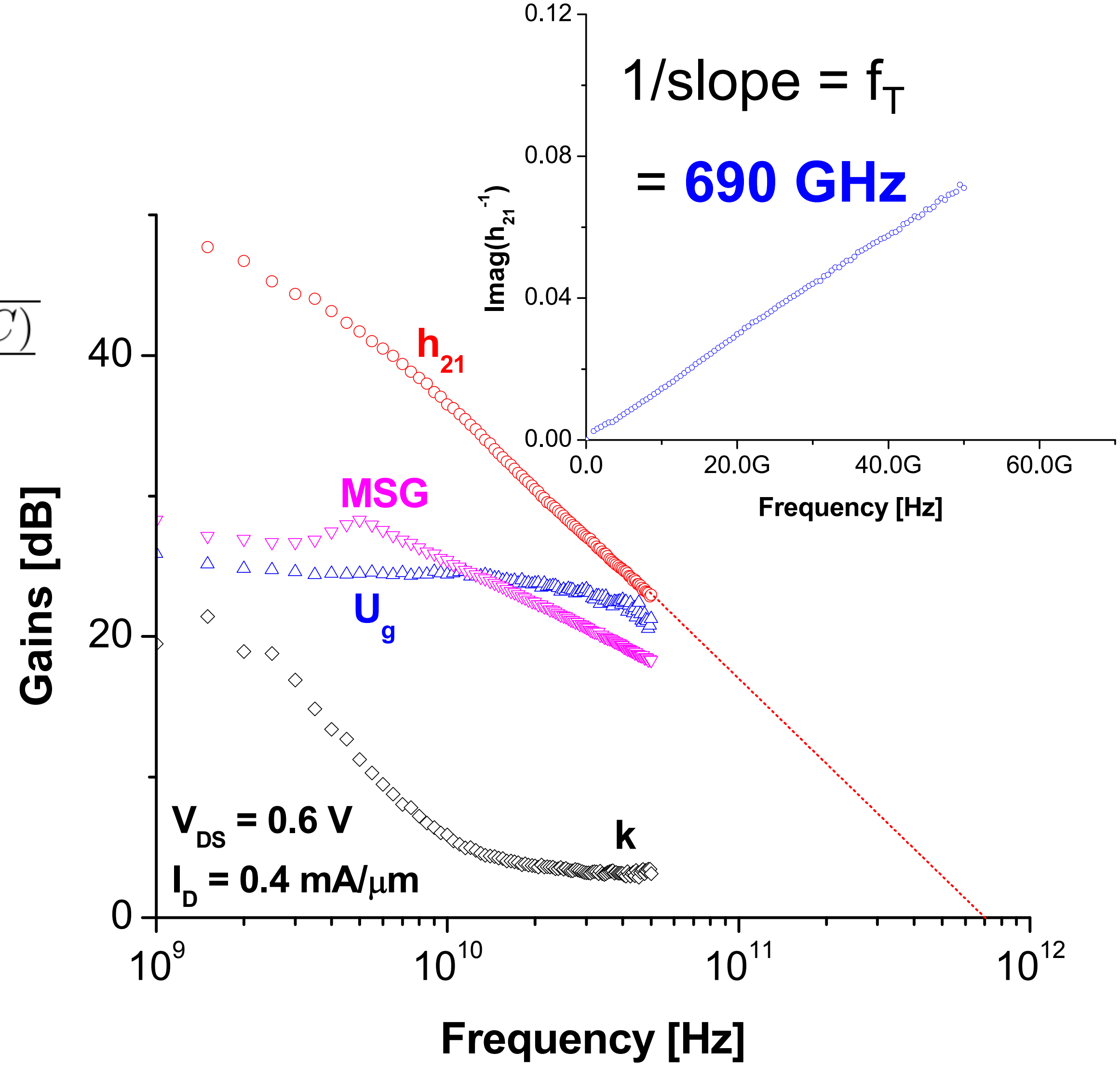
In one-pole system:

$$h_{21}(f) = \frac{h_{21}(DC)}{1 + jf\frac{h_{21}(DC)}{f_T}}$$

Then:

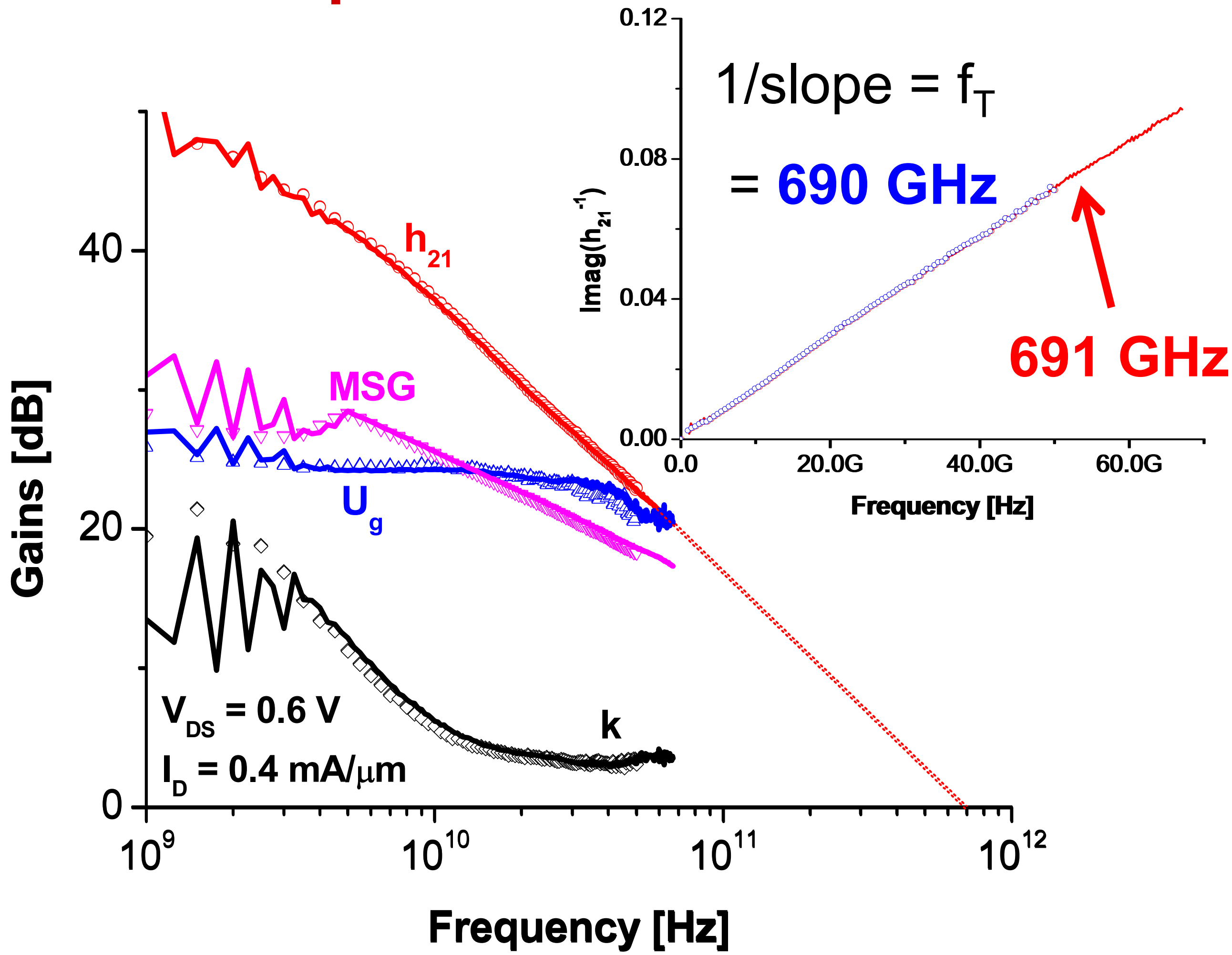
$$Im[\frac{1}{h_{21}(f)}] = \frac{f}{f_T}$$

Slope gives f_T



Gummel, Proc IEEE 1969

Different measurement system for f_T extraction



- 8510C @TSC: 1 ~ 50 GHz
- **PNA @UCSB: 1 ~ 67 GHz**

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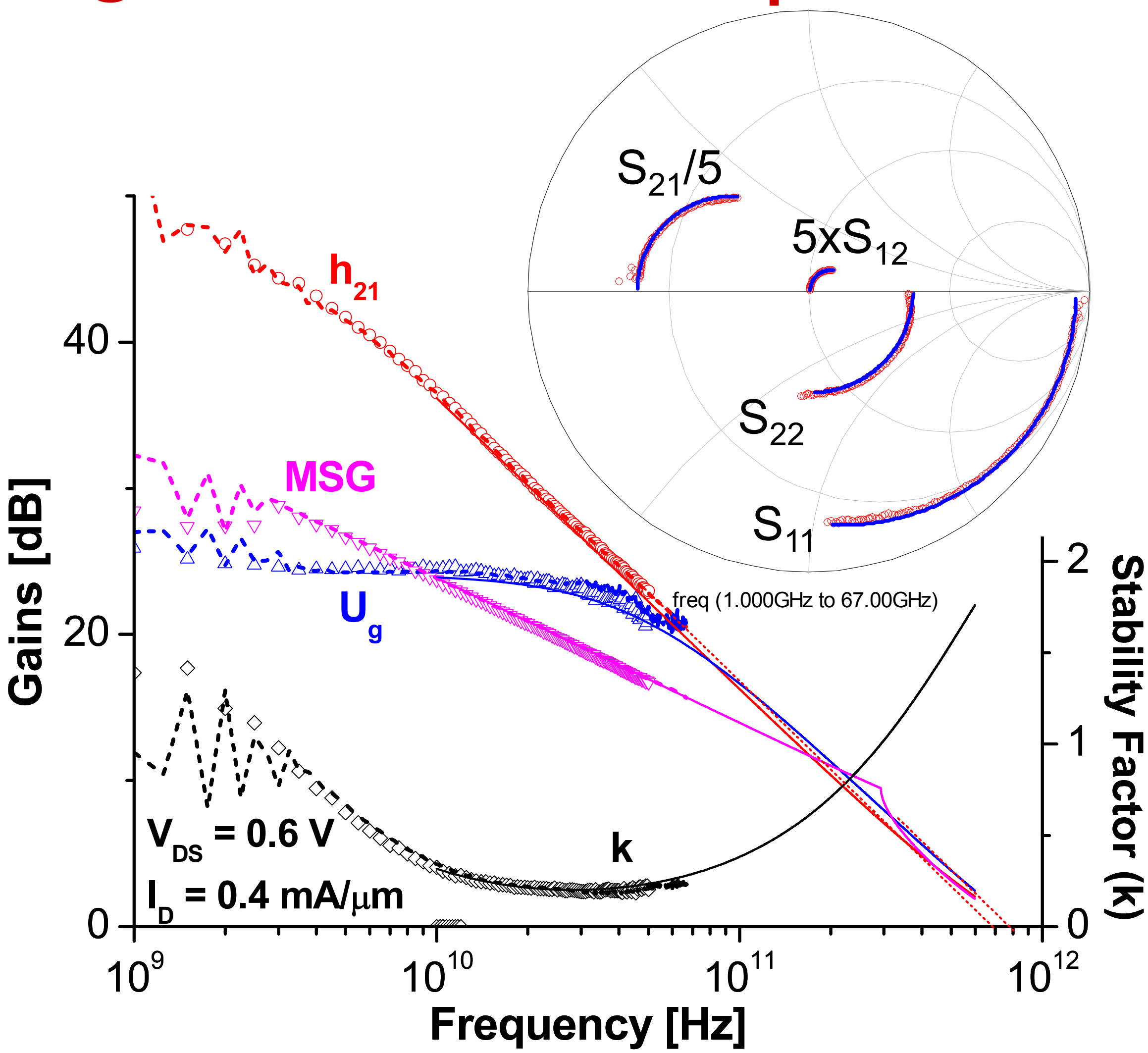
Small-signal model for f_T extraction



- **Excellent agreement**, modeled f_T = 680 GHz
  f_{max} = 800 GHz

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Summary on f_T measurements

Measurements in two different test benches:

		8510C @TSC	PNA @UCSB
f_T [GHz]	From H_{21}	**688**	**688**
	From Gummel's approach	**690**	**691**
	From Small-signal model	**680**	
f_{max} [GHz]		**800**	

All measurements at same bias point: V_{GS}=0.4 V, V_{DS}=0.6 V

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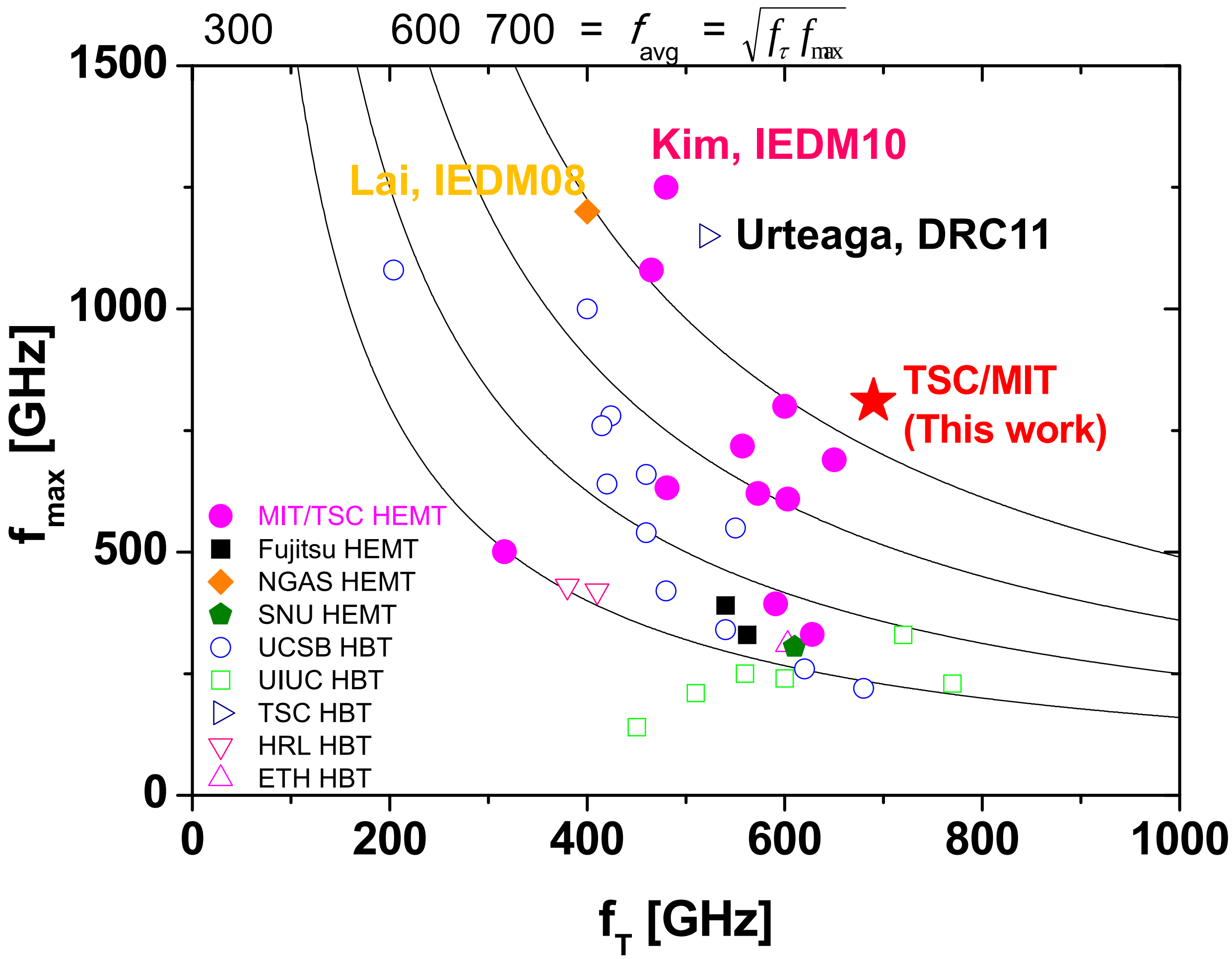
Kim, EDL 2010

Balance in f_T and f_{max}



→ Record f_T FET

→ Best-balanced f_T and f_{max} transistor

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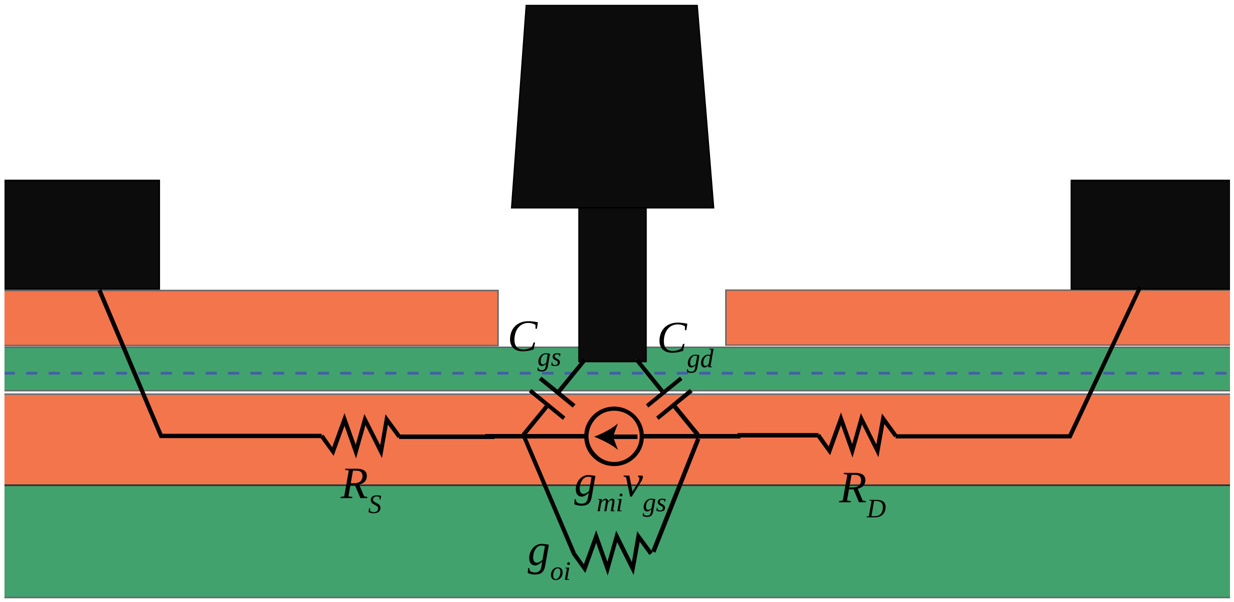
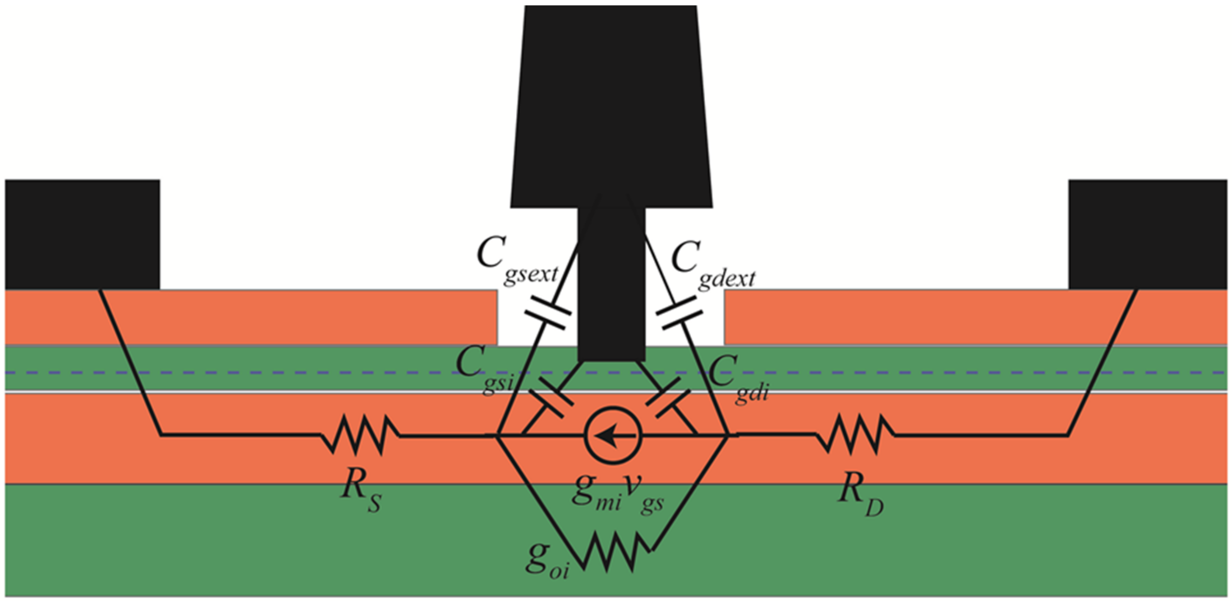
Analytical f_T Model



- First-order f_T expression for HEMT:

$$f_T = \frac{1}{2\pi} \frac{g_{mi}}{C_{gs} + C_{gd} + g_{mi}(R_S + R_D)[C_{gd} + (C_{gs} + C_{gd})\frac{g_{oi}}{g_{mi}}]}$$

Break out 'extrinsic' capacitances



- Capacitance components [fF/mm]:

$$C_{gs} = C_{gsi} + C_{gsext} = C_{gsi\_areal} \times L_g + C_{gsext}$$

C_{gsi_areal}: [fF/μm²]

$$C_{gd} = C_{gdi} + C_{gdext} = C_{gdi\_areal} \times L_g + C_{gdext}$$

C_{gdi_areal}: [fF/μm²]

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Delay time analysis

- Delay time:

$$\tau = \frac{1}{2\pi f_T} = \tau_t + \tau_{ext} + \tau_{par}$$

- Components of delay time:

Intrinsic delay (transit time)

$$\tau_t = \frac{C_{gsi} + C_{gdi}}{g_{mi}} = \frac{(C_{gsi\_areal} + C_{gdi\_areal})L_g}{g_{mi}} = \frac{L_g}{v_e}$$

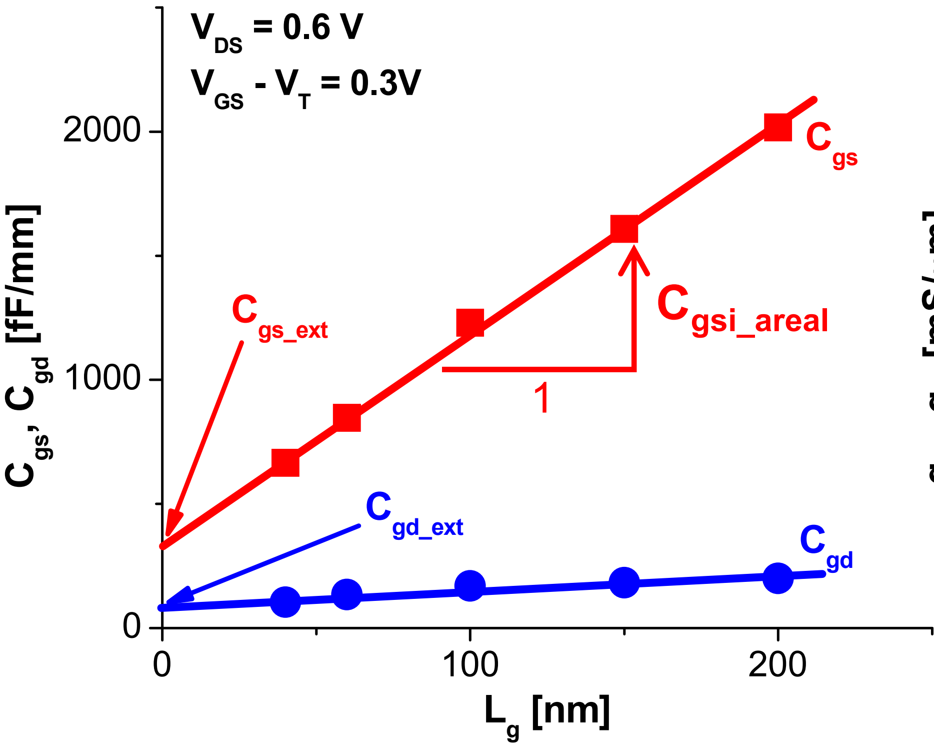
Extrinsic delay

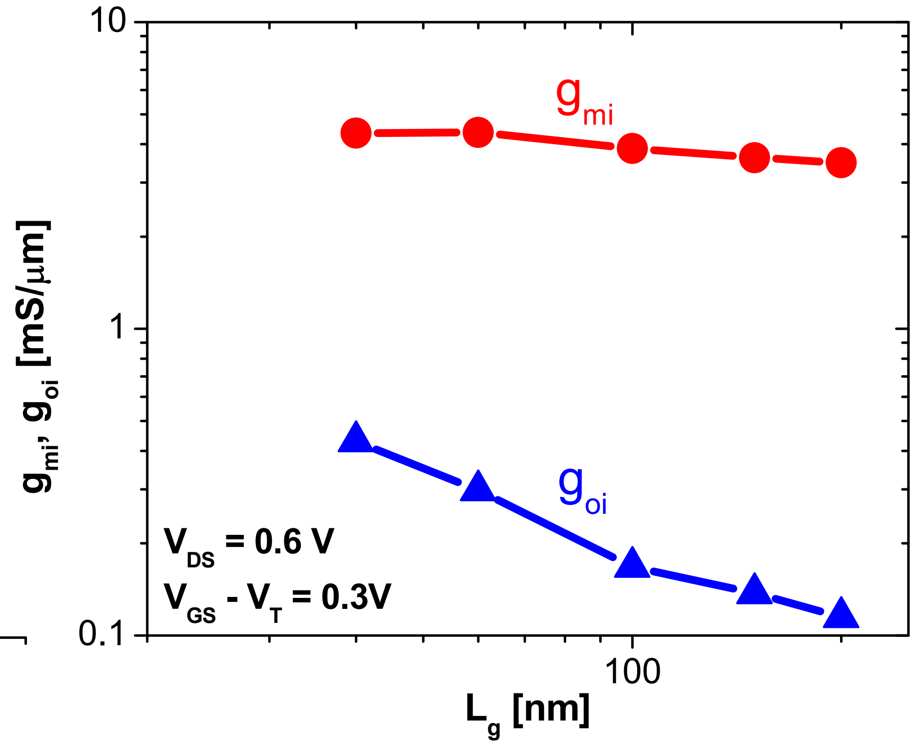
$$\tau_{ext} = \frac{C_{gsext} + C_{gdext}}{g_{mi}}$$

Parasitic delay

$$\tau_{par} = (R_S + R_D)[C_{gd} + (C_{gs} + C_{gd})\frac{g_{oi}}{g_{mi}}]$$

L_g-dependent model parameters





- Linearly proportional to L_g
- $C_{gs\_ext} > C_{gd\_ext}$

  ← $|V_{gs}| < |V_{gd}|$

As L_g↓,

- g_{mi} saturates at L_g = ~ 60 nm
- g_{oi} continues to increase

  → g_{mi}/g_{oi} ↓

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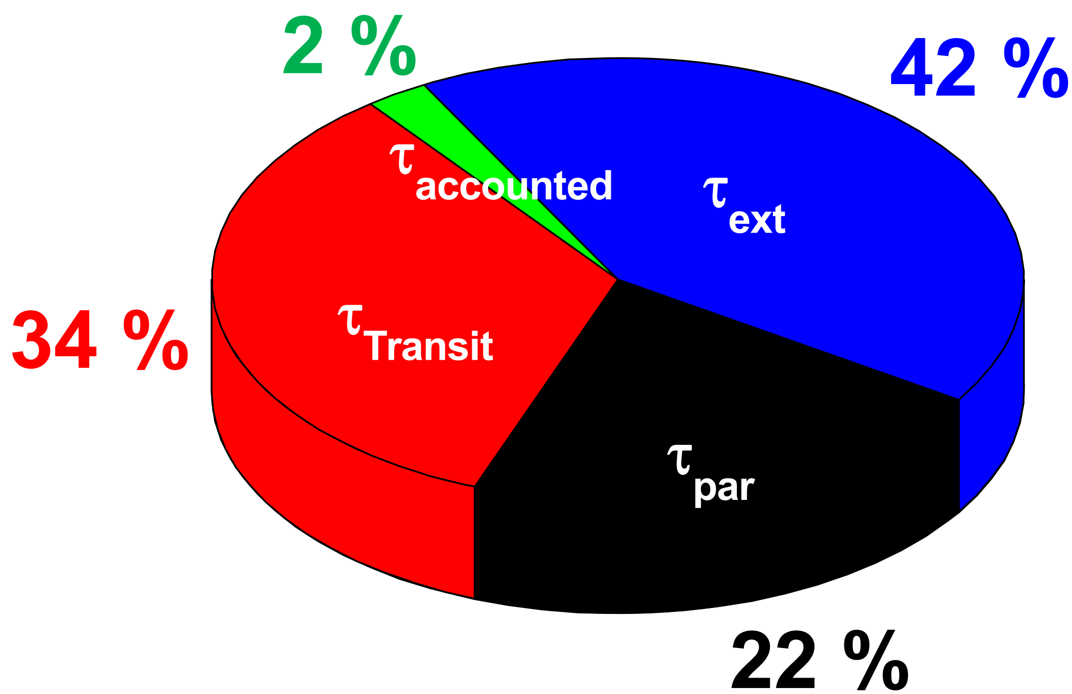
Delay components of L_g=40 nm InGaAs MHEMT

Delay time from f_t: ~231 fs

- Intrinsic delay: ~81 fs
- Extrinsic delay: ~ 99 fs
- Parasitic delay: ~50 fs
- Unaccounted: ~9 fs

least significant, yields v_e=5 x10^7 cm/s

most significant



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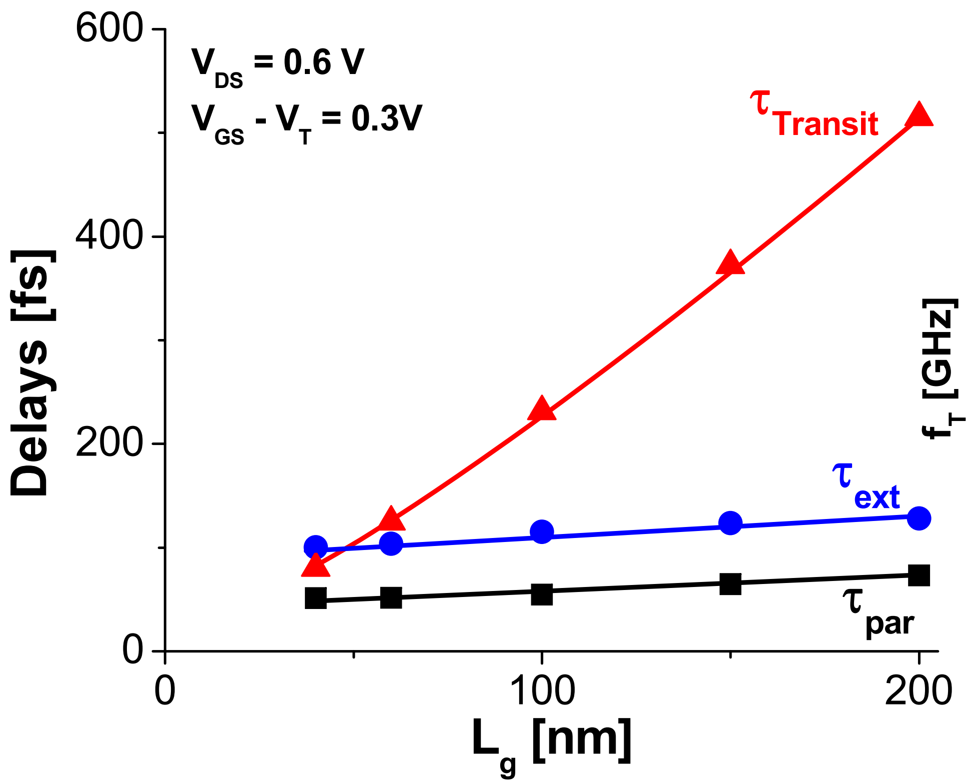
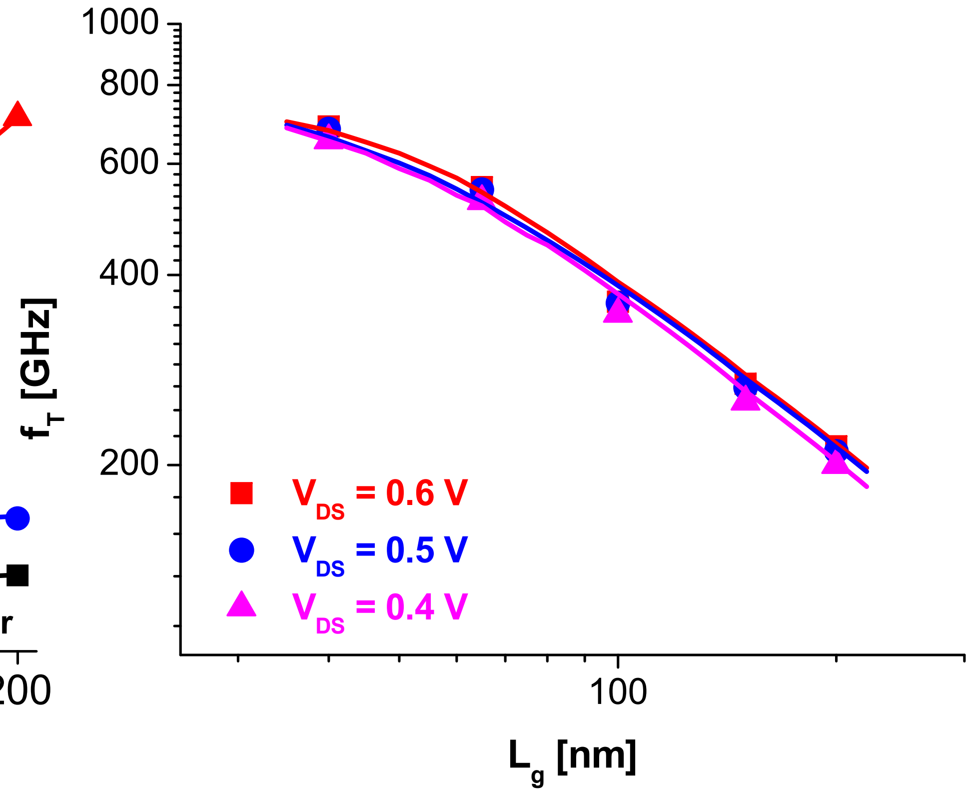
Scaling of delay components





τ_{ext} and τ_{par} do not scale, become dominant for L_g < ~ 60 nm.

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Options to improve f_T

- Intrinsic delay:

$$\tau_t = \frac{C_{gsi} + C_{gdi}}{g_{mi}} = \frac{L_g}{v_e}$$

$L_g \downarrow$ (without degrading g_{mi}), $v_e \uparrow$ → channel engineering

- Extrinsic delay:

$$\tau_{ext} = \frac{C_{gsext} + C_{gdext}}{g_{mi}}$$

C_{gsext}, $C_{gdext} \downarrow$, or alternatively $g_{mi} \uparrow$ (harmonious scaling)

- Parasitic delay:

$$\tau_{par} = (R_S + R_D)[C_{gd} + (C_{gs} + C_{gd})\frac{g_{oi}}{g_{mi}}]$$

R_S+$R_D \downarrow$, increase electrostatic integrity: $g_{oi}/g_{mi}\downarrow$

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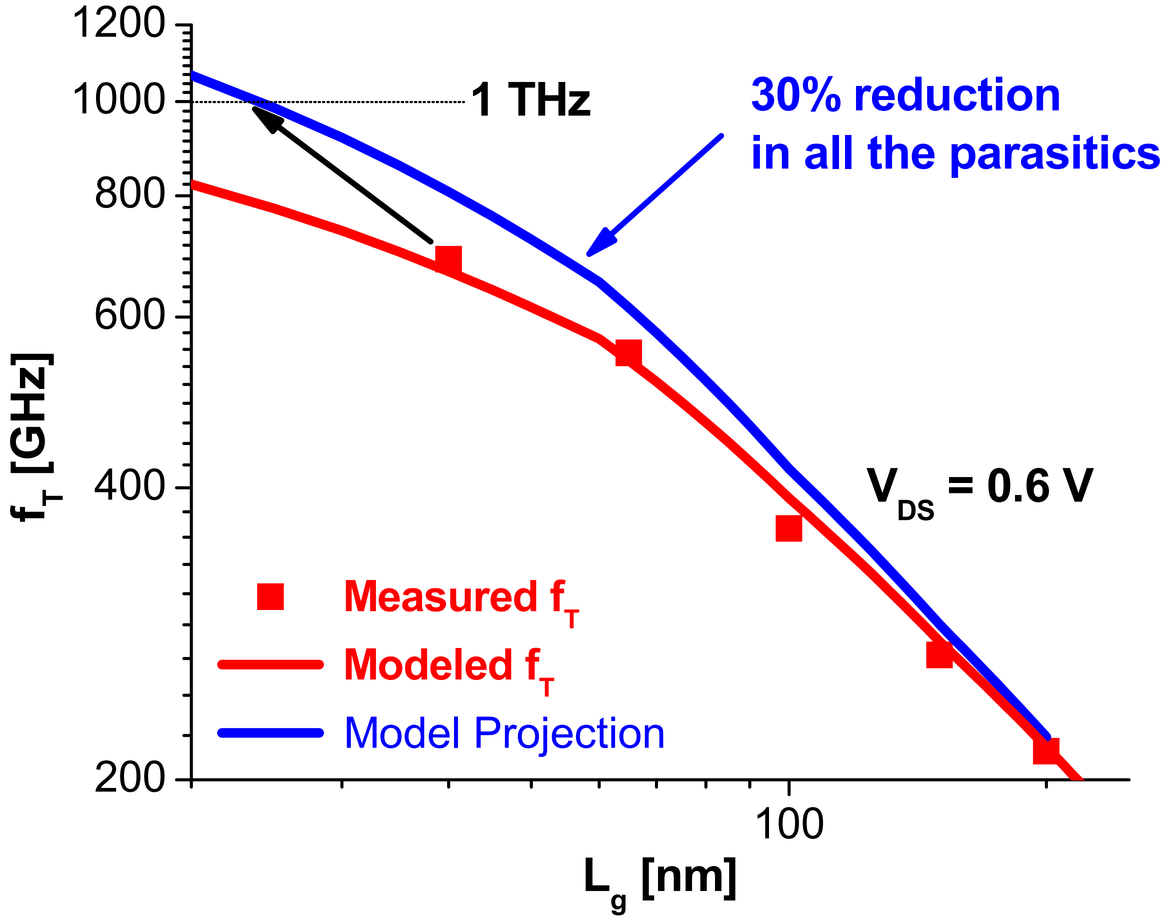
Model Projection



f_T = 1 THz is *feasible* at L_g = ~ 25 nm.

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Summary

40-nm $In_{0.7}Ga_{0.3}As$ MHEMTs on GaAs substrate

- R_{ON} = 280 Ω-μm, **g_{m_max} > 2.7 mS/μm** @ V_{DS} = 0.8 V
- S = 100 mV/dec., DIBL = 105 mV/V
- Measured **f_T = 688 GHz** (**Record** in any FET)
- f_T/f_{max} = 688/800 GHz (**Best-balanced** transistor)

Analytical f_T Model

- Excellent description of f_T behavior in III-V HEMTs
- Guidance to improve f_T beyond 1 THz

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