Performance Enhancement of P-channel InGaAs Quantum-well FETs by Superposition of Process-induced Uniaxial Strain and Epitaxially-grown Biaxial Strain

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Abstracts

We have developed a device architecture for p-channel InGaAs quantum-well field-effect transistors (QW-FETs) that incorporates uniaxial strain through a self-aligned dielectric stressor. For the first time, we demonstrate substantial enhancement in the transport characteristics of p-channel InGaAs QW-FETs through the combination of compressive uniaxial strain and compressive epitaxially grown biaxial strain. Up to 36% increase of intrinsic transconductance has been observed in devices with 2 μm gate length.

Introduction

Recently, InGaAs-channel n-type field-effect transistors (FETs) have attracted a great deal of interest for future sub-10 nm CMOS applications as a result of the more than 2x electron velocity over Si [1]. Promising InGaAs n-MOSFET results have already been demonstrated [2]. In the quest for an all InGaAs-based complementary logic technology, realizing a high performance p-channel InGaAs FET remains a great challenge. The key problem is the relatively small hole mobility (μ_h) of InGaAs which is of the same order as in Si.

A feasible way to improve hole mobility is through the application of uniaxial strain to the channel material. This approach has been widely adopted in Si p-MOSFETs. [3] Uniaxial strain has also been found to enhance hole mobility in III-V quantum wells. [4, 5] Recent studies suggest that by combining uniaxial strain and biaxial strain, effective mass (m^*) and μ_h in InGaAs quantum wells can be significantly enhanced, even more so than in Si. [6] Such an effect has also been observed in Ge p-MOSFETs. [7] To fully explore the potential of this new concept for improving the performance of p-channel InGaAs FETs, we have fabricated devices through a process that incorporates uniaxial strain on a heterostructure with the channel under biaxial strain.

Fabrication Process

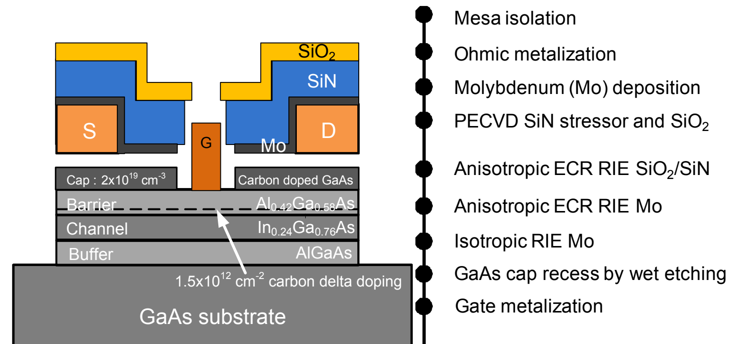

Fig. 1 (Left) P-channel InGaAs FET with built-in stressors. A refractory contact metal layer and SiN stressor are both self-aligned to the gate edge. High- (-2.1 GPa) and zero-stress SiN films were used for comparison. (Right) Fabrication process flow for the p-channel InGaAs QW-FET.

Fig. 1 shows the design of our p-channel QW-FET and the process flow. The starting MBE-grown modulation-doped heterostructure features a 9 nm thick $In_{0.24}Ga_{0.76}As$ channel grown on (100) GaAs with -1.7% compressive biaxial strain. $Al_{0.42}Ga_{0.58}As$ is used as the barrier material. Uniaxial strain is introduced through a compressively-strained SiN layer by PECVD. An opening is made in this film to accommodate the gate in a self-aligned way. In this way, the film exerts compressive stress in the semiconductor underneath the gap near the film edge. Below the SiN layer, a Mo film is introduced to prevent p-type dopant (carbon) passivation [8] during PECVD. With better metal selection, this metal film could behave as a self-aligned ohmic contact to the transistor. Above the SiN stressor, a SiO_2 layer is used to prevent shorting between the gate metal and the Mo layer. In our process, the Mo and SiN are pulled back from the gate edge in a self-aligned way through an isotropic RIE step. [9, 10] This allows the stressor to be placed in close proximity to the FET channel and introduce large strain. For comparison, two types of SiN were used with -2.1 GPa and nearly zero compressive stress. Devices with transport directions along [-110], [011], [010] and [100] were fabricated on the same heterostructure and were processed at the same time. Gate lengths, L_G, range from 2 to 8 μm.

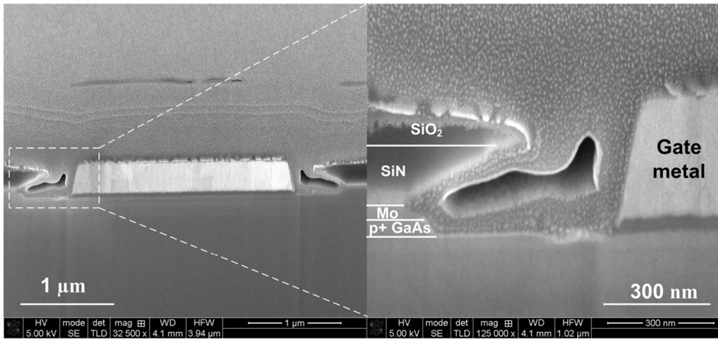

Fig. 2. (Left) Cross-section SEM of a p-channel QW-FET with L_G = 2 µm, [-110] channel and SiN stress of -2.1 GPa. (Right) Zoom-in SEM of the left gate edge area.

Fig. 2 shows a cross-section SEM example of a processed FET. After the gate recess process, the distance between the gate and the GaAs cap is found to be ~400 nm. This distance can be shrunk by reducing the process time of the isotropic SiN and Mo RIE. No side etch of the GaAs cap under the Mo layer is observed. This feature is useful for future self-aligned ohmic metal contact.

Mechanical Simulations

The stress distribution in our target structure was studied by 3D mechanical simulations. The simulated structure is similar to that of **Fig. 1**. A 200-nm SiN layer is placed on top of a GaAs cap. A side recess of 100 nm on the GaAs cap was used for the simulations. The SiN layer is under -2 GPa compressive biaxial intrinsic stress. The simulations calculate 3D distributions of all stress components. The most important two are along the channel direction and along the gate width direction. The simulations (**Fig. 3**) reveal that stress peaks at the edge of the recessed cap. This is better seen in **Fig.4**, which shows stress distribution in a 2 um recessed structure along the channel direction. Uniaxial longitudinal stress peaks at the edges of the cap and it drops towards the middle of the gap. Uniaxial transversal stress is 2-3 times smaller and has an opposite sign (tensile). The fact that the transverse stress is tensile is desirable, as the negative transverse piezoresistance coefficient of InGaAs [6] yields an additional μ_h enhancement.

Fig. 5 shows the simulated values for longitudinal and transverse stress taken at the center of the recessed gap ("center stress") as a function of L_G. The longitudinal center stress increases markedly with decreasing L_G. There are three regimes of stress sensitivity to L_G, determined by the relative dimensions of L_G, side recess length and stressor thickness. The first regime is with L_G much larger than stressor thickness in which stress increases slowly with decreasing L_G. The second regime is with L_G comparable to the stressor thickness in which the center stress increases

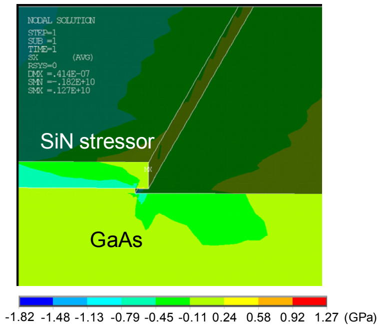

Fig. 3. Spatial distribution of stress along gate length direction by 3D finite-element mechanical simulations. A side-recessing distance of 100 nm for GaAs cap was considered in the simulations.

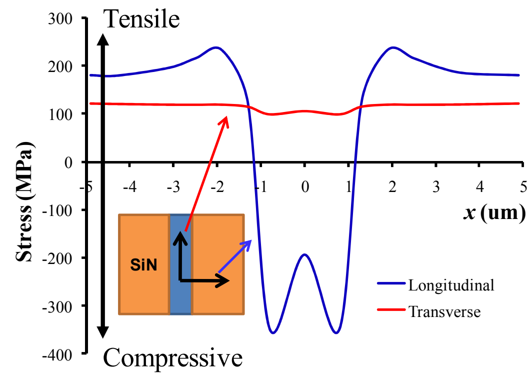

Fig. 4. Simulated longitudinal and transversal surface stress across a 2-µm recess opening, created by a 200 nm thick SiN with -2 GPa stress.

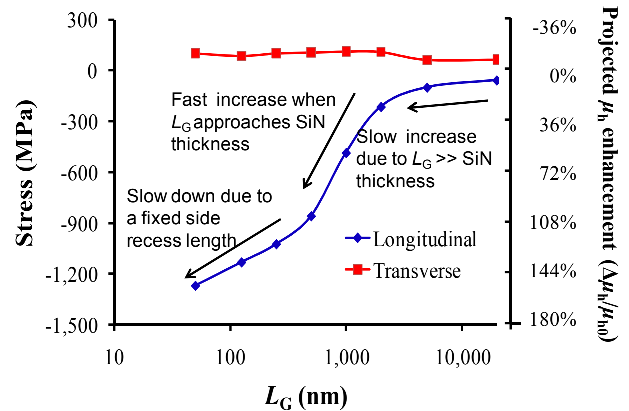

Fig. 5. Longitudinal and transverse center stress scaling with L_G and projected μ_h enhancement. The center stress was simulated following the structure in Fig. 1. The μ_h enhancement was projected assuming that μ_h is linearly proportional to stress and using the piezoresistance coefficients in [6].

sharply with decreasing L_G. The third regime is with L_G comparable to the side-recess length in which stress enhancement with scaling slows down. The p-channel QW-FETs in this work fall in the first regime due to L_G being much larger than the SiN thickness. The maximum center stress expected in our 2 µm device with a 100 nm side recess length is around -220 MPa. As L_G scales down to the sub-50 nm range, up to -1.2 GPa stress is expected in the FET.

Assuming a linear relationship between stress and mobility enhancement, a greater than 160% enhancement in μ_h is expected as devices scale down to L_G < 50 nm [6]. Greater enhancements are possible with stressor structure optimization.

Experimental Results

In the fabricated devices, significant improvements in device performance were found when uniaxial strain was introduced through the SiN stressor. **Fig. 6** compares the output characteristics of two devices with high- and zero-stress SiN, with L_G = 2 μm and channel along [-110]. A significant increase in the drain current is observed. **Fig. 7** shows the subthreshold characteristics of the two devices. They both have similar gate current characteristics and subthreshold swing. These characteristics are also similar to devices fabricated without RIE process which rules out any RIE-induced damage. A threshold voltage shift was observed between the two devices. This is possibly caused by a slight difference in the final AlGaAs barrier thicknesses possibly originating in a thickness difference between the stressed and unstressed SiN layers.

Performance improvements were also clearly observed in the transconductance (**Fig. 8**). The intrinsic transconductance (g_{mi}) was extracted from the extrinsic transconductance (g_{mext}) using output conductance and source/drain resistance (R_S/R_D) measured by the gate current injection method [11, 12]. R_S and R_D are also significantly smaller in the high-stress sample with a maximum reduction of 22%. (**Fig. 9**) This is likely due to a reduction of the resistance in the side-recess regions next to the gate. The stress level in these regions is higher than under the gate, as suggested by our simulations.

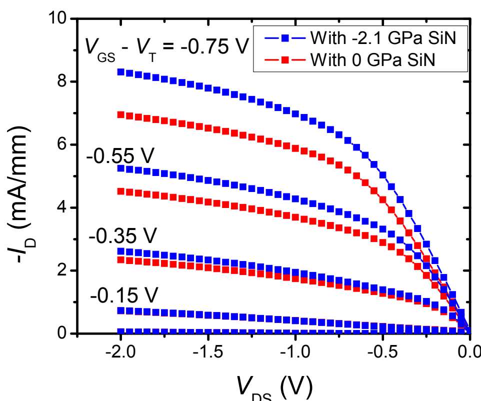

Fig. 6. Output characteristics of FETs with high-stress and zero-stress SiN films. L_G = 2 μm. Channel aligned with [-110] direction.

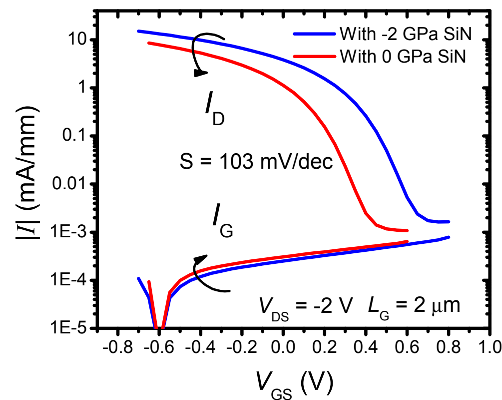

Fig. 7. Subthreshold characteristics of FETs with high-stress and zero-stress SiN films. L_G = 2 μm. Channel aligned with [-110] direction. The subthreshold slope of the devices is 103 mV/dec in both cases.

We have studied the L_G dependence of transconductance enhancement. $\Delta g_{mi}/g_{mi}^0$ becomes more pronounced as L_G decreases (**Fig. 10**), consistent with our mechanical model (**Fig. 5**).

We additionally investigated the dependences of the g_{mi} enhancement and R_{SD} reduction on the crystal orientation of hole transport. As shown in **Fig. 11**, we found the effect of uniaxial stress is not isotropic. In particular, the enhancement of g_{mi} is the highest when the channel is along [-110] direction and the lowest along [110]. The enhancement along the <100> directions is in between. A similar pattern was found in the relative magnitude of R_{SD} for different crystal orientations. (**Fig. 9**) The <110> anisotropy of enhancement agrees with earlier chip-bending measurements on this heterostructure: μ_h increases 12% per -100 MPa uniaxial stress along the channel direction with a [-110]-oriented channel, but only 4.6% per -100 MPa in the [110] channel [6]. One main reason for this is the asymmetric change of the valence band profile in the quantum well induced by piezoelectric effect. [6]

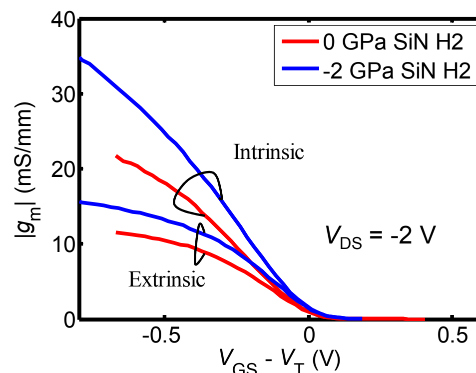

Fig. 8. Transconductance at V_{DS} = -2 V of FETs with high-stress and zero-stress SiN films. L_G = 2 μm. Channel aligned with [-110] direction.

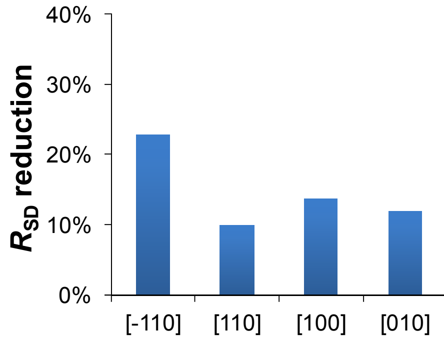

Fig. 9. Reduction in source-drain resistance extracted by gate current injection method for four major crystal orientations. A decrease of R_{SD} was seen in all four cases. Best results obtained in the [-110] orientation.

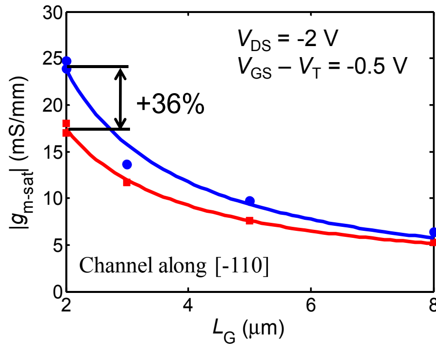

Fig. 10. Gate length dependence of peak intrinsic saturation-regime transconductance for high-stress and zero-stress samples along [-110].

Using *k.p* method, we have simulated the valence band structure (**Fig. 12** left) in our QW including the external uniaxial strain, built-in biaxial strain and the piezoelectric effect. We have calculated the average transport m^*, a key factor that impacts μ_h, by following the treatment in [13]. The calculated m^* exhibits a similar anisotropic behavior (**Fig. 12** right) as observed in the experiments.

Conclusions

We have developed a device architecture for p-type InGaAs FETs that incorporates uniaxial strain through a self-aligned dielectric stressor. For the first time, we demonstrate substantial enhancements in transport characteristics that originate in the combination of compressive process-induced uniaxial strain and compressive epitaxially grown biaxial strain. A maximum of 36% increase in the intrinsic transconductance in QW-FETs with L_G = 2 µm was observed. The structure exhibits promising gate-length scalability and is compatible with self-aligned source drain metal contacts. Our proposed device architecture holds promise to implement high-performance p-channel III-V FETs in a variety of material systems for future CMOS applications.

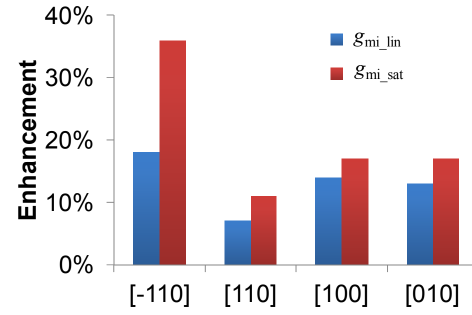

Fig. 11. Increase of intrinsic transconductance in linear regime (g_{mi_lin}) and saturation regime (g_{mi_sat}) for pFETs with L_G = 2 µm along the four major crystal orientations. Best results obtained along [-110] orientation.

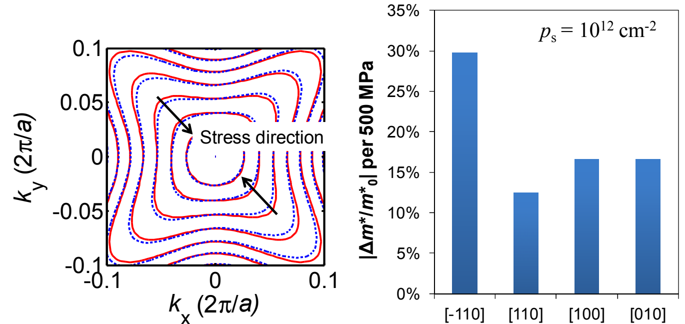

Fig. 12. (Left) *k.p* simulation showing anisotropic change of valence band with uniaxial stress. (Right) Change of average in-plane effective mass following a nonparabolic multi-band treatment, for <110> and <100> orientations. The maximum change in the effective mass along strain direction is calculated to occur along the [-110] direction.

Acknowledgements

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