Performance Enhancement of P-channel InGaAs Quantum-well FETs by Superposition of Process-induced Uniaxial Strain and Epitaxially-grown Biaxial Strain

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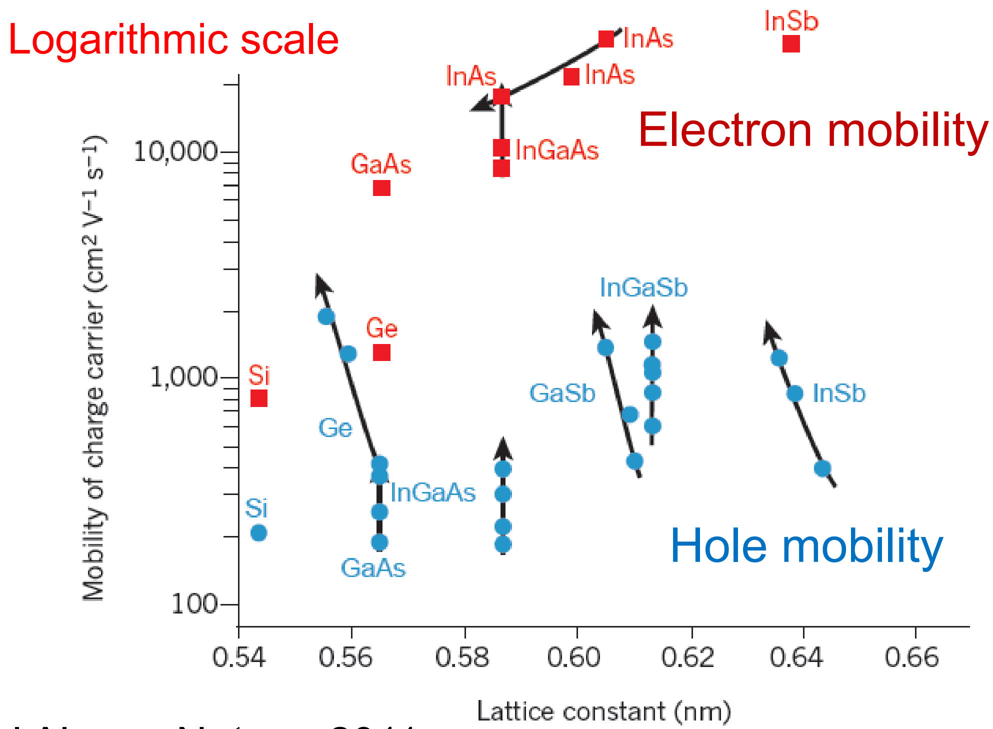
Fabrication: MTL at MIT.

Outline

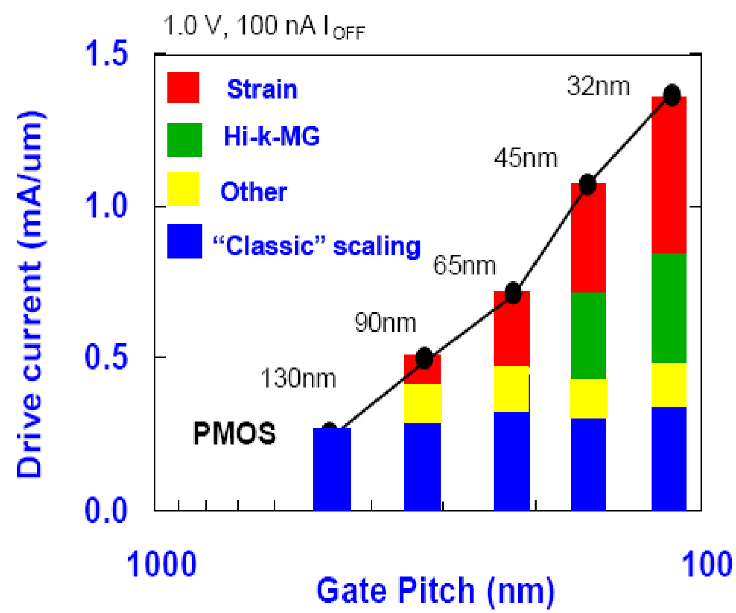
- Motivation
- Mechanical simulations
- Device technology
- Experimental results
- Conclusions

Motivation

- **Interests in InGaAs CMOS – Fueled by excellent v_e and μ_e**
- **Key challenge for InGaAs CMOS**
  - Bridging performance gap between n- and p-FET.
- **Our approach – Introduce strain to InGaAs p-FET**
  - Uniaxial + biaxial compressive strain



del Alamo, Nature, 2011

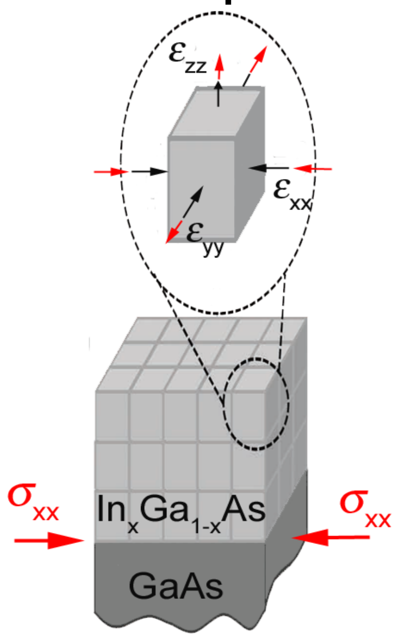


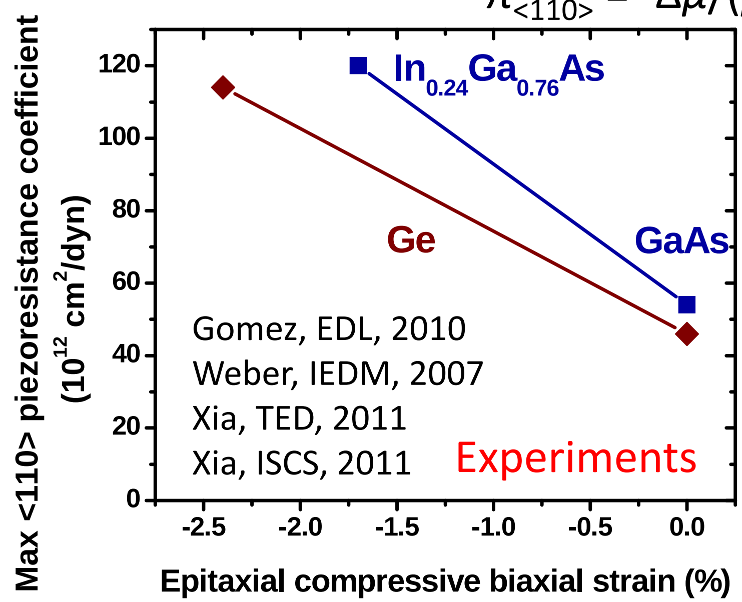
Kuhn, IWJT, 2010

Why biaxial strain + uniaxial strain?

- Sources for strain include:
  - Epitaxial lattice mismatch → Biaxial strain
  - Fabrication process → Uniaxial strain

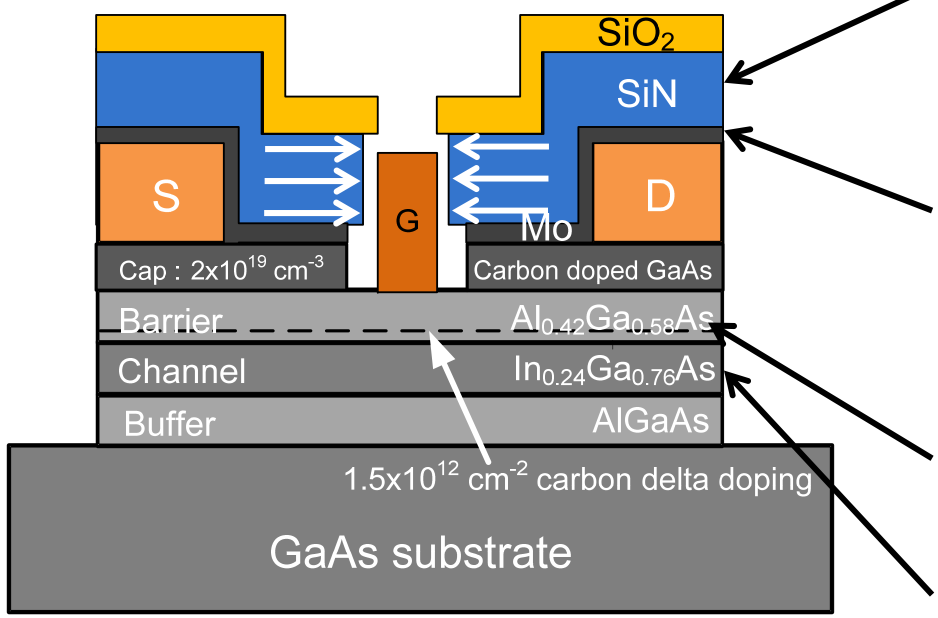
$\pi_{<110>} = -\Delta\mu/(\mu_0\sigma_{<110>})$





- Enhancements of μ_h by biaxial and uniaxial strain add superlinearly
- Similar effect found in Si simulations (Wang, TED, 2006)

InGaAs QW-FET with uniaxial + biaxial strain



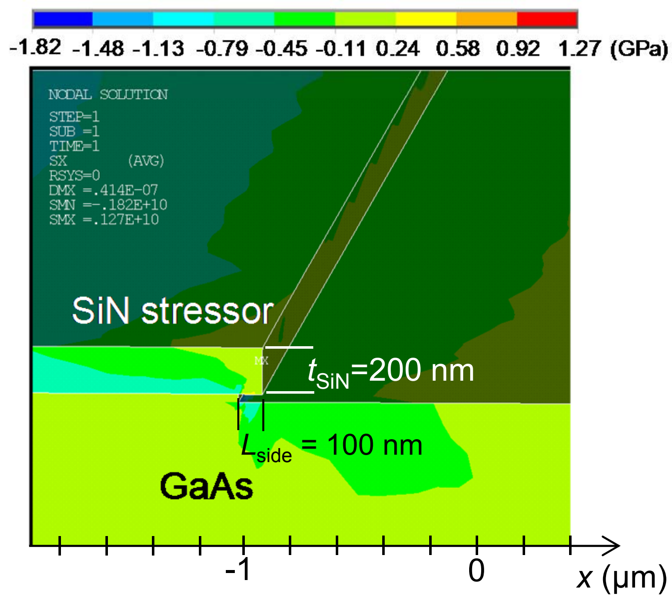
- Self-aligned stressor (compressively stressed)
- Self-aligned metal layer (Mo)
- Carbon delta-doping
- Biaxial strain in the channel as grown

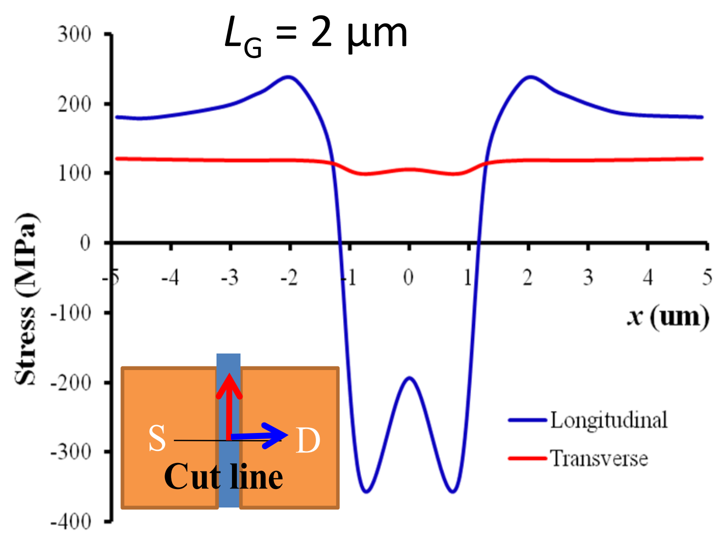
- Induced stress scalable with L_G (next slide)

Mechanical stress simulations

- Parameters used in simulations: t_{SiN} = 200 nm; SiN σ_{int} = -2 GPa

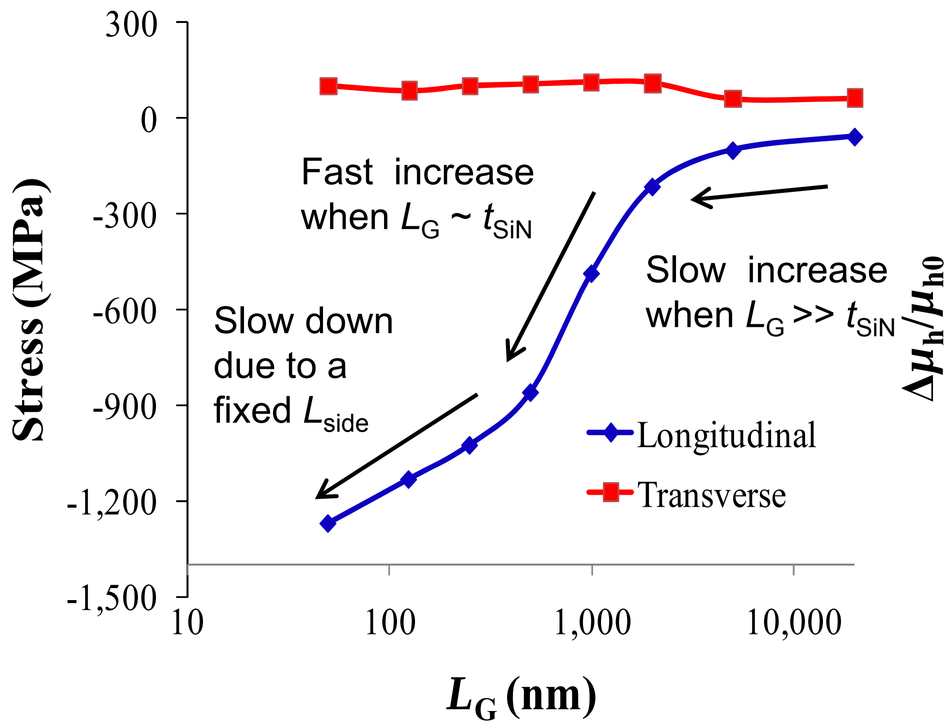
Longitudinal stress distribution

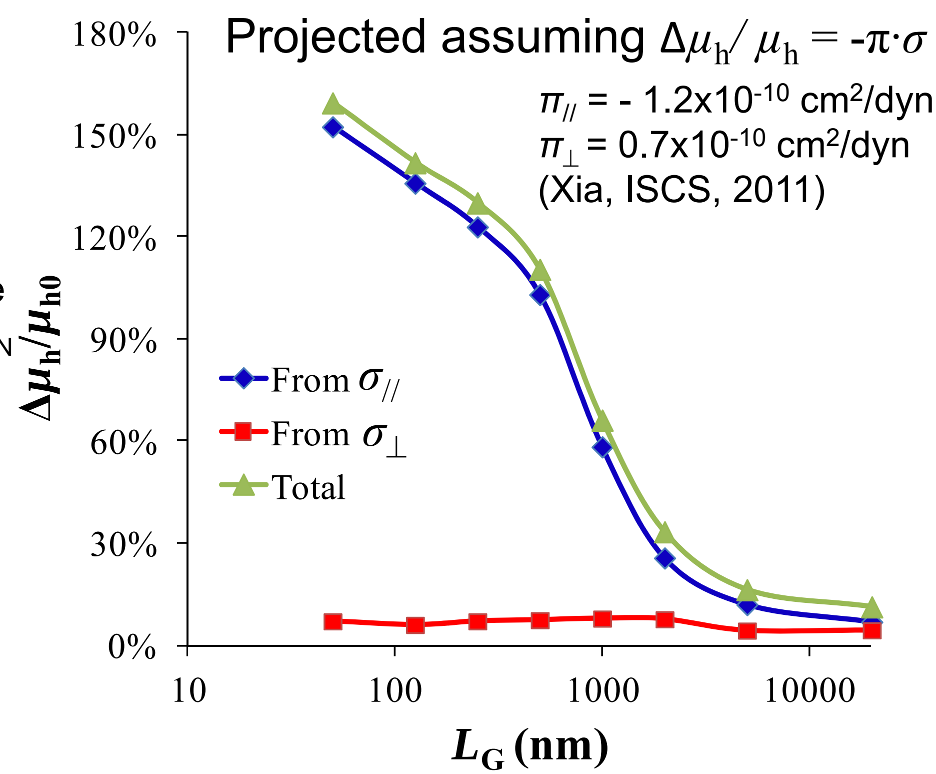




- Desirable stress type can be obtained with the proposed stressor structure
  - Compressive longitudinal stress → $\mu_h \uparrow$
  - Tensile transverse stress → $\mu_h \uparrow$

L_G scalability of induced stress at middle of gate



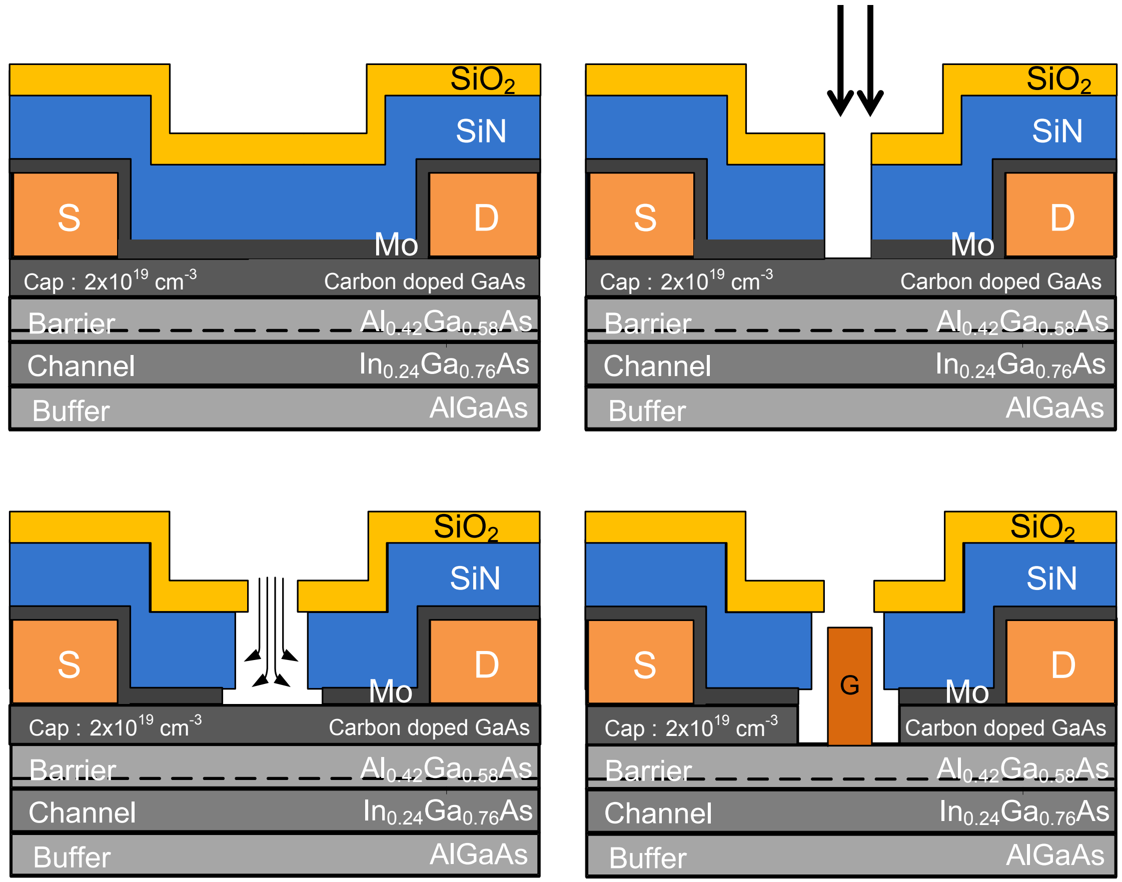


- L_G ↓ → Stress ↑ inside gate opening
- Assume linear Δμ with σ

  → >160% μ_h enhancement for L_G < 50 nm

Device technology

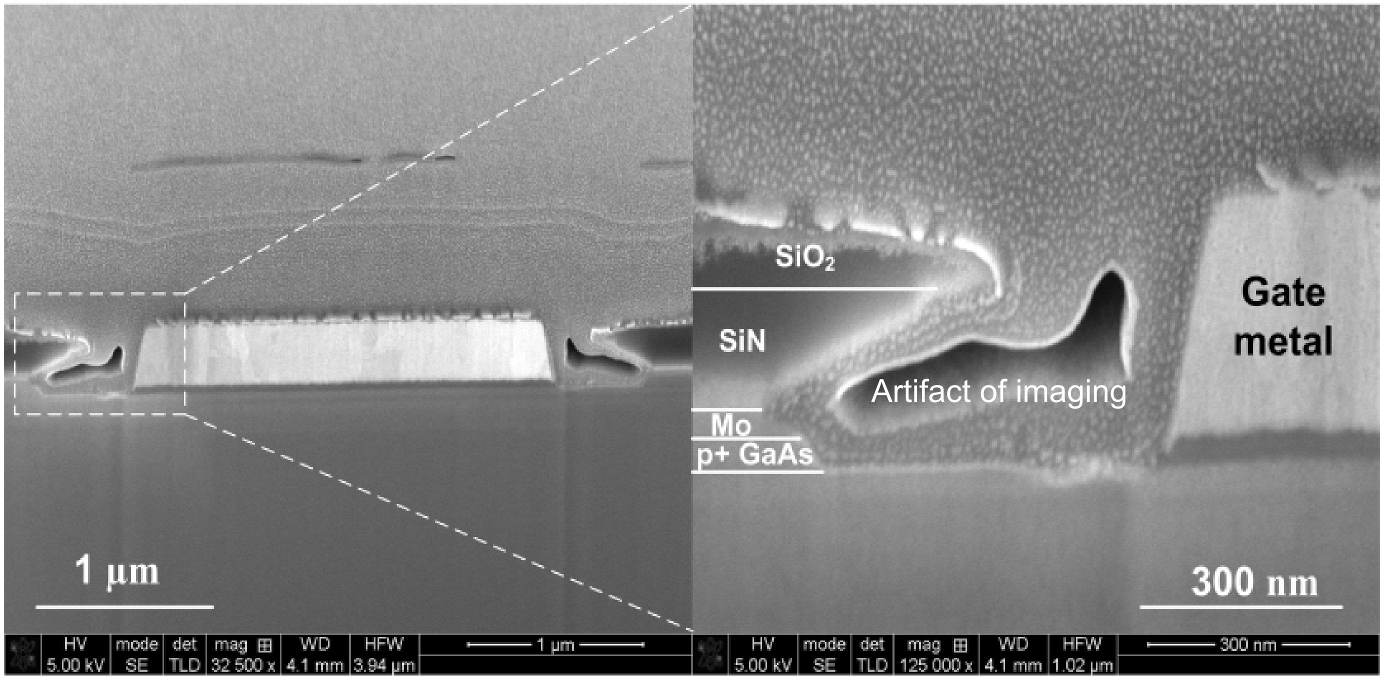
- Mesa isolation
- Ohmic metalization
- Molybdenum (Mo) deposition
- PECVD SiN stressor and SiO_2
- Anisotropic ECR RIE SiO_2/SiN
- Anisotropic ECR RIE Mo
- Isotropic RIE Mo
- GaAs cap recess by wet etching
- Gate metalization



Key considerations:

- Avoid Mo layer short to gate metal
- Air gap as small as possible

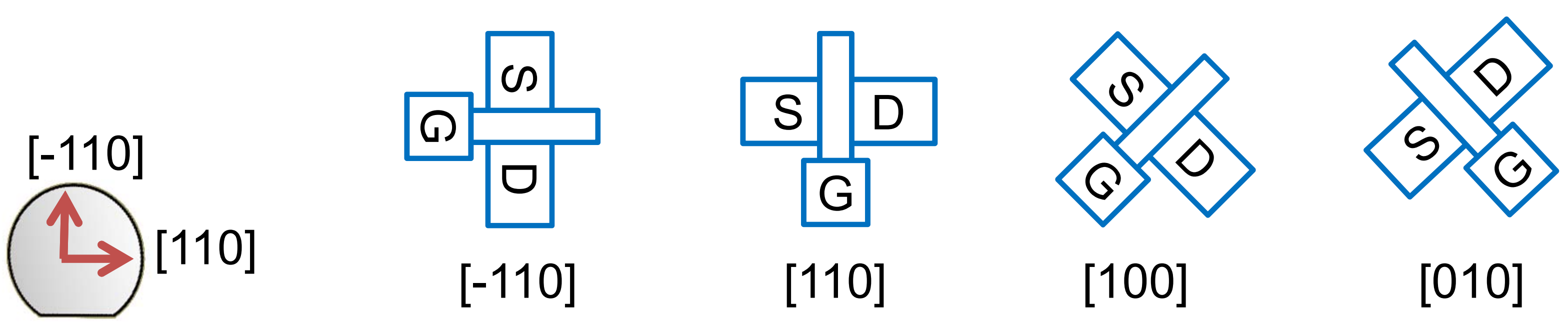
Device cross-section



- L_G = 2 µm; channel along [-110]
- $L_{side} \approx$ 400 nm

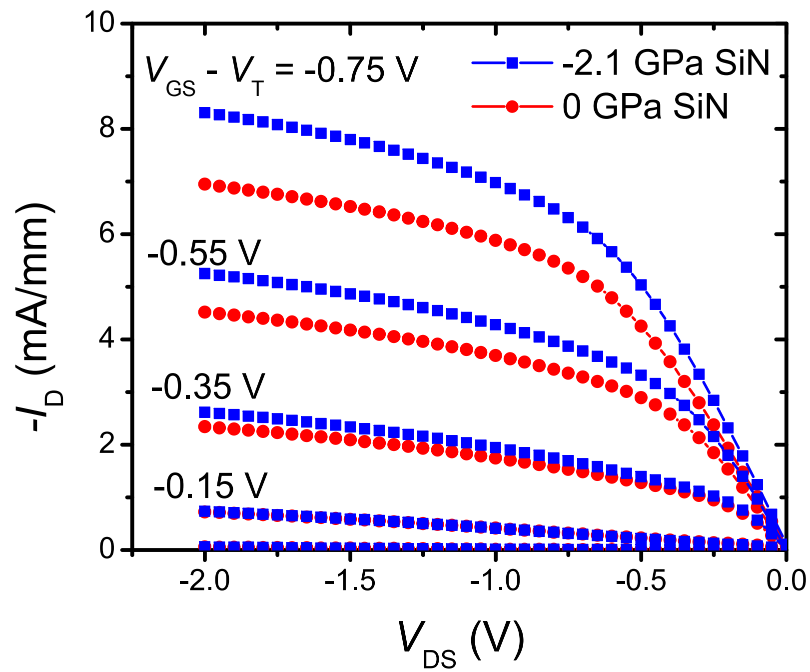
Experimental parameters for devices

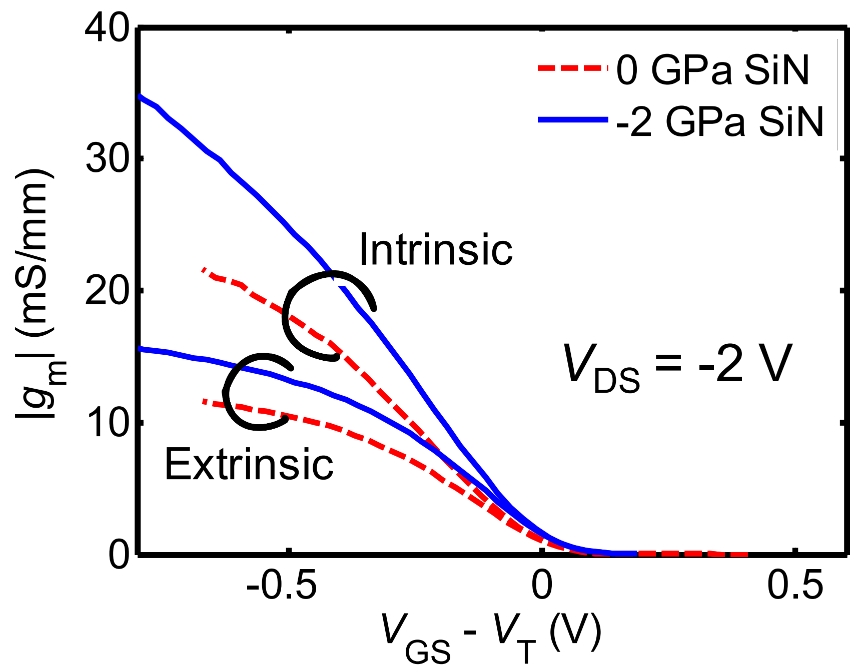
- Split experiments:
  - SiN with -2.1 GPa stress *vs* SiN with 0 Pa stress
  - SiN film stress obtained from wafer curvature measurements
- L_G = 2 μm to 8 μm
- Four channel orientations:



QW-FET electrical characteristics

- Example: L_G = 2 μm; channel along [-110]

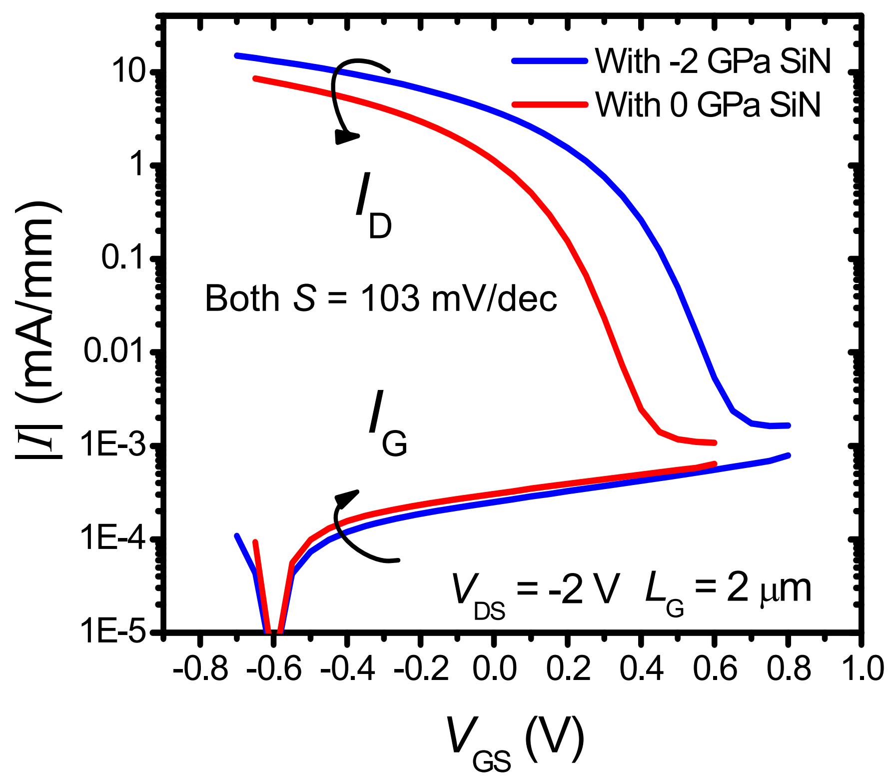




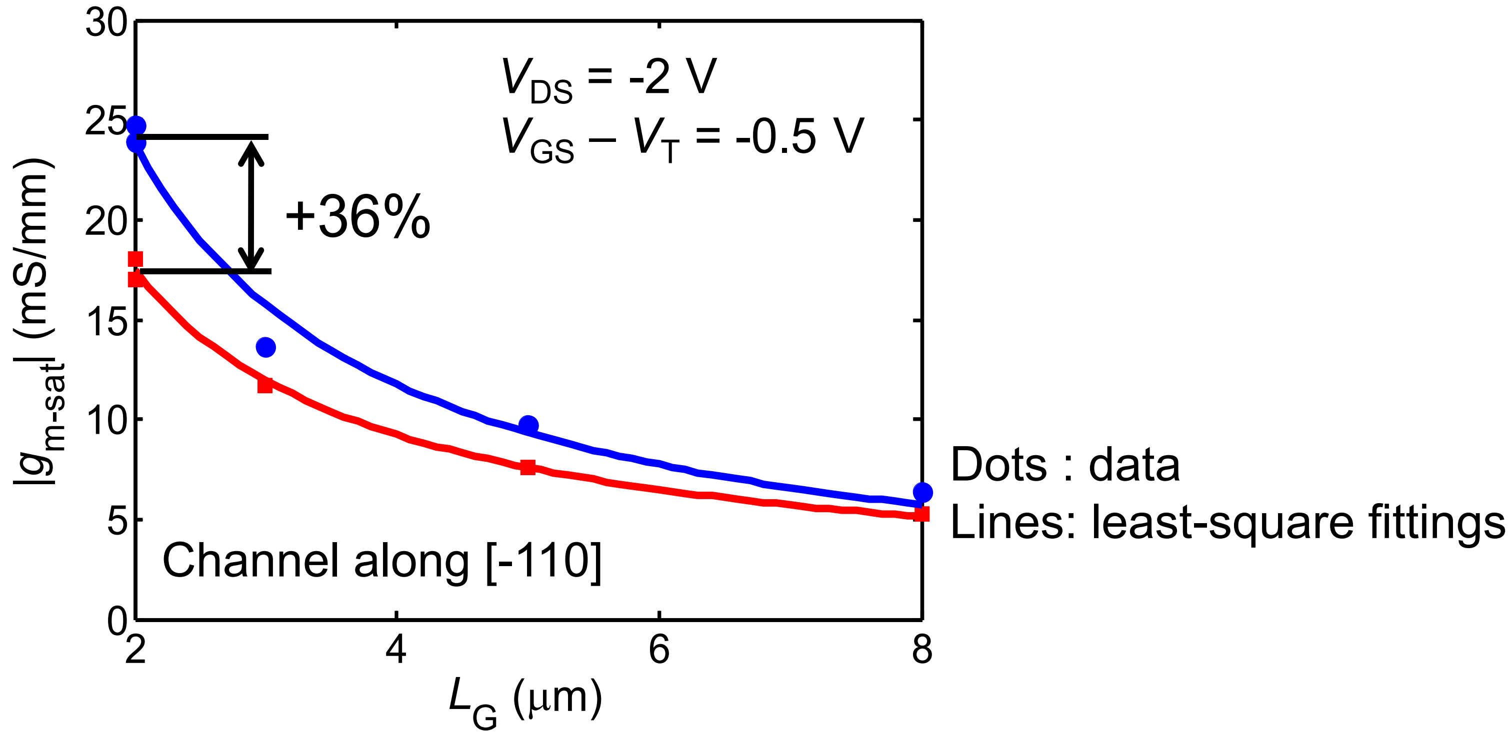
- Significant drive current increase
- Transconductance increase at all gate overdrives

Subthreshold characteristics and V_T

- Similar I_G as chemically etched samples→ No RIE damage
- V_T shift between high- and low- stress samples
  - Likely due to different anisotropic RIE overetch

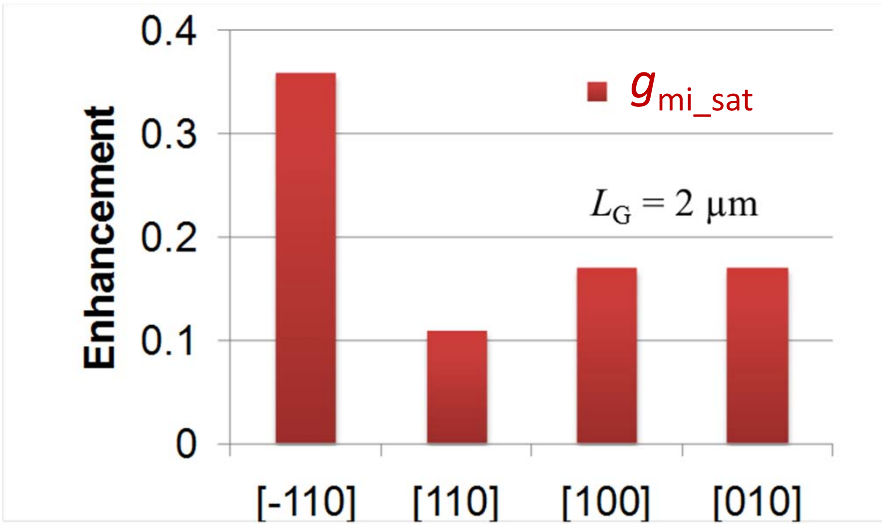


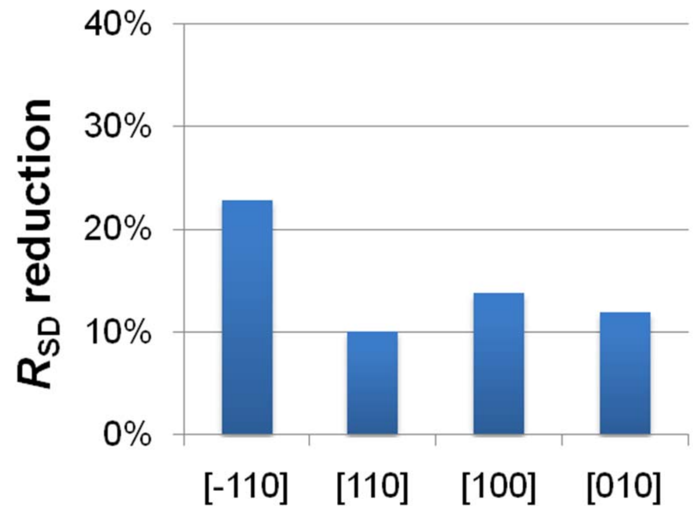
L_G dependence of g_m



- Increasing enhancement observed with decreasing L_G
- Consistent with stress simulations + π measurements
  - >160% enhancement expected with L_G < 50 nm

Crystal direction dependence

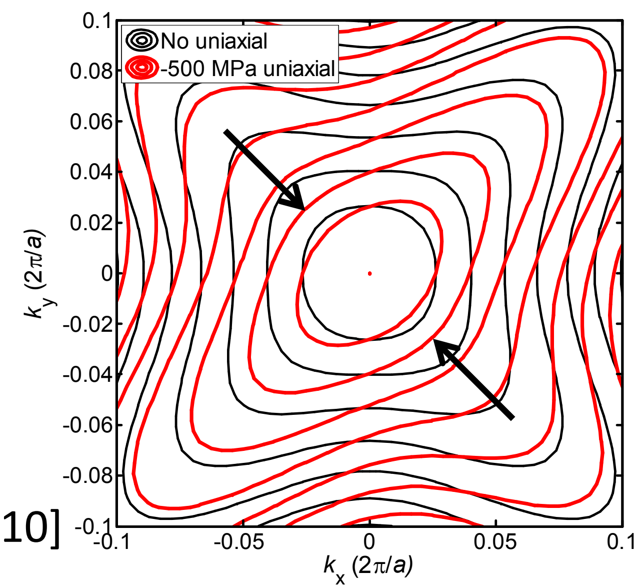


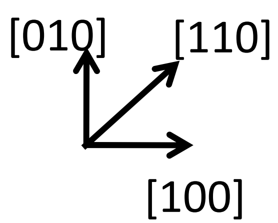


- Observed anisotropic Δg_{mi} and ΔR_{SD}
  - g_{mi} extracted using g_{mext}, R_S, R_D and g_D
  - R_S, R_D extracted using gate current injection method
- <110> anisotropy consistent with measurements of piezoresistance coefficients
  - $\pi_{[-110]} : \pi_{[110]}$ = 2.6 (Xia, ISCS, 2011)

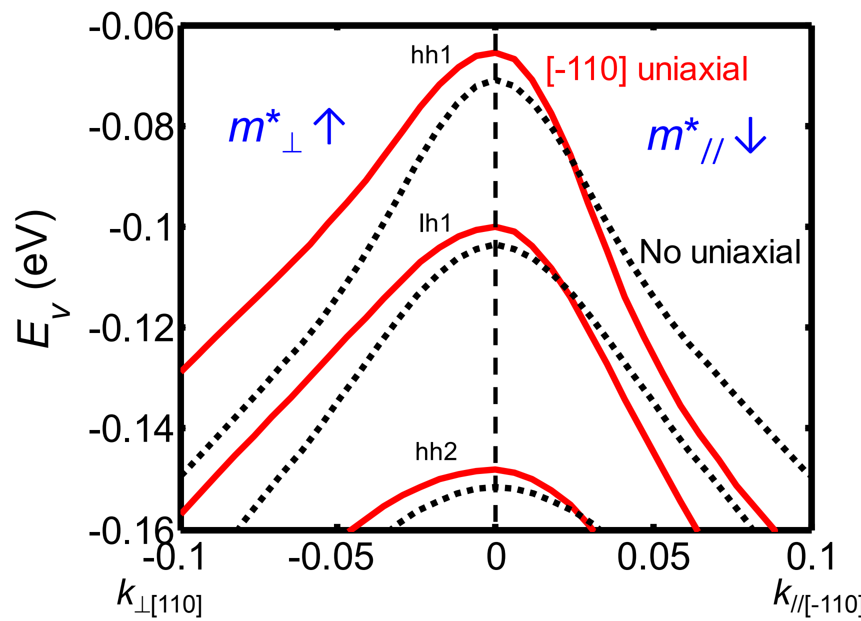
Theoretical discussions

- Valence band change due to strain in InGaAs
  - Used *k.p* methods (nextnano[3])
  - Calculated subbands in $In_{0.24}Ga_{0.76}As$ quantum well





In-plane iso-energy contours of hh1 ***with*** and ***without*** uniaxial strain



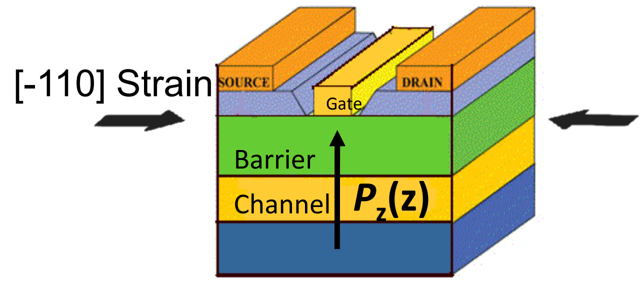
- Compressive strain parallel to channel is desirable

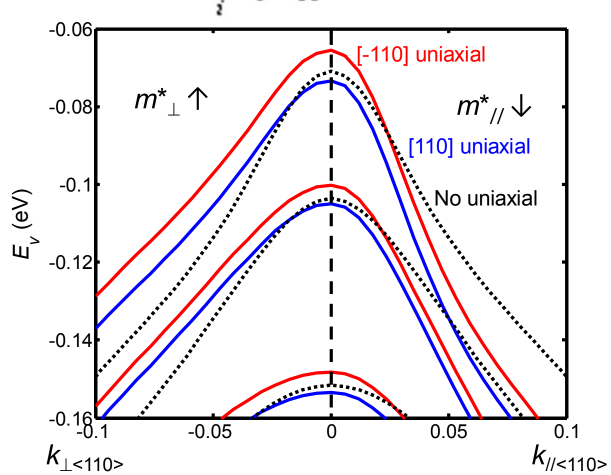
Effective mass model

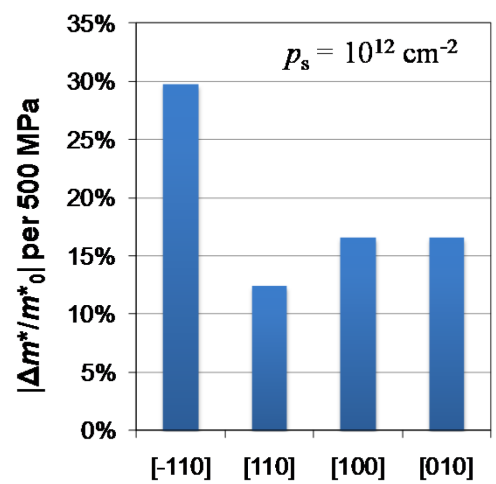
- Treat nonparabolic valence band using energy dependent *m** (De Michielis, TED, 2007)

$$\mu = \frac{q\tau}{m^*} \qquad m_i^*(E,\vec{k}_i) = \frac{\hbar^2 |\vec{k}_i|^2}{2(E_{vi}-E_i)}$$

$$m^*(\vec{k}) = \frac{\sum_i \int_{-\infty}^{E_{vi}} m_i^*(E,\vec{k}) f(E) g_i(E) dE}{\sum_i \int_{-\infty}^{E_{vi}} f(E) g_i(E) dE}$$







From simulations:

- Δm^* anisotropy induced by quantization change due to piezoelectric effect
- Δm^* anisotropy consistent with g_m measurements.

Conclusions

- Developed device architecture for InGaAs p-FETs that incorporates uniaxial strain through self-aligned dielectric stressor
- Key results:
  - Biaxial strain + uniaxial strain → substantial enhancements in transport characteristics
  - Up to +36% Δg_m observed in L_G = 2 μm device
  - Strong enhancement anisotropy due to piezoelectric effect
- For further enhancement:
  - Scale down L_G and bring S/D closer
  - Project Δg_m >160% @ L_G < 50 nm
- Study useful to other p-type III-V materials (e.g. InGaSb, InSb)