High-Voltage DC and RF Power Reliability of GaN HEMTs

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ICNS 2011

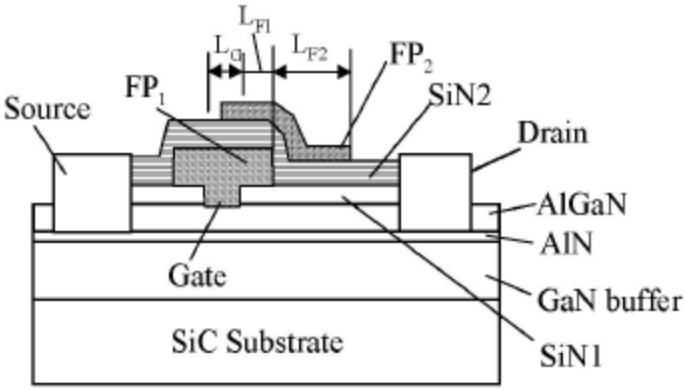
Glasgow, July 10-15, 2011

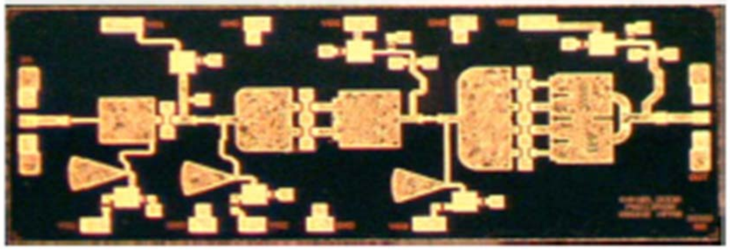
Acknowledgements:

ARL (DARPA-WBGS program), ONR (DRIFT-MURI program)

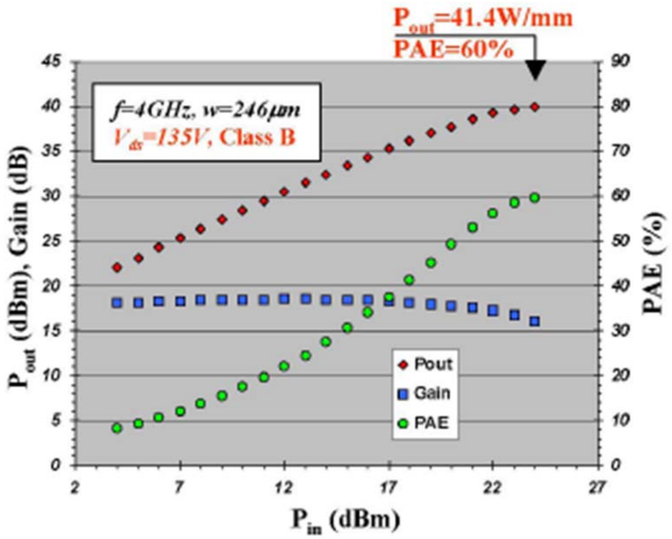
Accel-RF Corporation

Breakthrough RF-mmw power in GaN HEMTs





Micovic, MTT-S 2010

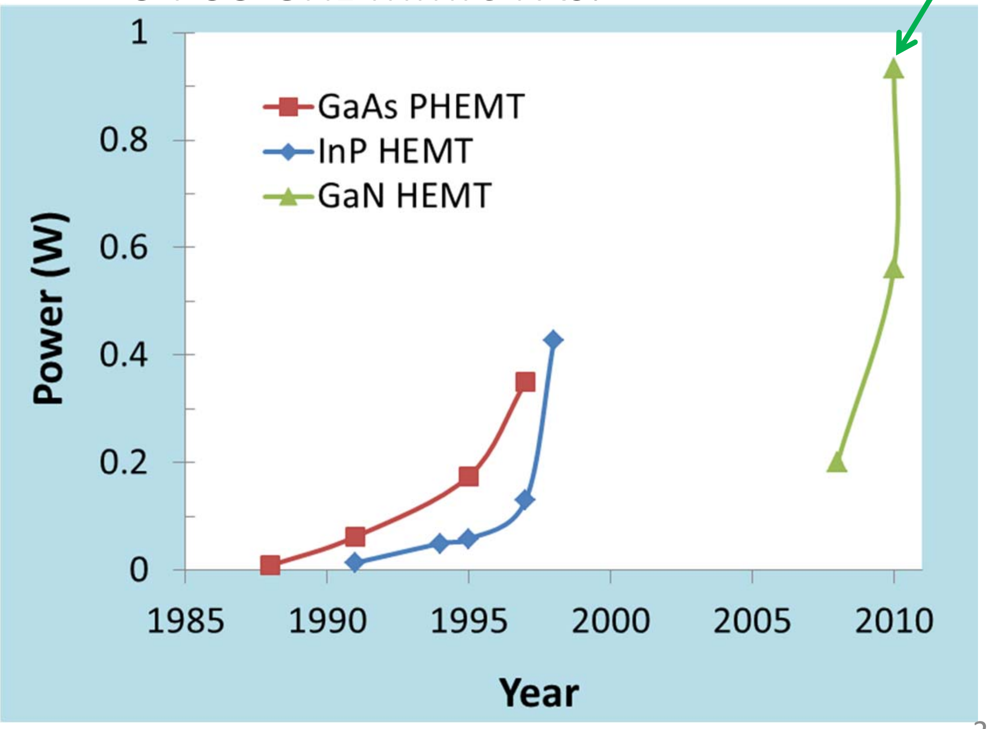


P_{out}>40 W/mm, over 10X GaAs!

Wu, DRC 2006

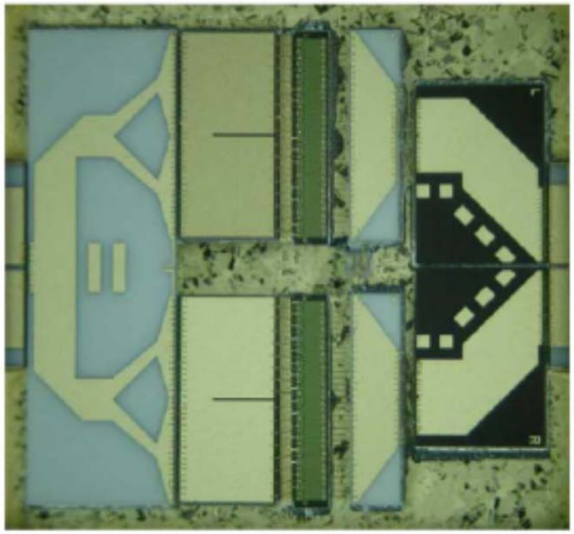
Micovic, Cornell Conf 2010

94-95 GHz MMIC PAs:



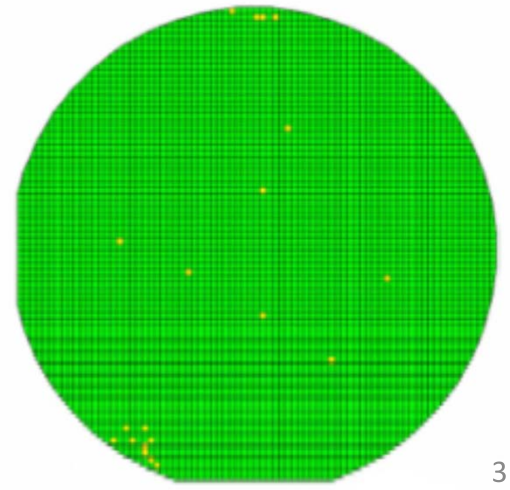
GaN HEMTs in the field

Counter-IED Systems (CREW)

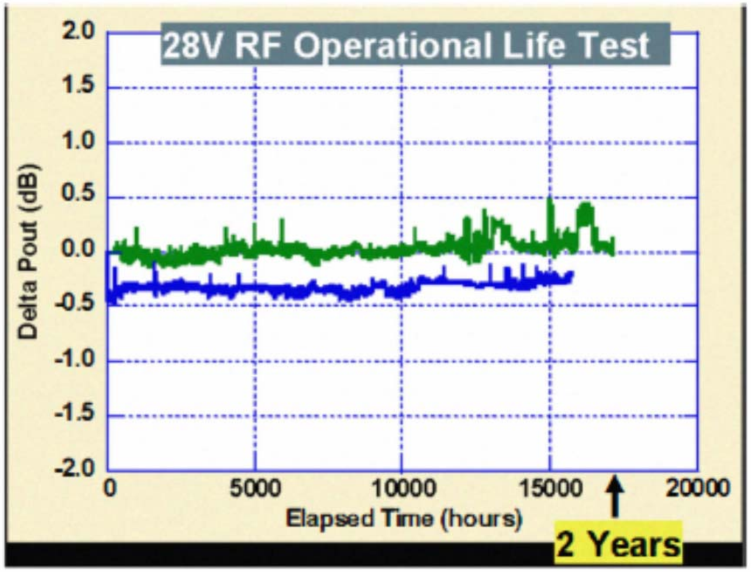


200 W GaN HEMT for cellular base station
Kawano, APMC 2005

100 mm GaN-on-SiC volume manufacturing
Palmour, MTT-S 2010

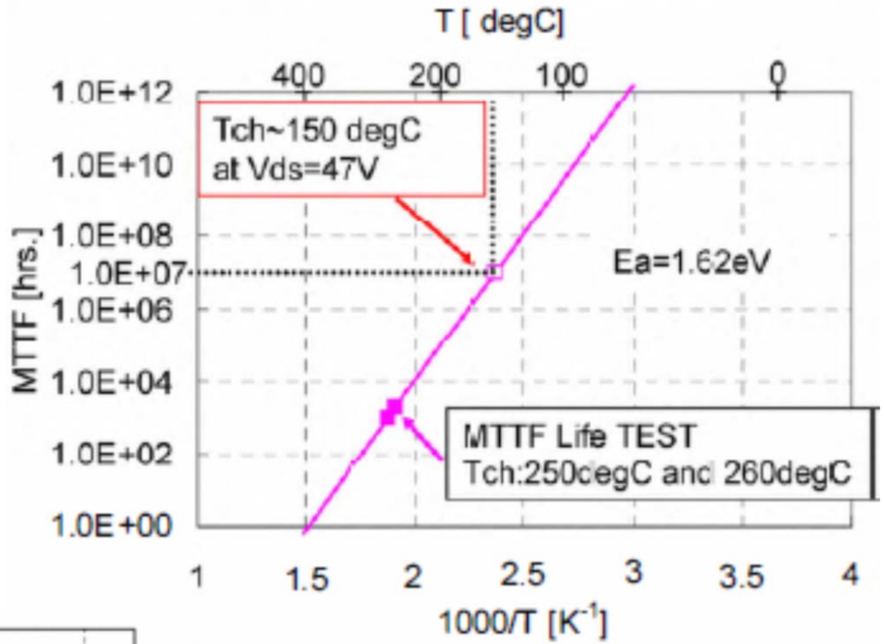


Recent great strides in RF power reliability



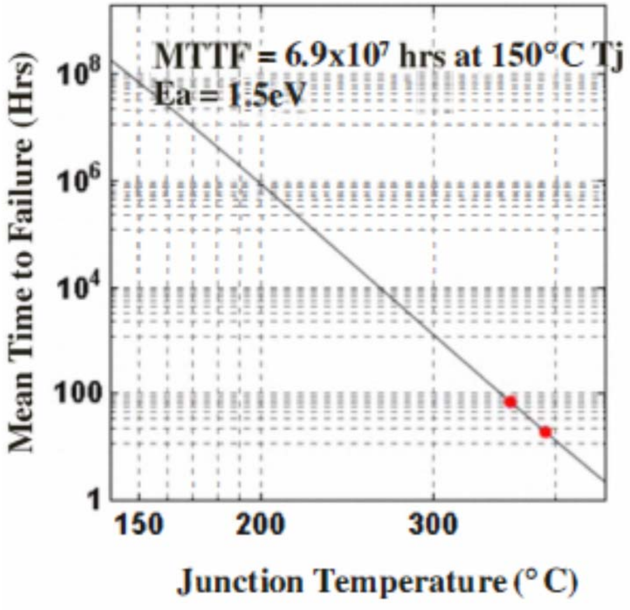
28 V RF oper. life > 2 years (X-band, 3 dB comp., ~150^{o}C)

Kolias, MTT-S 2010



MTTF=1x10^7 h at 47 V (C-band, 5 dB comp., ~150^{o}C)

Yamasaki, MTT-S 2010



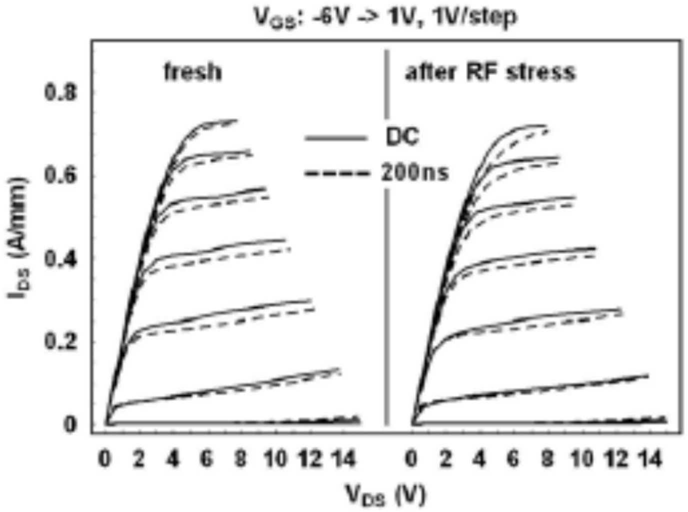
MTTF=7x10^7 h at 28 V (40 GHz, 1.5 dB comp., ~150^{o}C)

Heying, MTT-S 2010

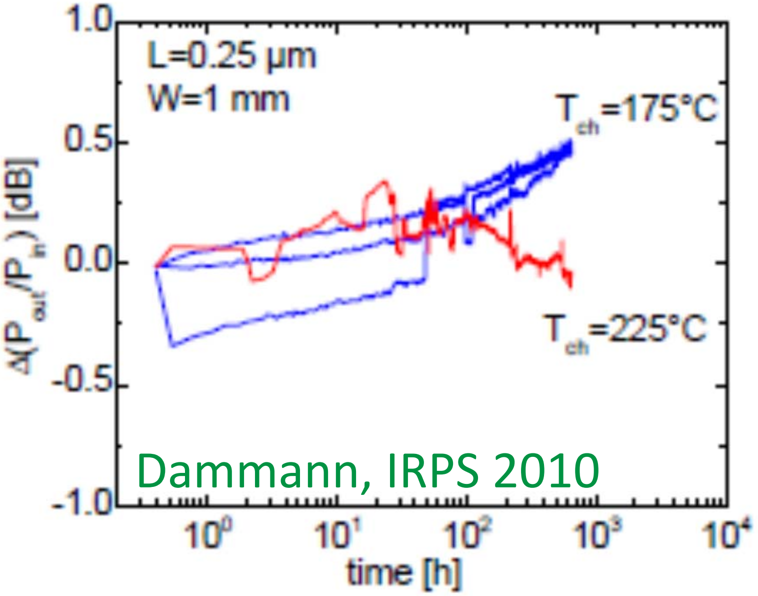
Dominant degradation mechanisms under RF stress?

- In general:
  - RF stress → P_{out}↓, Gain↓, I_{Dmax}↓, $|I_G|$↑, V_T shift, dispersion↑
  - RF introduces more degradation than DC
  - RF stress accelerated by V_{DQ}, P_{in}, T_j

Conway, IRPS 2007; Joh, ROCS 2008, IEDM 2010, ROCS 2011; Chini, IEDM 2009



Chini, EUMW 2009



Dammann, IRPS 2010

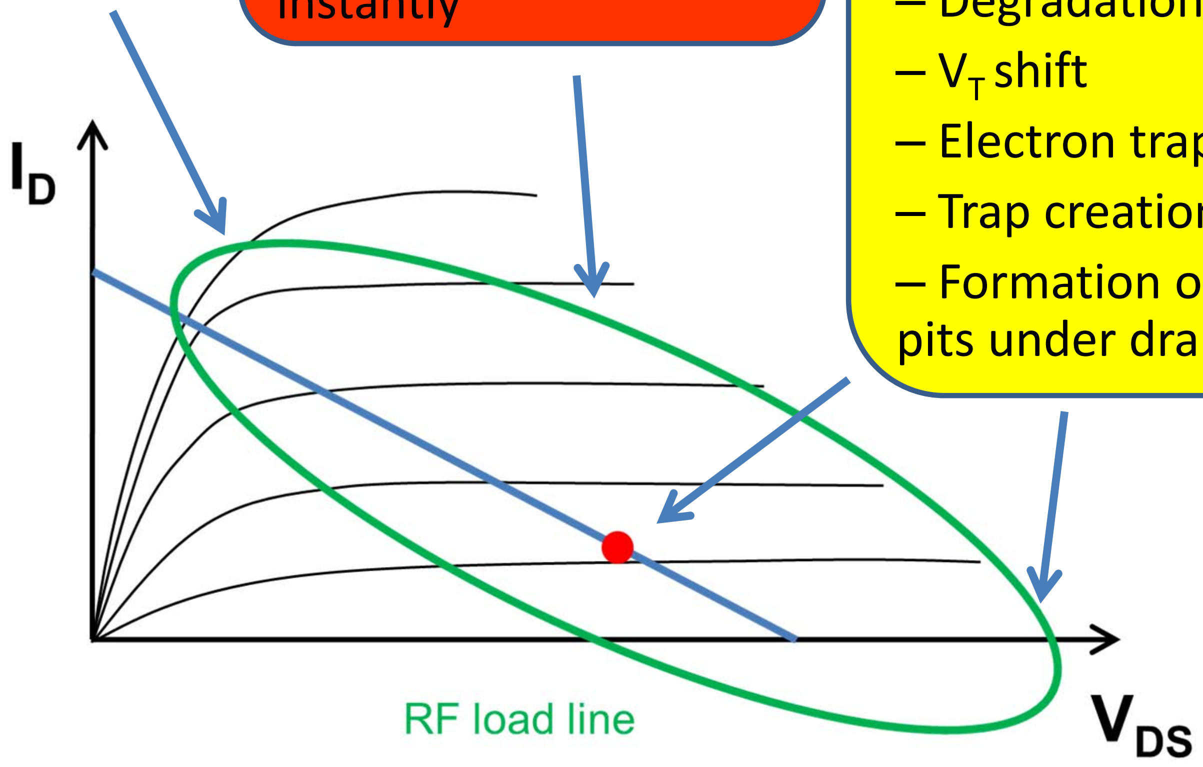
- Indications of two competing mechanisms:
  - Trap creation and trapping?
  - Field-driven structural degradation?

Rozman, ROCS 2009; Chini, IEDM 2009

Outline

1. RF power reliability concerns
2. Methodology for RF reliability experiments
3. Electrical and structural results
4. Discussion: the role of gate placement
5. Conclusions

RF power reliability concerns



ON DC stress:

– Mostly benign

High-power DC stress:

– Not accessible to DC stress experiments

– Device blows up instantly

OFF and semi-ON high-voltage DC stress :

– Degradation of I_{Dmax}, R_D, I_{Goff}

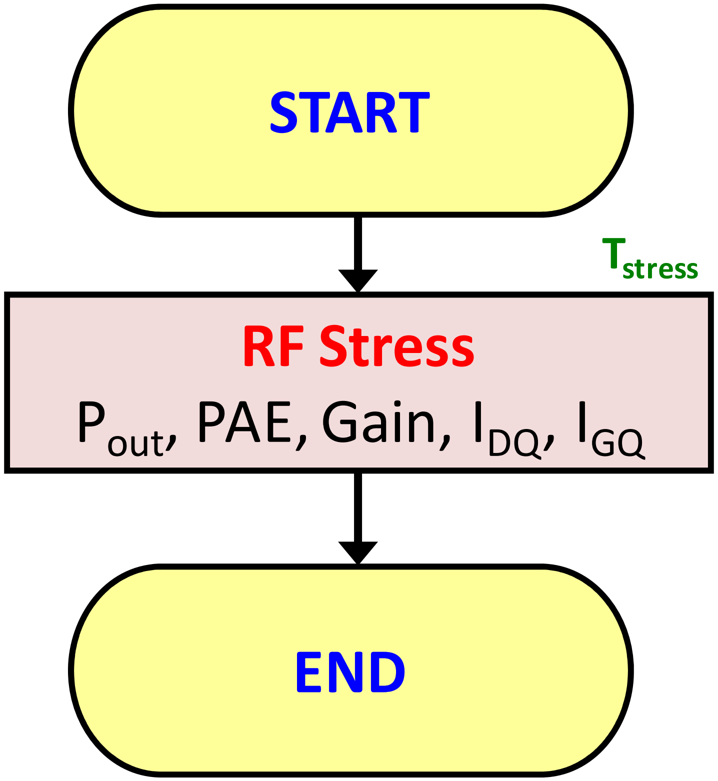
– V_T shift

– Electron trapping

– Trap creation

– Formation of grooves and pits under drain-end of gate

RF experiment flowchart: conventional approach



START

T_{stress}

RF Stress

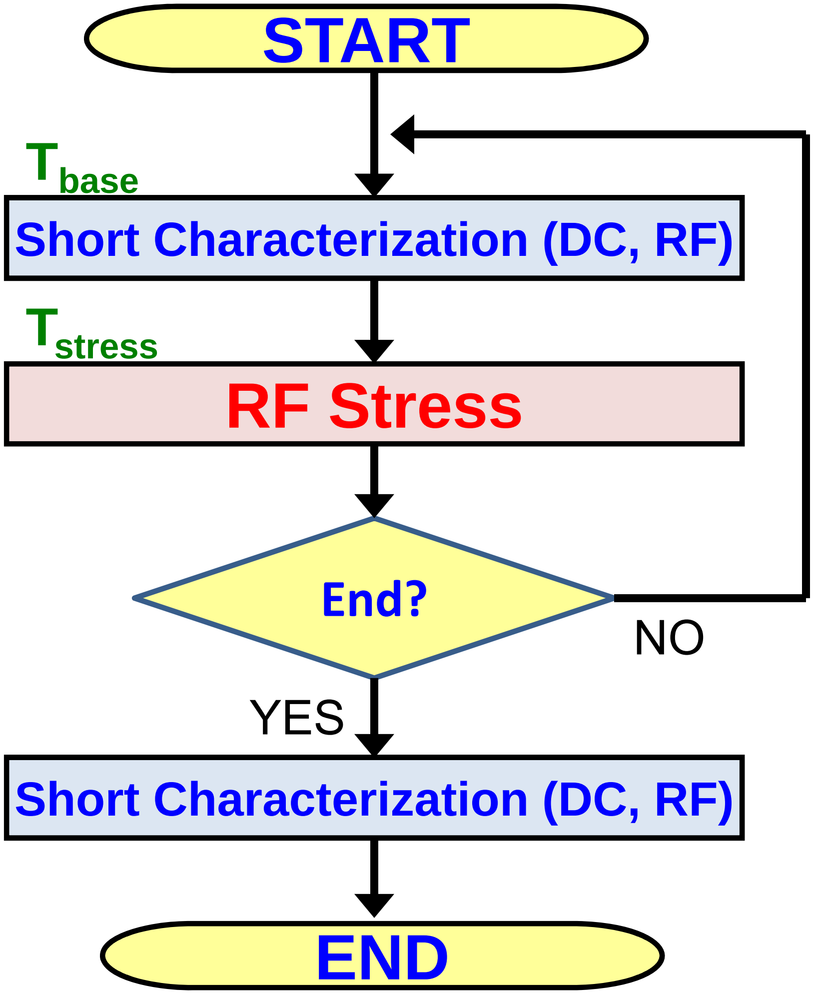
P_{out}, PAE, Gain, I_{DQ}, I_{GQ}

END

Limitations:

- Bias point shifts during stress
- Limited RF characterization
- No DC characterization
- No trap characterization
- If examining different RF conditions, RF characterization confusing

RF experiment flowchart: improved approach (I)



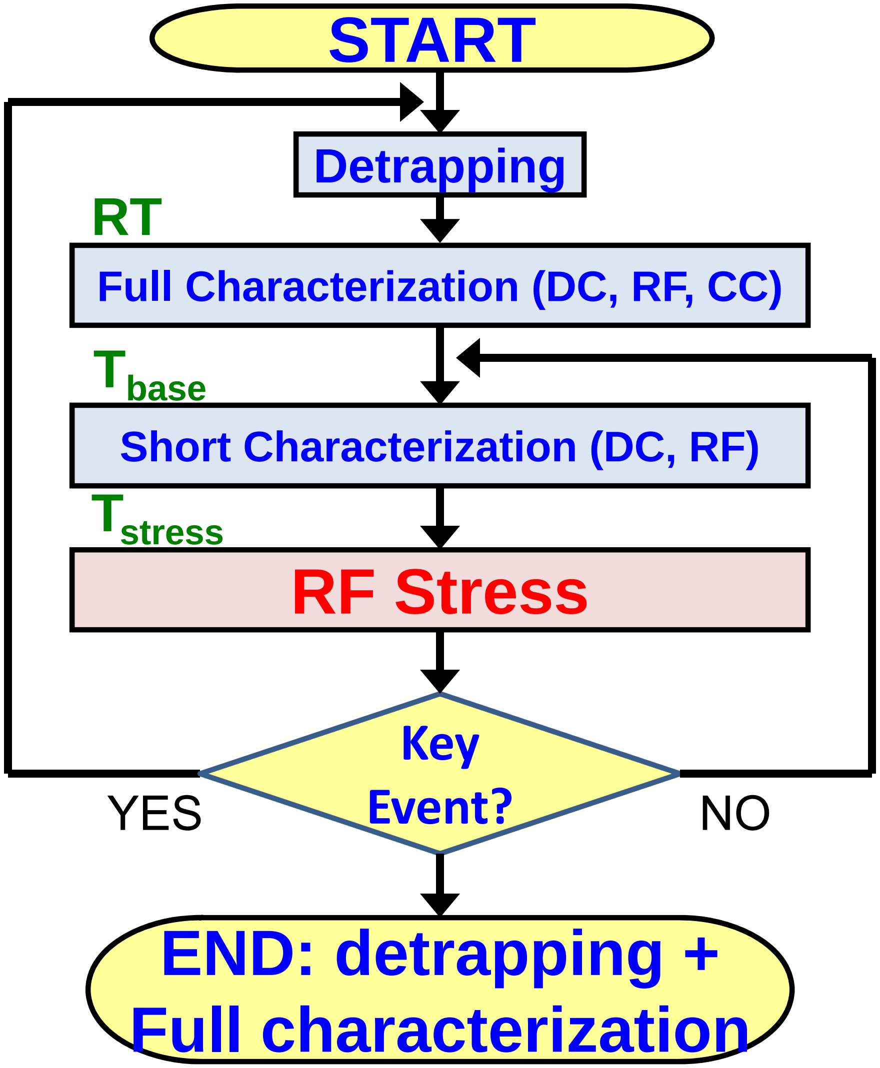
New features:

- RF and DC characterization under standardized conditions
- At beginning, end and periodically through experiment

Limitations:

- Limited characterization
- Characterization temperature cannot be too different from stress temperature
- Cannot separate trapping from "permanent" degradation

RF experiment flowchart: improved approach (II)



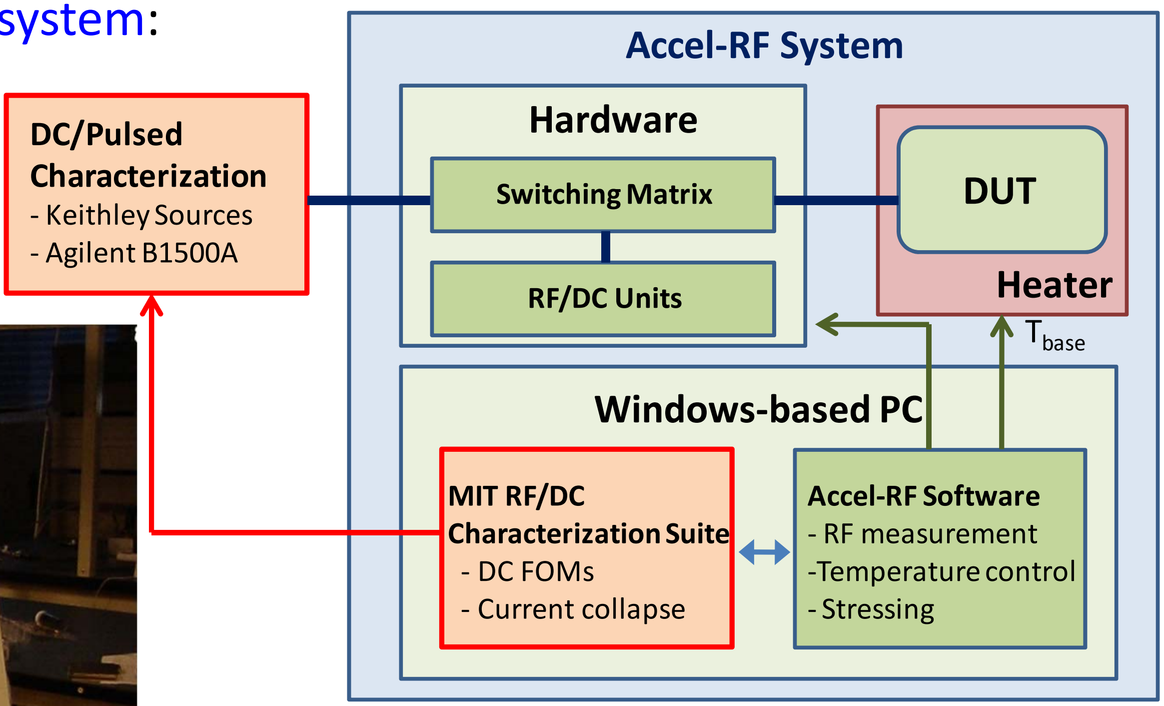
New features:

- Comprehensive DC, RF and pulsed characterization under standardized conditions (RT)
- At beginning, end, and during experiment
- Detrapping step to enable trap characterization

Setup for RF reliability studies

Accel-RF AARTS RF10000-4/S system:

- two 2-4 GHz channels
- two 7-12 GHz channels
- Max P_{in}=30 dBm
- T_{base}=50-200 °C



DC/Pulsed Characterization
- Keithley Sources
- Agilent B1500A

Accel-RF System

Hardware

Switching Matrix

RF/DC Units

DUT

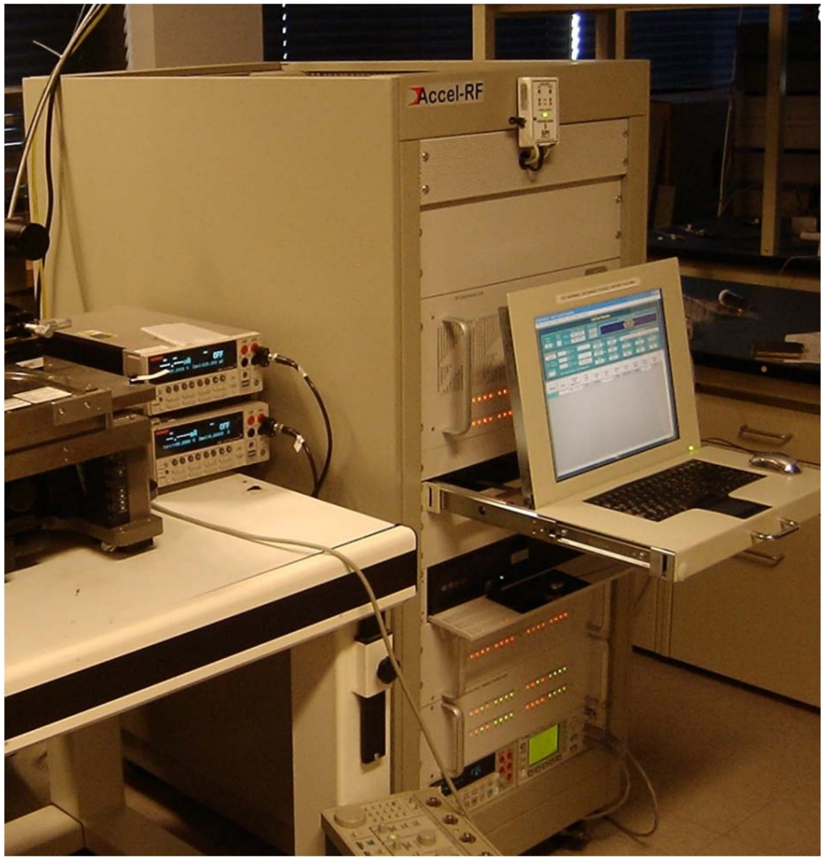
Heater

T_{base}

Windows-based PC

MIT RF/DC Characterization Suite
- DC FOMs
- Current collapse

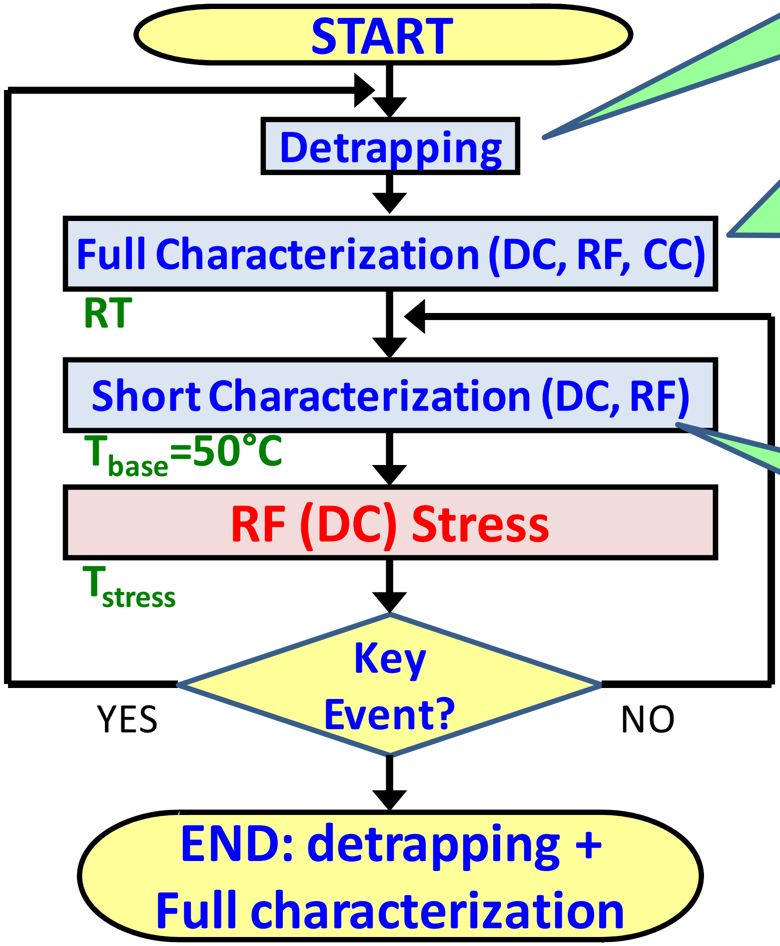
Accel-RF Software
- RF measurement
-Temperature control
- Stressing



Augmented with:

- external instrumentation for DC/pulsed characterization
- software to control external instrumentation and extract DC and RF FOMs

RF-stress experiments



START

Detrapping

Full Characterization (DC, RF, CC)

RT

Short Characterization (DC, RF)

T_{base}=50°C

RF (DC) Stress

T_{stress}

Key Event?

YES

NO

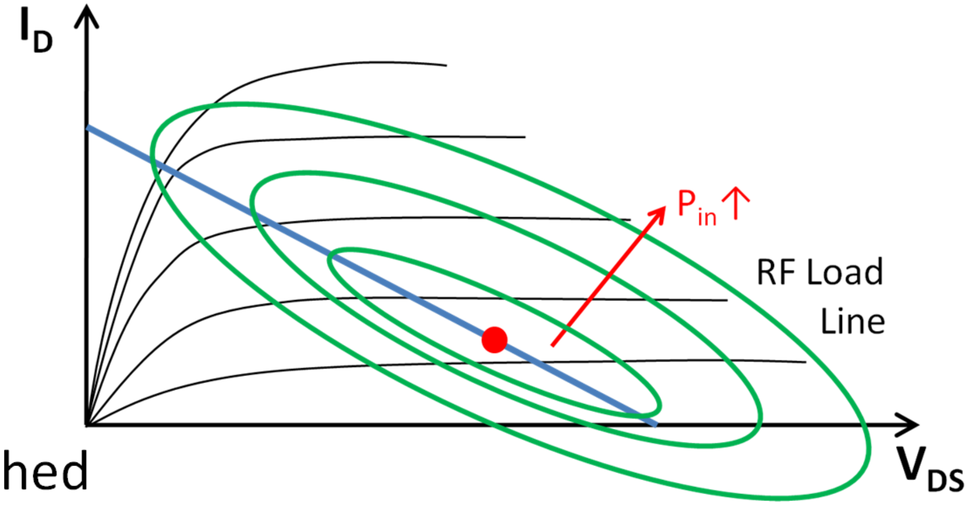
END: detrapping + Full characterization

T_{base}=100°C for 30 mins

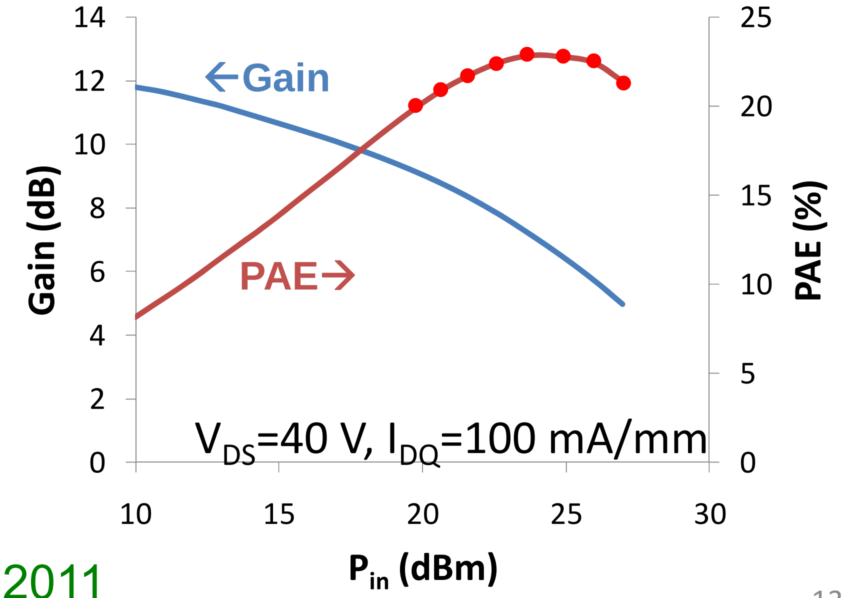
- Full DC I-V sweeps
- RF power sweep @ V_{DS}=28 V, I_{DQ}=100 mA/mm
- Current collapse (after 1” V_{DS}=0, V_{GS}=-10 V pulse)
- Room temperature

- DC FOMs: I_{Dmax}, R_S, R_D, V_T, I_{Goff}, …
- RF FOMs @ V_{DS}=28 V, I_{DQ}=100 mA/mm
  - Saturated conditions (P_{in}=23 dBm): $P_{out,sat}$, G_{sat}, PAE
  - Linear conditions (P_{in}=10 dBm): G_{lin}
- Every few minutes at T_{base}=50°C

RF stress experiments: P_{in} step-stress

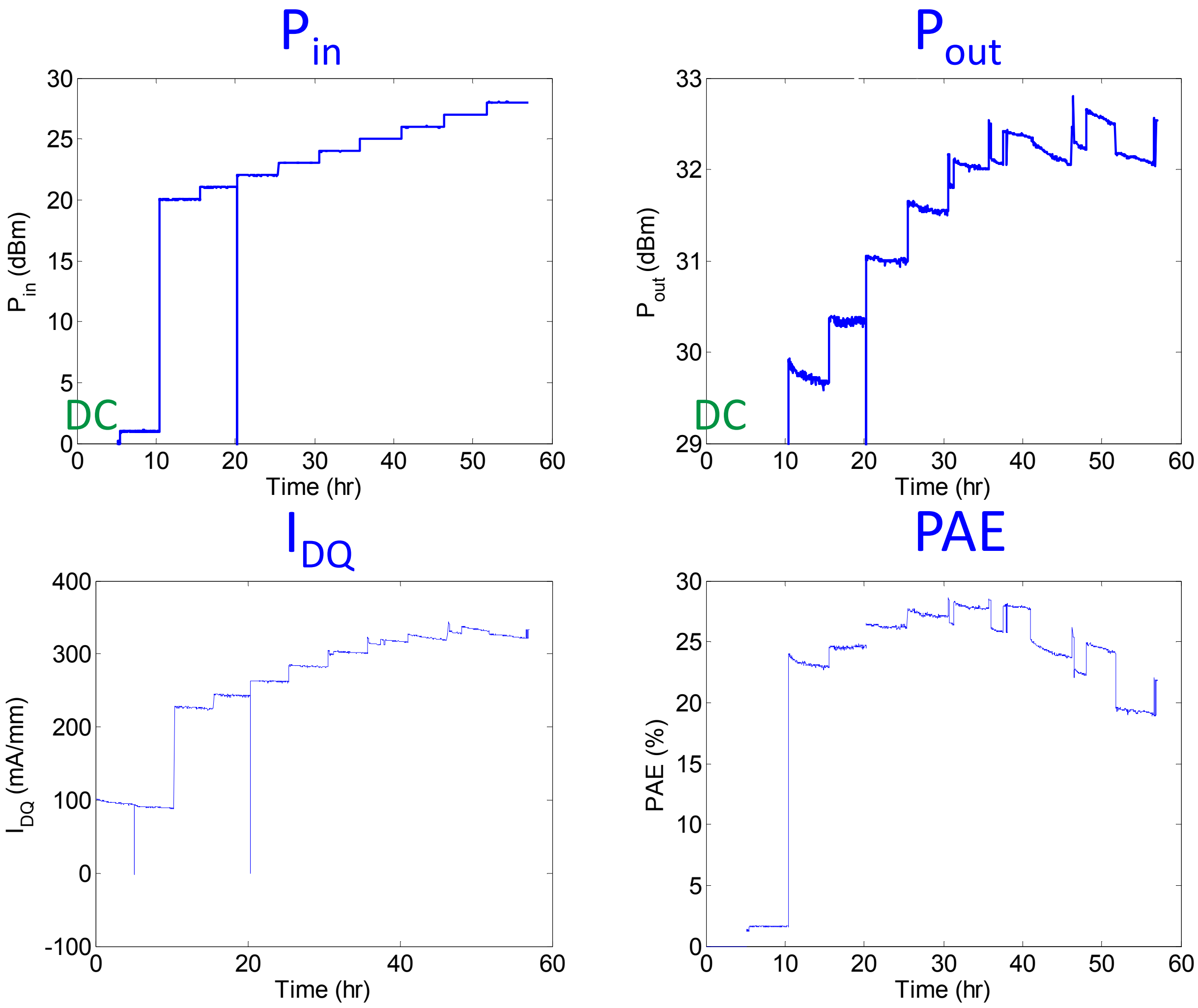


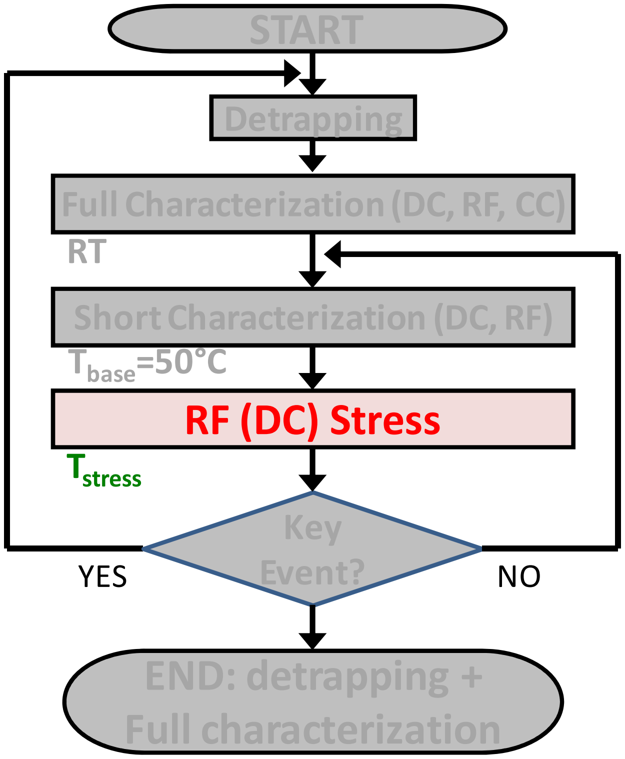
- Motivation:
  - higher P_{in} → larger V waveform at output
- MMIC:
  - single-stage internally-matched
  - 4x100 µm GaN HEMT (OFF-state V_{crit} >60 V at RT)
  - Gate centered in S-D gap
- Step P_{in} stress:
  - V_{DS} = 40 V, I_{DQ} = 100 mA/mm
  - P_{in} = 0 (DC), 1, 20-27 dBm
  - 300 min stress at each step
  - T_{stress}=50 °C (T_j=110-230°C)



Joh, ROCS 2011

Evolution of RF stress





START

Detrapping

Full Characterization (DC, RF, CC)

RT

Short Characterization (DC, RF)

T_{base}=50°C

RF (DC) Stress

T_{stress}

Key Event?

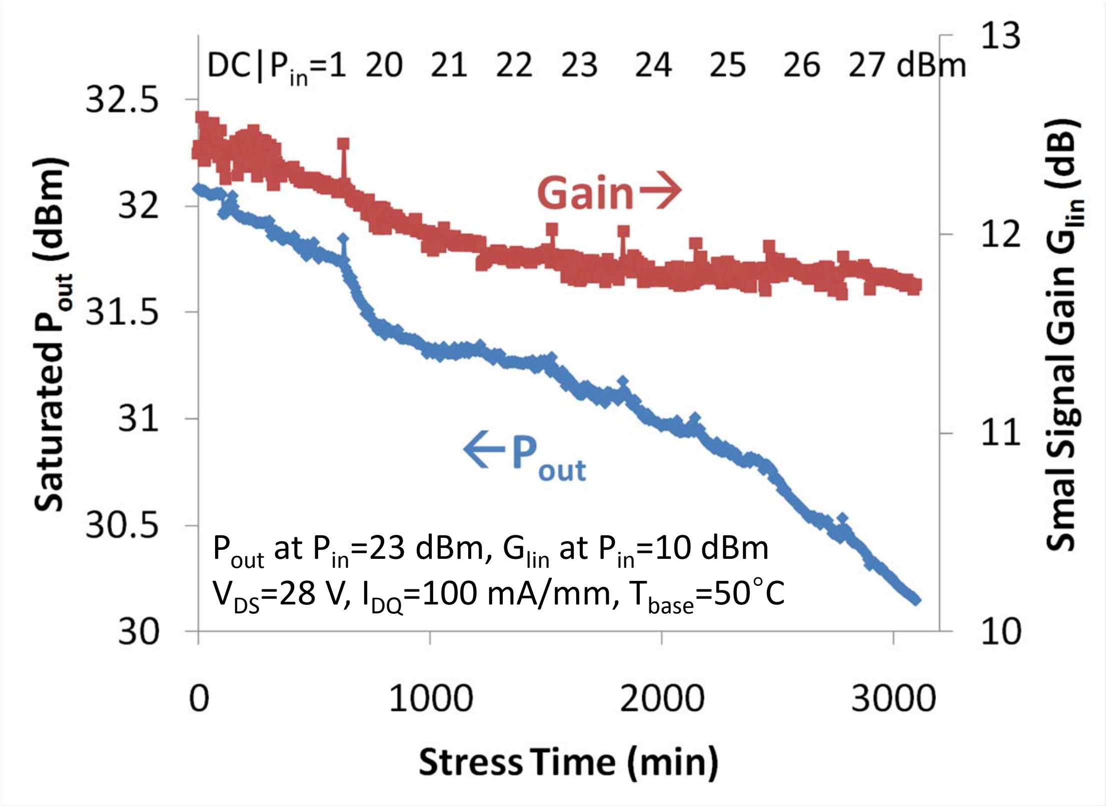
YES

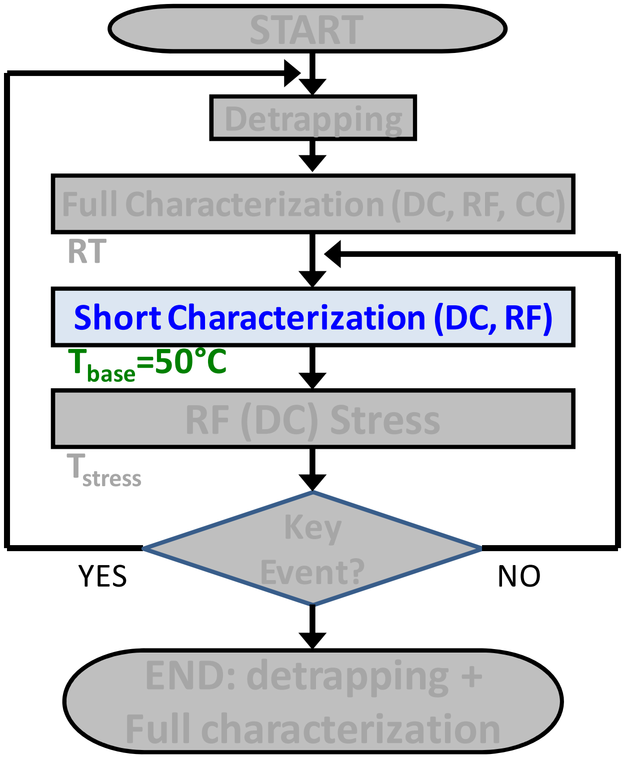
NO

END: detrapping + Full characterization

- P_{in} changing → RF FOMs changing
- Degradation apparent but not easily quantifiable

RF FOM during short characterization




START

Detrapping

Full Characterization (DC, RF, CC)

RT

Short Characterization (DC, RF)

T_{base}=50°C

RF (DC) Stress

T_{stress}

Key Event?

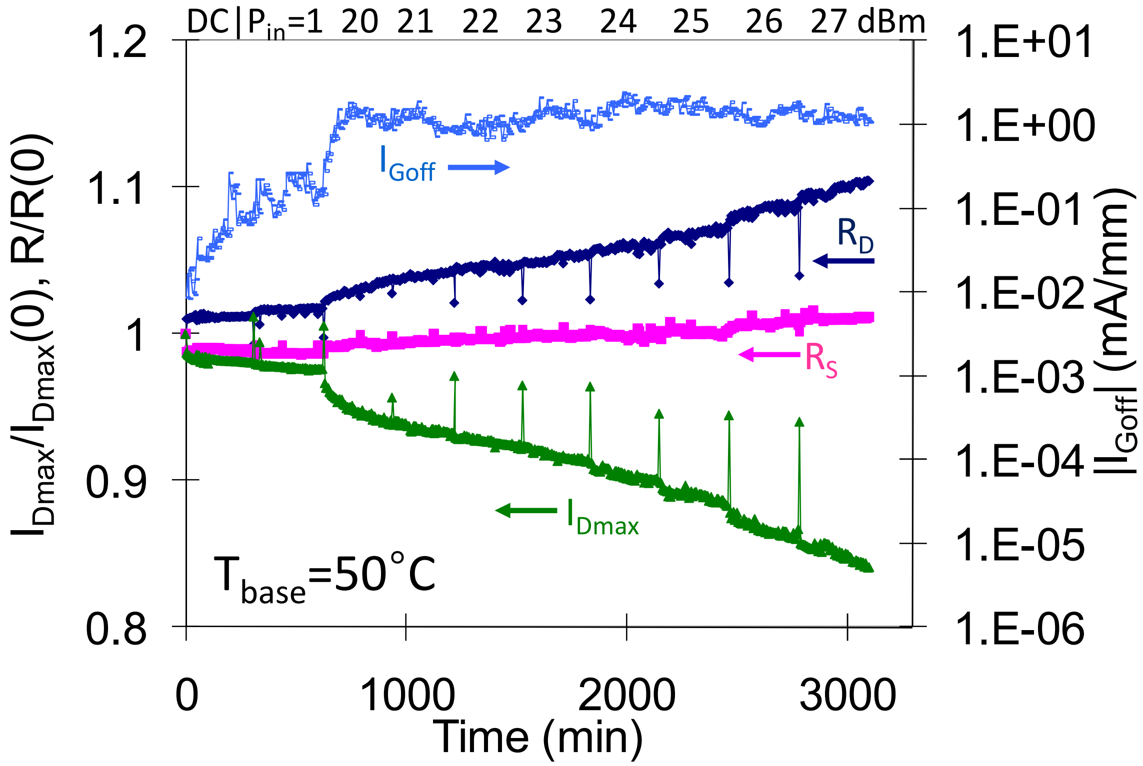
YES

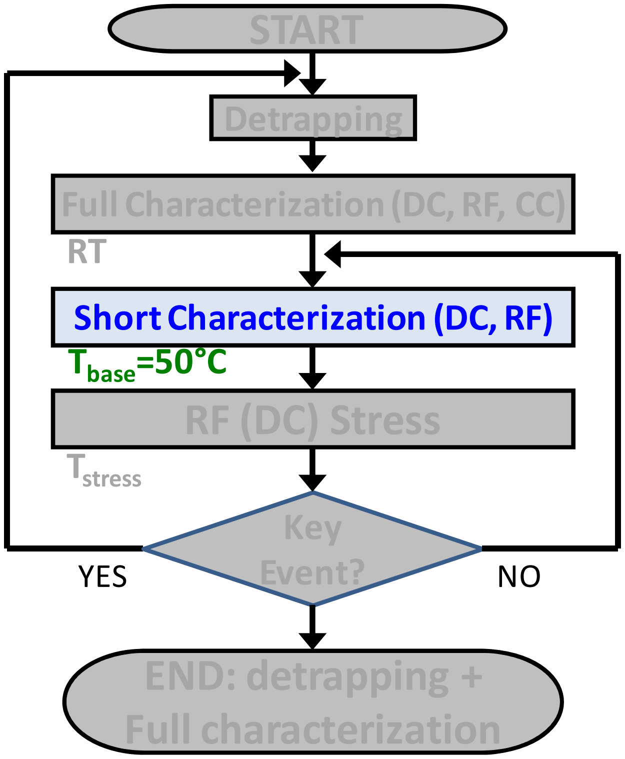
NO

END: detrapping + Full characterization

- Mild degradation under DC and low P_{in}
- Adding RF increases degradation: P_{in} ↑ → P_{out} ↓

DC FOM during short characterization





START

Detrapping

Full Characterization (DC, RF, CC)

RT

Short Characterization (DC, RF)

T_{base}=50°C

RF (DC) Stress

T_{stress}

Key Event?

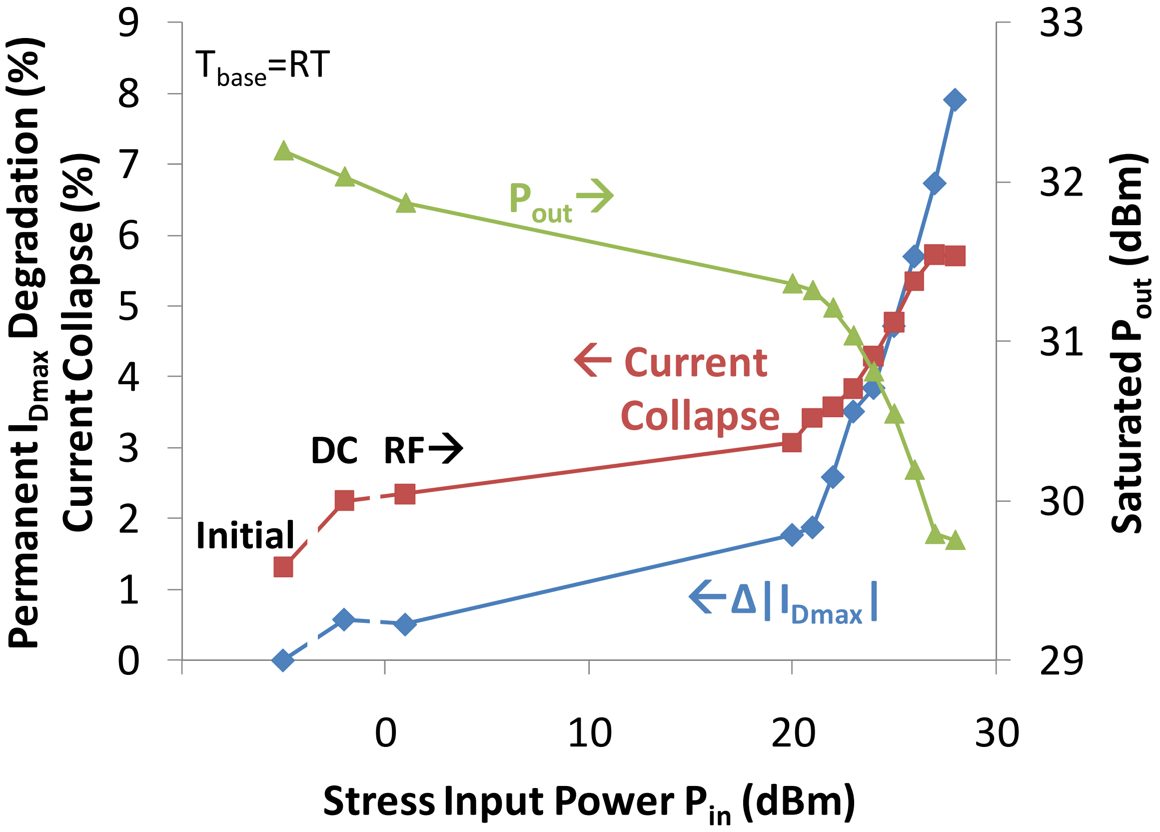
YES

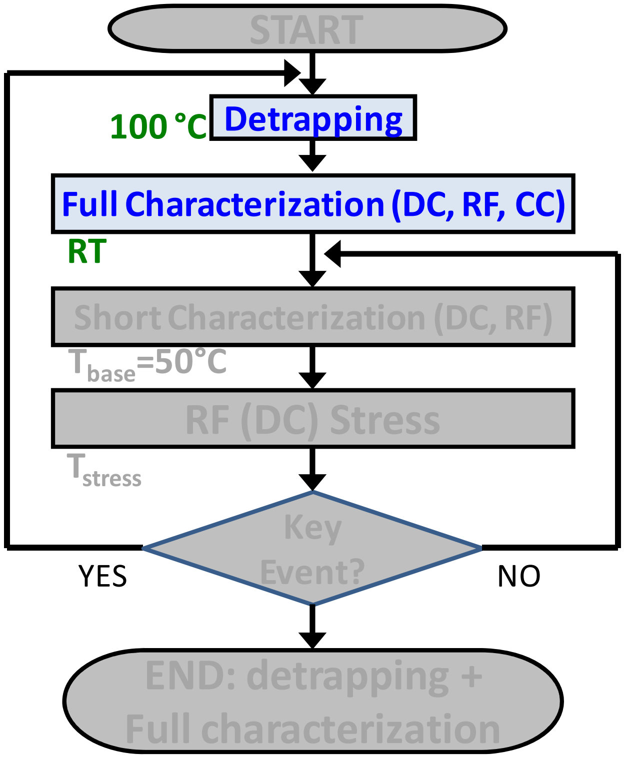
NO

END: detrapping + Full characterization

- Mild degradation under DC and low P_{in}
- At P_{in}=20 dBm, step degradation in I_{Goff}
- Beyond P_{in}=20 dBm, increasing degradation of I_{Dmax} and R_D

DC/RF/CC full characterization




START

100 °C **Detrapping**

Full Characterization (DC, RF, CC)

RT

Short Characterization (DC, RF)

T_{base}=50°C

RF (DC) Stress

T_{stress}

Key Event?

YES

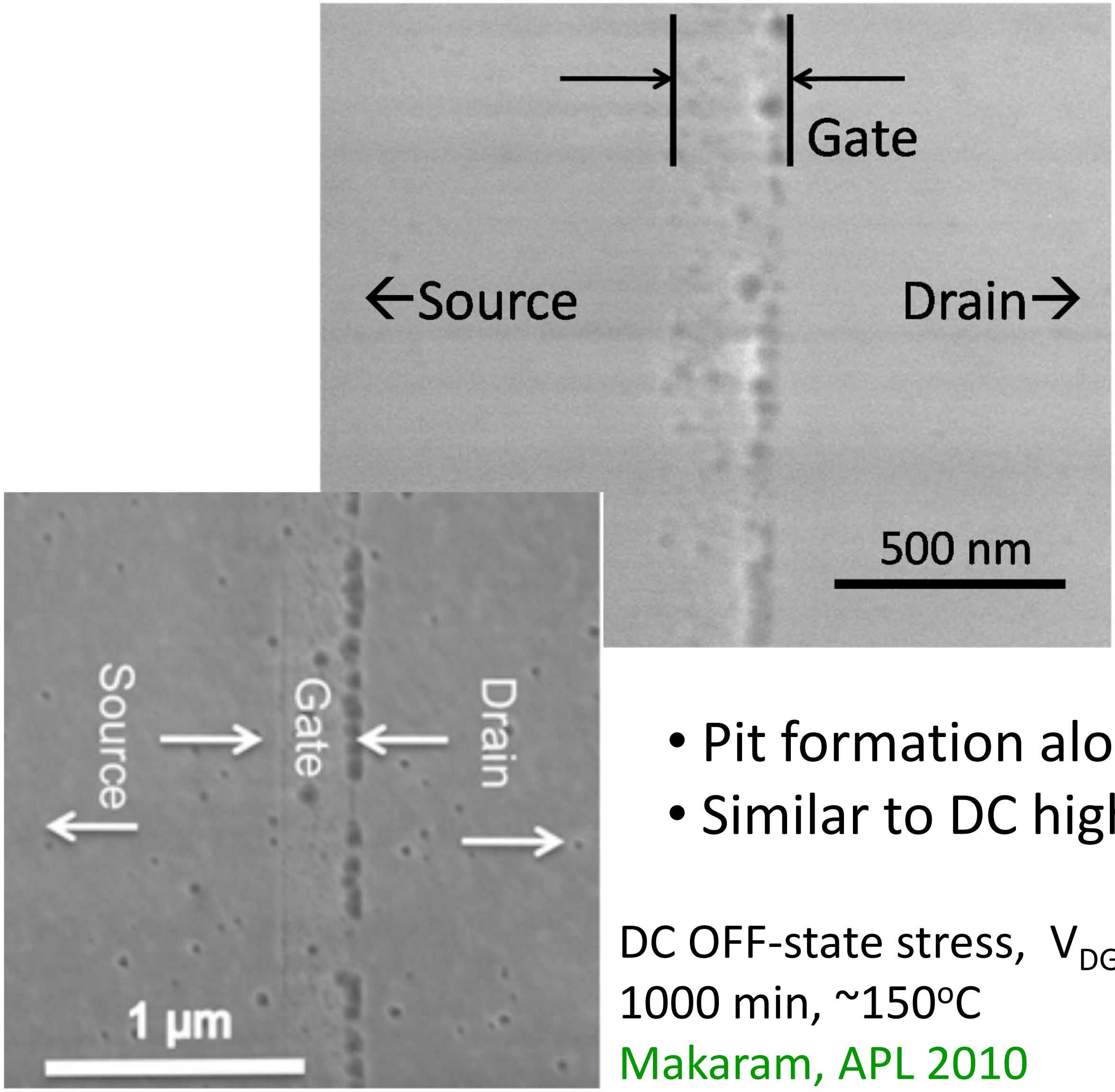
NO

END: detrapping + Full characterization

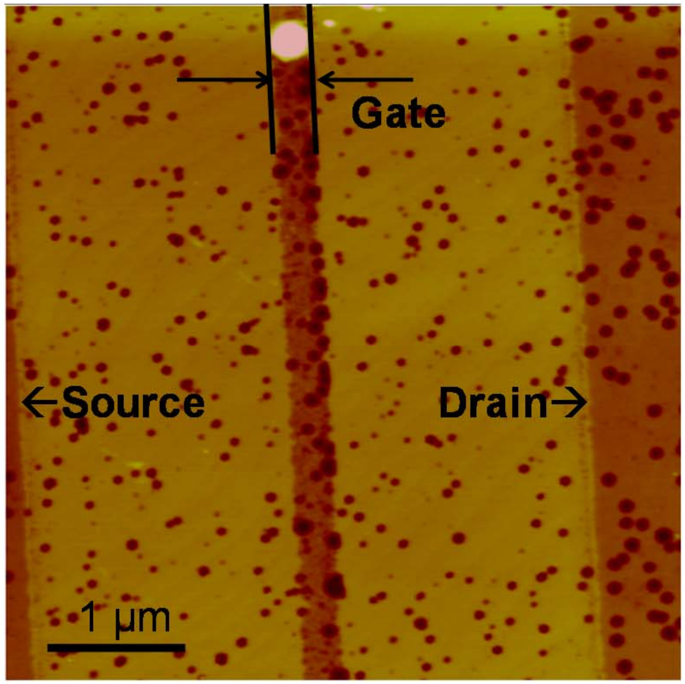
- Beyond P_{in}=20 dBm:
  - Sharp P_{out} degradation
  - Permanent degradation of I_{Dmax}
  - Increased CC → evidence of new trap creation

Structural degradation (planar view)

SEM



AFM



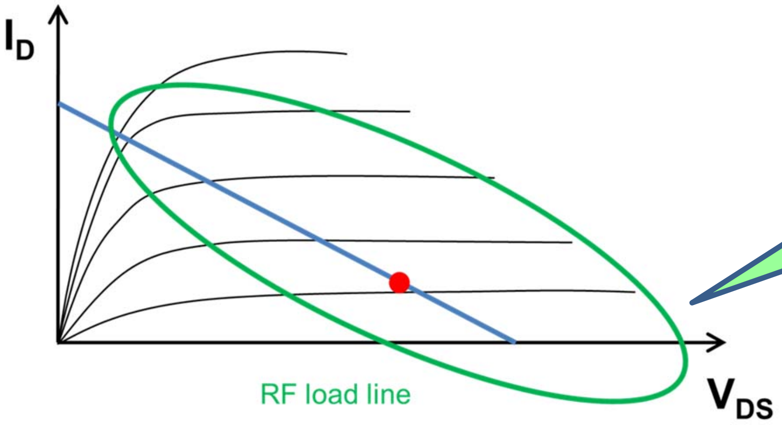
- Pit formation along drain end of gate edge
- Similar to DC high voltage OFF-state stress

DC OFF-state stress, V_{DG}=50 V,
1000 min, ~150^{o}C
Makaram, APL 2010

HV OFF-state DC *vs.* RF power degradation

Similar pattern of degradation:

	HV OFF-state DC	**RF power**
I_{Dmax}	↓ beyond V_{crit}	↓ beyond $P_{in\text{-}crit}$
R_D	↑ beyond V_{crit}	↑ beyond $P_{in\text{-}crit}$
R_S	small increase	small increase
I_{Goff}	↑ beyond V_{crit}	↑ beyond $P_{in\text{-}crit}$
Current Collapse	↑ beyond V_{crit}	↑ beyond $P_{in\text{-}crit}$
Permanent I_{Dmax}	↓ beyond V_{crit}	↓ beyond $P_{in\text{-}crit}$
Pits under drain end of gate	Yes	Yes
Pits under source end of gate	No	No

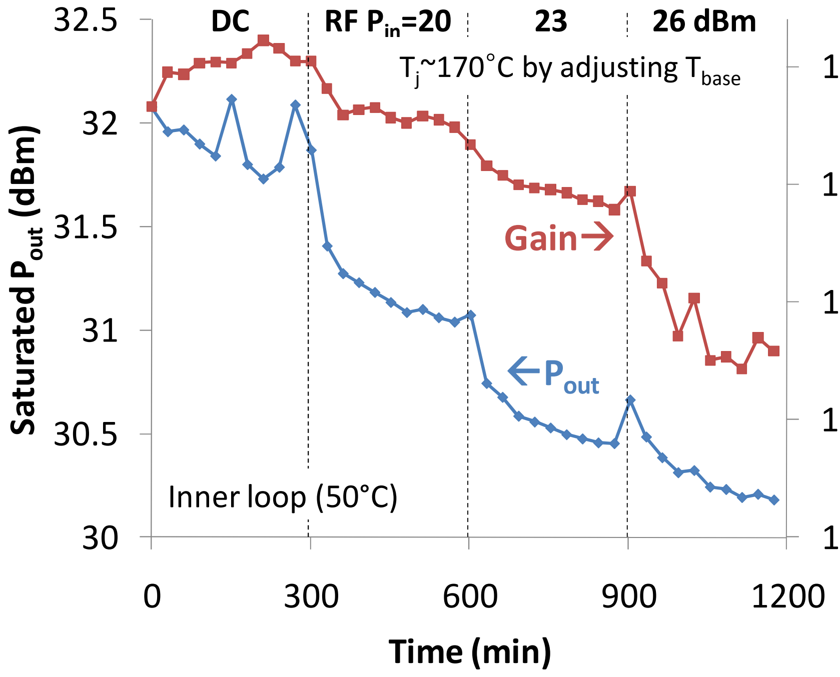


High V end of load line responsible for degradation

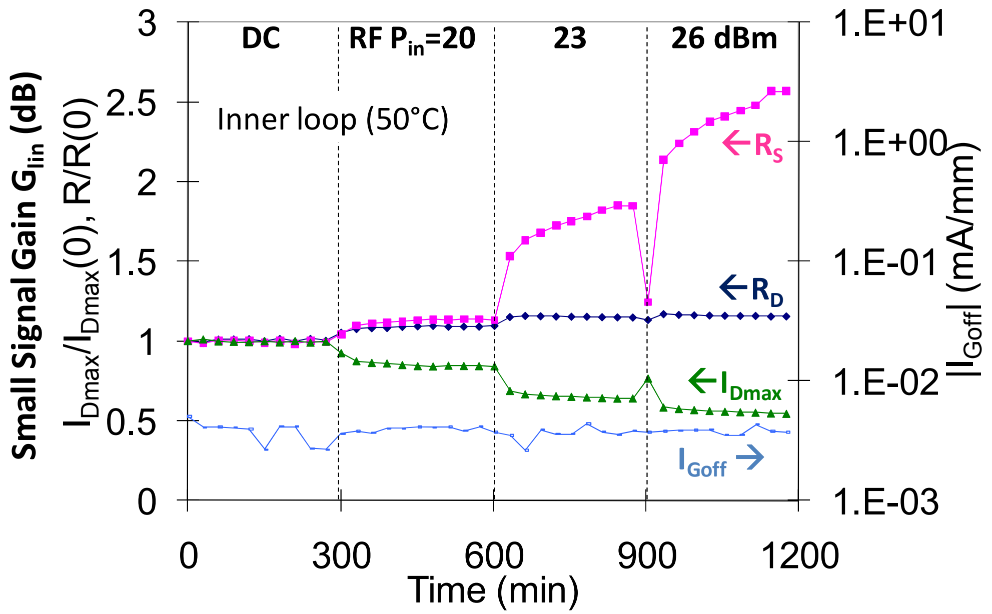
Step P_{in} stress: *Offset Gate*

Offset gate devices (L_{GS}<L_{GD}): OFF-state V_{crit} > 80 V at T=150°C

RF FOMs



DC FOMs



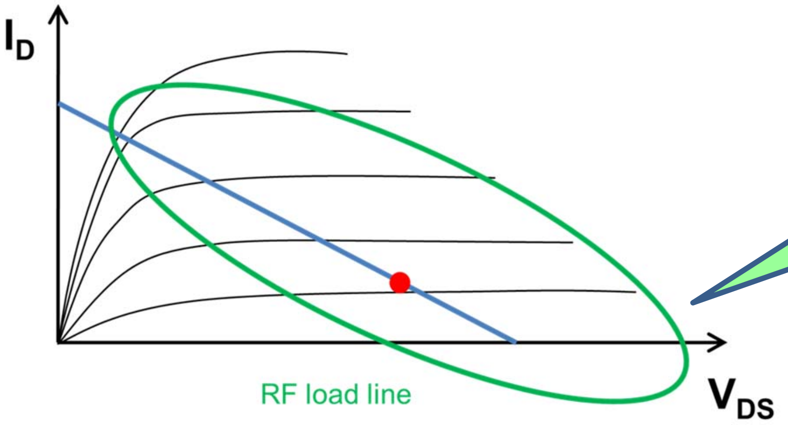
Joh, IEDM 2010

- Increased degradation under high P_{in}
- No I_{Goff} degradation
- Degradation of I_{Dmax} **and R_S**, not R_D

HV OFF-state DC *vs.* RF power degradation

Different pattern of degradation:

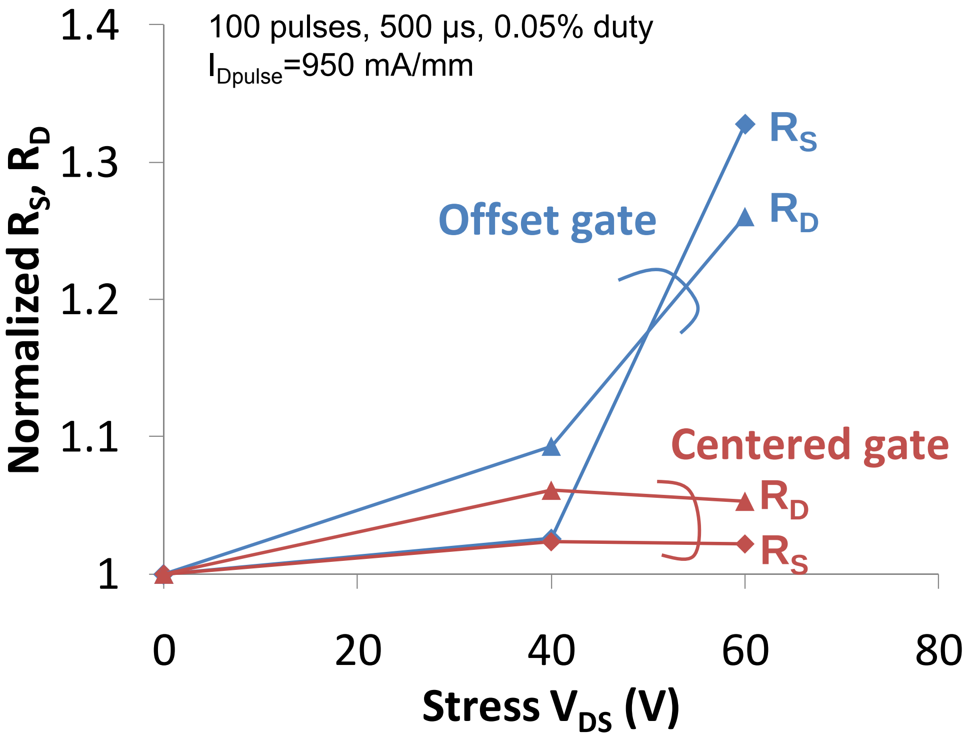
	HV OFF-state DC	**RF power**
I_{Dmax}	↓ beyond V_{crit}	↓ beyond $P_{in\text{-}crit}$
R_D	↑ beyond V_{crit}	↑ beyond $P_{in\text{-}crit}$
R_S	small increase	**↑↑ beyond $P_{in\text{-}crit}$**
I_{Goff}	↑ beyond V_{crit}	**No**
Current Collapse	↑ beyond V_{crit}	↑ beyond $P_{in\text{-}crit}$
Permanent I_{Dmax}	↓ beyond V_{crit}	↓ beyond $P_{in\text{-}crit}$
Pits under drain end of gate	Yes	**No**
Pits under source end of gate	No	No



High V end of load line **NOT** responsible for degradation

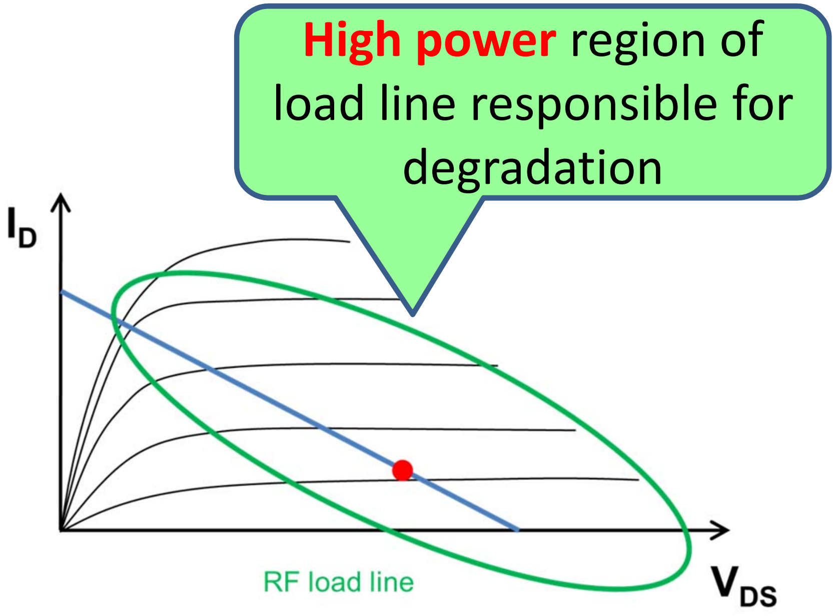
High-power pulsed stress

- High-power stress not accessible in DC → pulsed stress
- Offset-gate and centered-gate devices on same wafer:



100 pulses, 500 μs, 0.05% duty

I_{Dpulse}=950 mA/mm



High power region of load line responsible for degradation

- Pulsed stress reproduces R_S degradation in offset gate device
- No R_S degradation in centered gate

Summary

- New RF reliability testing methodology developed
- Under RF stress, degradation worse than at DC bias point
- Different patterns of RF degradation observed:
  - In some device designs, it reproduces HV OFF-state DC degradation (field driven)
  - In other device designs, degradation pattern correlates with high-power pulsed stress (power driven?)

→ DC reliability not good predictor for RF reliability

→ Need for fundamental studies of RF reliability