Analytical Model for RF Power Performance of Deeply Scaled CMOS Devices

Usha Gogineni[1], Jesús del Alamo[1], and Alberto Valdes-Garcia[2]

[1]Massachusetts Institute of Technology, Cambridge, MA, [2] IBM T.J. Watson Research Center

***Abstract* — This paper presents a first order model for RF power of deeply scaled CMOS. The model highlights the role of device on-resistance in determining the maximum RF power. We show excellent agreement between the model and the measured data on 45 nm CMOS devices across a wide range of device widths, under both maximum output power and maximum PAE conditions. The model allows circuit designers to quickly estimate the power and efficiency of a device layout without need for complicated compact models or simulations.**

***Index Terms* — CMOS, power amplifiers, millimeter wave, on-resistance, PAE.**

I. Introduction

Estimating the maximum RF output power for a device at any given bias point is an onerous task. Power amplifier designers often rely on RF power simulations using compact device models [1-2]. These simulations are very time consuming and the need for accurate compact models means that the power estimations are only accurate when designing in mature device technologies. Moreover, in the case of CMOS, compact models are usually tailored for digital or analog applications and hence are not accurate enough for modeling the device behavior under the large signal swings characteristic of RF power applications. Also, power simulations around the peak PAE point often lead to convergence issues and hence do not predict the peak power very well [3].

In view of all the challenges described above, it would be ideal to have a simple analytical model that can predict the maximum output power and the trade-off between output power and PAE in a device. The analytical models presented in textbooks [4-10] usually ignore R_{on} and also assume zero V_{DSsat}. However, to obtain high power, the device is usually biased at a high drain current, which means the output power is strongly affected by R_{on}. In this paper, we present an analytical model that correctly accounts for the on-resistance of the device, thus allowing us to make quick back-of-the-envelope predictions of the output power and PAE. We validate the model by comparing the power and efficiency predictions from the model with measured load-pull data on 45 nm CMOS devices.

II. Model Description

The power amplifier model used in this paper is based on the overdriven class AB amplifier discussed in [4] (Fig. 1). The transistor is characterized by a threshold voltage V_t and an on-resistance R_{on}. It is biased at an operating point (V_{GQ}, V_{DQ}). The current through the drain in the absence of RF input signal is I_{DQ}. The RF load consists of a fundamental load resistor R_L, and a shunt connected "tank" circuit with its resonant frequency at the fundamental frequency of operation (f_o). All harmonics in the load current are assumed to be shorted by the tank circuit and generate no voltage. Hence, the current flowing through R_L is just the first harmonic, i_1, and the voltage across R_L is assumed to be sinusoidal with a magnitude set by the load resistor.

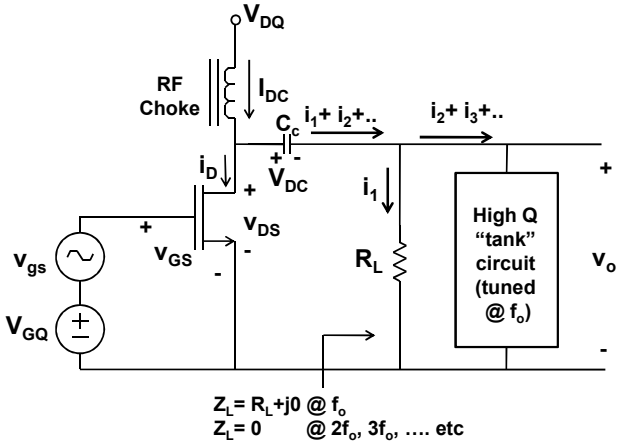

Fig. 1: Circuit diagram of a reduced conduction angle RF power amplifier.

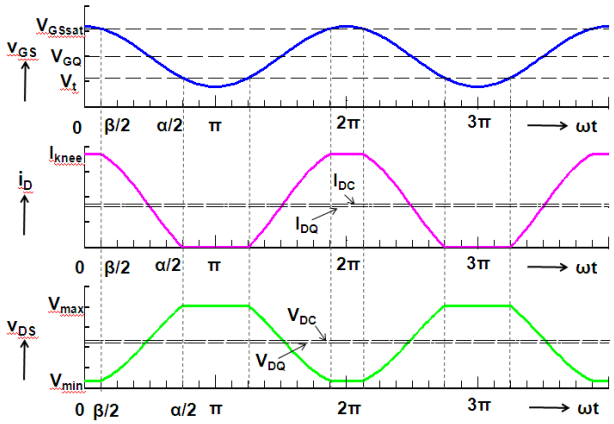

Fig. 2: Waveforms for input voltage and output current and voltage in the reduced conduction angle amplifier of Fig. 1.

Fig. 2 shows the waveforms for key voltages and currents in the power amplifier when operated in the maximum power condition for a certain bias point and load resistance. When $v_{GS} < V_t$, the device enters the cut-off regime and the drain current is zero. When $v_{GS} > V_{GSsat}$, the device enters the linear regime and the drain current is clipped at I_{knee}. For all other values of v_{GS}, the drain current is assumed to be cosinusoidal. The shape of the drain voltage waveform is 180 degrees out of phase with the drain current waveform. When $i_D = I_{knee}$, v_{DS} is pinned at the minimum value V_{min}, and when $i_D = 0$, the drain voltage is clipped at V_{max}.

α denotes the conduction angle and represents the proportion of the RF cycle for which $v_{GS} > V_t$ and $i_D > 0$. Since the waveform is symmetric about $\omega t = 0$, the current cut-off points are at $\omega t = \pm\alpha/2$. β denotes the proportion of the RF cycle for which $v_{GS} > V_{GSsat}$ and $i_D = I_{knee}$.

Assuming that the drain current and voltage follow a pure cosine between $\alpha/2$ and $\beta/2$, we can write:

$$i_D(\omega t) = \begin{cases} I_{knee} & 0 \le |\omega t| \le \frac{\beta}{2} \\ I_{DQ} + I_d \cos \omega t & \frac{\beta}{2} \le |\omega t| \le \frac{\alpha}{2} \\ 0 & \frac{\alpha}{2} \le |\omega t| \le \pi \end{cases} \quad (1)$$

$$v_{DS}(\omega t) = \begin{cases} V_{min} & 0 \le |\omega t| \le \frac{\beta}{2} \\ V_o + V_d \cos \omega t & \frac{\beta}{2} \le |\omega t| \le \frac{\alpha}{2} \\ V_{max} & \frac{\alpha}{2} \le |\omega t| \le \pi \end{cases} \quad (2)$$

The values of I_{knee}, I_d, V_o and V_d can be determined by recognizing that the waveforms need to be continuous at $\alpha/2$ and $\beta/2$.

V_{min} can be expressed in terms of I_{knee} and R_{on} as:

$$V_{min} = I_{knee} R_{on} \quad (3)$$

Our model describes the maximum power situation for any given value of α and β. Hence, we assume a maximum voltage swing for v_{DS} that is symmetric about V_{DQ}. In other words,

$$V_{max} - V_{min} = 2(V_{DQ} - V_{min}) \quad (4)$$

This assumption is widely made in the analysis of power amplifiers [4, 6, 8].

The magnitudes of the DC and fundamental component of the drain current and voltage can be obtained by Fourier analysis of equations (1) and (2):

$$I_{DC} = \frac{I_{DQ}}{\pi \cos\frac{\alpha}{2}} \left[\frac{\beta}{2} \left(\cos\frac{\alpha}{2} - \cos\frac{\beta}{2} \right) + \frac{(\alpha - \beta)}{2} \cos\frac{\alpha}{2} - \left(\sin\frac{\alpha}{2} - \sin\frac{\beta}{2} \right) \right] \quad (5)$$

$$I_1 = \frac{2I_{DQ}}{\pi \cos\frac{\alpha}{2}} \left[\sin\frac{\beta}{2} \left(\cos\frac{\alpha}{2} - \cos\frac{\beta}{2} \right) - \frac{(\sin\alpha - \sin\beta)}{4} + \cos\frac{\alpha}{2} \left(\sin\frac{\alpha}{2} - \sin\frac{\beta}{2} \right) - \frac{(\alpha - \beta)}{4} \right] \quad (6)$$

$$V_{DC} = \frac{1}{\pi} \left[V_{min} \frac{\beta}{2} + \frac{\left(V_{min} \cos\frac{\alpha}{2} - V_{max} \cos\frac{\beta}{2} \right)(\alpha - \beta)}{2\left(\cos\frac{\alpha}{2} - \cos\frac{\beta}{2} \right)} + \frac{(V_{max} - V_{min}) \left(\sin\frac{\alpha}{2} - \sin\frac{\beta}{2} \right)}{\left(\cos\frac{\alpha}{2} - \cos\frac{\beta}{2} \right)} + V_{max} \left(\pi - \frac{\alpha}{2} \right) \right] \quad (7)$$

$$V_1 = \frac{2}{\pi} \left[V_{min} \sin\frac{\beta}{2} + \frac{(V_{max} - V_{min})(\alpha - \beta)}{4\left(\cos\frac{\alpha}{2} - \cos\frac{\beta}{2} \right)} + \frac{\left(V_{min} \cos\frac{\alpha}{2} - V_{max} \cos\frac{\beta}{2} \right) \left(\sin\frac{\alpha}{2} - \sin\frac{\beta}{2} \right)}{\left(\cos\frac{\alpha}{2} - \cos\frac{\beta}{2} \right)} + \frac{(V_{max} - V_{min})(\sin\alpha - \sin\beta)}{4\left(\cos\frac{\alpha}{2} - \cos\frac{\beta}{2} \right)} - V_{max} \sin\frac{\alpha}{2} \right] \quad (8)$$

The fundamental component of the drain voltage is the same as the voltage across the load resistor. This is, because we assumed that V_{DC} drops across the capacitor C_c and that the second and higher order harmonics are shorted out at the fundamental frequency of operation.

The output power, efficiency, and fundamental load resistance values that are associated with a particular choice of α and β can then be directly computed using the following expressions:

$$P_{DC} = V_{DQ} \cdot I_{DC} \quad (9)$$

$$P_{out} = \frac{I_1}{\sqrt{2}} \cdot \frac{V_1}{\sqrt{2}} \quad (10)$$

$$\eta_D\ (\%) = \frac{P_{out} * 100}{P_{DC}} \quad (11)$$

$$R_L = \frac{V_{max} - V_{min}}{I_{knee}} \quad (12)$$

The model equations presented above can be used to generate the drain efficiency – output power locus for any given device. The inputs to the model are the DC operating point (V_{DQ}, I_{DQ}) and R_{on} of the device. For any given value of α and β, describing a random maximum power condition, the value of output power, drain efficiency, average current and load resistance can be computed using the above expressions. This exercise is repeated for multiple pairs of α and β to construct the drain efficiency – output power locus.

An example is shown in Fig. 3 for a device with R_{on} = 9.6 Ω biased at V_{DQ} = 1.1 V and I_{DQ} = 200 mA/mm. R_{on} was calculated from measured DC data as V_{DS}/I_D with V_{DS} = 50 mV. For any given α, as β is increased, more of the current waveform gets clipped at I_{knee}, and more of the voltage waveform gets clipped at V_{min}. This leads to a decrease in the peak of the current waveform and a corresponding increase in the peak of the voltage waveform. In turn, this results in a decrease in I_{DC} and I_1 and a corresponding increase in V_{DC} and V_1. Since P_{out} =

$I_1V_1/2$, as β increases, P_{out} initially increases because of the rise in V_1, but then starts decreasing as the reduction in I_1 begins to dominate. On the other hand, since I_{DC} decreases with increasing β, the drain efficiency increases monotonically. As α decreases towards class B operation (α = π), the peak of the current waveform increases, thus leading to higher power.

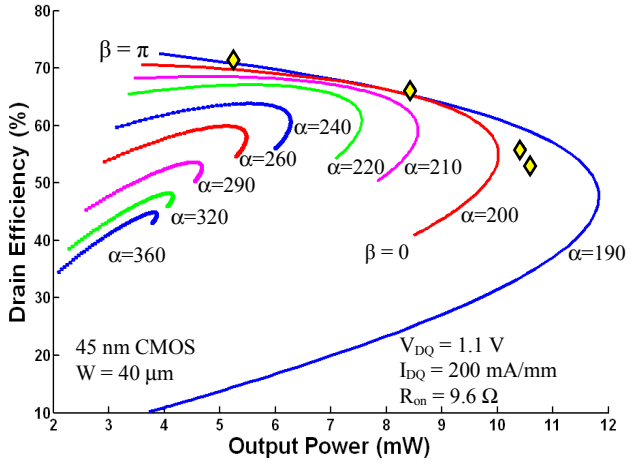

Fig. 3: Modeled locus of drain efficiency versus output power. P_{out} and η_D measurements at different R_L are shown as symbols in the figure and show good agreement with the model.

III. COMPARISON WITH MEASUREMENTS

The devices used in this study were fabricated using IBM's 45 nm low-power CMOS process [11]. The test devices have a gate length of 40 nm and are designed to operate at V_{DD}=1.1 V. Devices with gate widths between 40 µm and 640 µm were fabricated by connecting multiple unit cells in parallel. Each unit cell contains 20 fingers of 2 µm finger width. RF power measurements were performed in the 2 – 18 GHz range using a Maury Microwave load-pull system. Power measurements for all devices were performed at $V_{DS} = V_{DD}$, and V_{GS} set to yield a DC drain current density I_{DQ} = 200 mA/mm under low input power conditions. The output power and PAE were recorded at an input power level corresponding to the peak PAE condition. The source and load impedances were tuned for either (a) maximum P_{out}, or (b) maximum PAE. f_{max} for these devices, at the bias point under consideration, ranged from 200 GHz in the narrow devices to 100 GHz in the widest device. We found that the output power measured on the 45 nm devices is independent of frequency in the 2-18 GHz range [12]. Therefore, for $f << f_{max}$, the frequency dependence is smaller than the influence of other factors, and hence has been ignored in this work.

The RF power data measured on a W = 40 µm device at several R_L values is shown along with the model data in Fig. 3. The measured data shows reasonable agreement with the modeled locus.

The modeled $\eta_D - P_{out}$ locus can be used to predict the maximum output power a device can deliver at a given drain efficiency, or vice versa. Fig. 4 shows the measured η_D (symbols) and the values chosen as input to the model (solid lines) for the two different impedance matching conditions (optimized power and optimized PAE). The appropriate R_{on} and DC operating points were used in the model for each device.

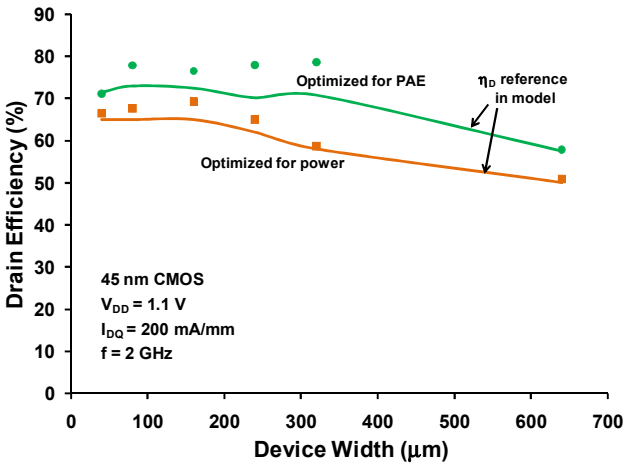

Fig. 4: Drain Efficiency as a function of device width. The solid line represents η_D selected as reference in the model for predicting maximum P_{out} and optimum R_L for that η_D. The symbols are the measured η_D at 2 GHz.

The model assumes that only the first harmonic of the drain current flows through the load resistance and that all the other harmonics are shorted out through perfect impedance matching at the fundamental frequency. However, in practice the impedance match need not be perfect and could yield non-zero values of second and higher order harmonics of the current. This would result in an increased value of the output power and drain efficiency. This explains why the maximum modeled drain efficiency was less than the measured values for some of the devices. In such cases, the maximum modeled efficiency closest to the measured value was selected as input to calculate the maximum P_{out}.

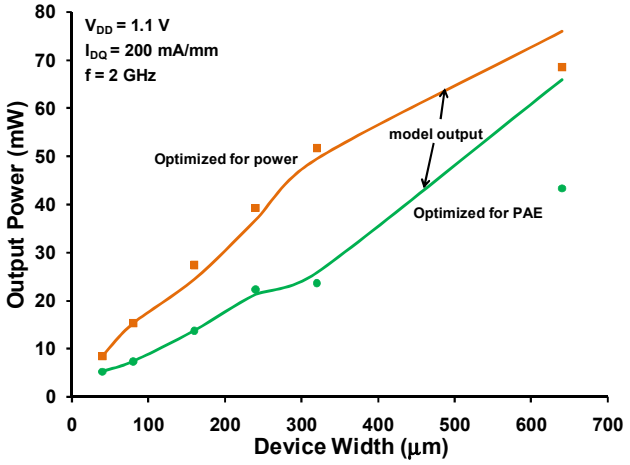

Fig. 5: Output power as a function of device width. The solid line represents the maximum P_{out} predicted by the model. The symbols show the measured P_{out} at 2 GHz.

For each value of drain efficiency chosen as input, the maximum possible power predicted by the model, for any combination of α and β values, is recorded. The corresponding values of alpha and beta are also noted and are used to calculate the average drain current and the load resistance.

Fig. 5 shows the modeled values for maximum output power and the measured data, across all device widths. The excellent agreement suggests that the maximum output power delivered by a device at any given bias point is only limited by the on-resistance of the device. The device capacitances play a role in degrading the PAE of the device. However, as long as extra input power can be provided to charge the capacitors, one can always obtain the same maximum power.

The measured P_{out} on the 640 µm device is significantly lower than the modeled value (Fig. 5). This could be because of self-heating effects, which become significant in the wide devices. The self heating explanation is further borne out in Fig. 6, where the modeled and measured values of the average drain current (I_{DC}) are shown as a function of device width. In general, the modeled I_{DC} closely matches the measured values, thus validating the model. The measured I_{DC} on the 640 µm device is somewhat lower than the modeled value, also consistent with self heating.

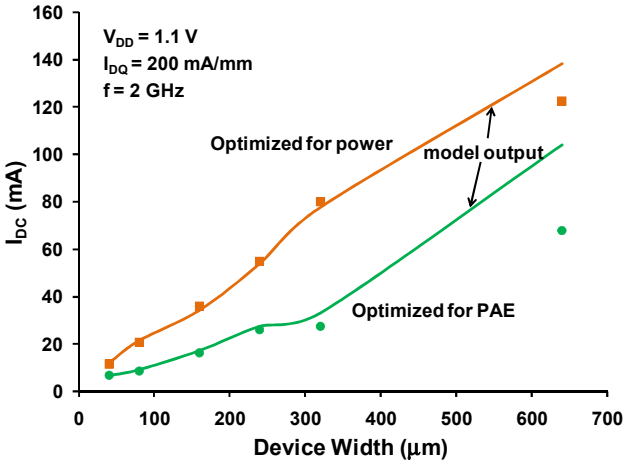

Fig. 6: Average drain current as a function of device width. The solid line represents I_{DC} predicted by the model. The symbols show the measured I_{DC} at 2 GHz.

Fig. 7 shows the load resistance used in the power measurements (symbols), as well as the value of R_L computed from the model (solid lines). The modeled values show reasonable agreement with the measurements. This means designers can use this model to not only predict the maximum output power of a device for any given drain efficiency, but also to estimate the load resistance needed to achieve the required power. Output matching networks can then be designed to present this resistance to the load.

In a CMOS device, R_{on} can be approximated as the sum of the source resistance (R_S) and drain resistance (R_D), since the channel resistance is typically much smaller than R_D or R_S. Hence, if we can estimate R_D and R_S for any device layout, through parasitic extractions from layout, we can predict the maximum P_{out} and η_D for that device. Thus, using this model, circuit designers can estimate the power capability of their designs and optimize the design to achieve the necessary power or efficiency targets.

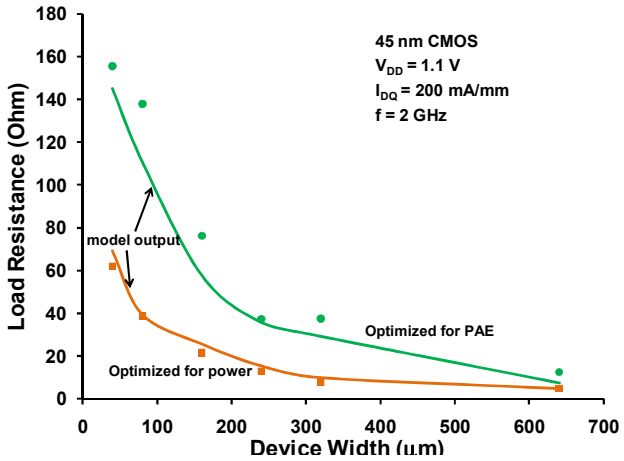

Fig. 7: Load resistance needed to obtain maximum P_{out}. Solid line is optimum R_L predicted by model. Symbols are measured data at 2 GHz.

IV. CONCLUSION

A simple analytical model for the RF output power and drain efficiency of CMOS has been presented. The model uses the DC operating point and on-resistance of the device as inputs and gives out the maximum output power and the load resistance at any value of the drain efficiency. We have shown that the modeled values of P_{out}, η_D, and R_L show excellent agreement with the measured data on 45 nm CMOS devices across a wide range of device widths. Our work shows that on-resistance is the most significant limiter to the output power of CMOS devices. Circuit designers can use this model to estimate the power and efficiency of their device and to optimize their device layout to meet performance targets.

ACKNOWLEDGEMENT

This work was funded by a Semiconductor Research Corporation (SRC) grant 2007-HJ-1661. The authors would like to thank IBM Microelectronics for fabricating the test structures.

REFERENCES

[1] S. Aloui, *et al.*, "A 60GHz 13 dBm fully integrated 65 nm RF CMOS power amplifier", *NEWCAS-TAISA*, 2008, pp: 237-240.
[2] N. Kurita, *et al.*, "60GHz and 80GHz wide band power amplifier MMICs in 90nm CMOS technology", *RFIC*, 2009, pp: 39-42.
[3] P. Estrada, "Overcoming verification tool limitations for analog / RF designs", *EE Times Design*, 2007.
[4] S. C. Cripps, *RF Power Amplifiers for Wireless Communications*, 2006.
[5] B. J. Baliga, *Silicon RF Power MOSFETs*, 2005.
[6] M. K. Kazimierczuk, *RF Power Amplifiers*, 2008.
[7] D. M. Pozar, *Microwave Engineering*, 1998.
[8] J. L. B. Walker, *High-Power GaAs FET Amplifiers*, 1993.
[9] M. Albulet, *RF Power Amplifiers*, 2001.
[10] A. Grebennikov, *RF and Microwave Power Amplifier Design*, 2005.
[11] J. Yuan, *et al.*, "A 45 nm low cost low power platform by using integrated dual-stress-liner technology," *VLSI Technology Symposium*, 2006, pp. 100-101.
[12] U. Gogineni, *et al.*, "RF power potential of 45 nm CMOS technology," *SiRF, 2010*, pp. 204-207.