RMO4A

Analytical Model for RF Power Performance of Deeply Scaled CMOS Devices

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Outline

- Motivation
- Technology and Measurement Details
- Effect of R_{on} on Maximum P_{out}
- Analytical Model Description
- Comparison of Model with Measurements
- Conclusions

Motivation

P_{outmax} often estimated through RF power simulations

- Time consuming
- Need accurate compact models
- CMOS models usually tailored for digital applications

Need an analytical model that can

- Provide physical understanding of basics of power scaling
- Estimate power capability of a device without need for complex models or simulations

Pros & Cons of Analytical Model

Pros:

- Predicts P_{outmax} and trade-off between P_{out} and PAE
- Correctly accounts for R_{on} of the device
- No need for complex models or simulations

Limitations:

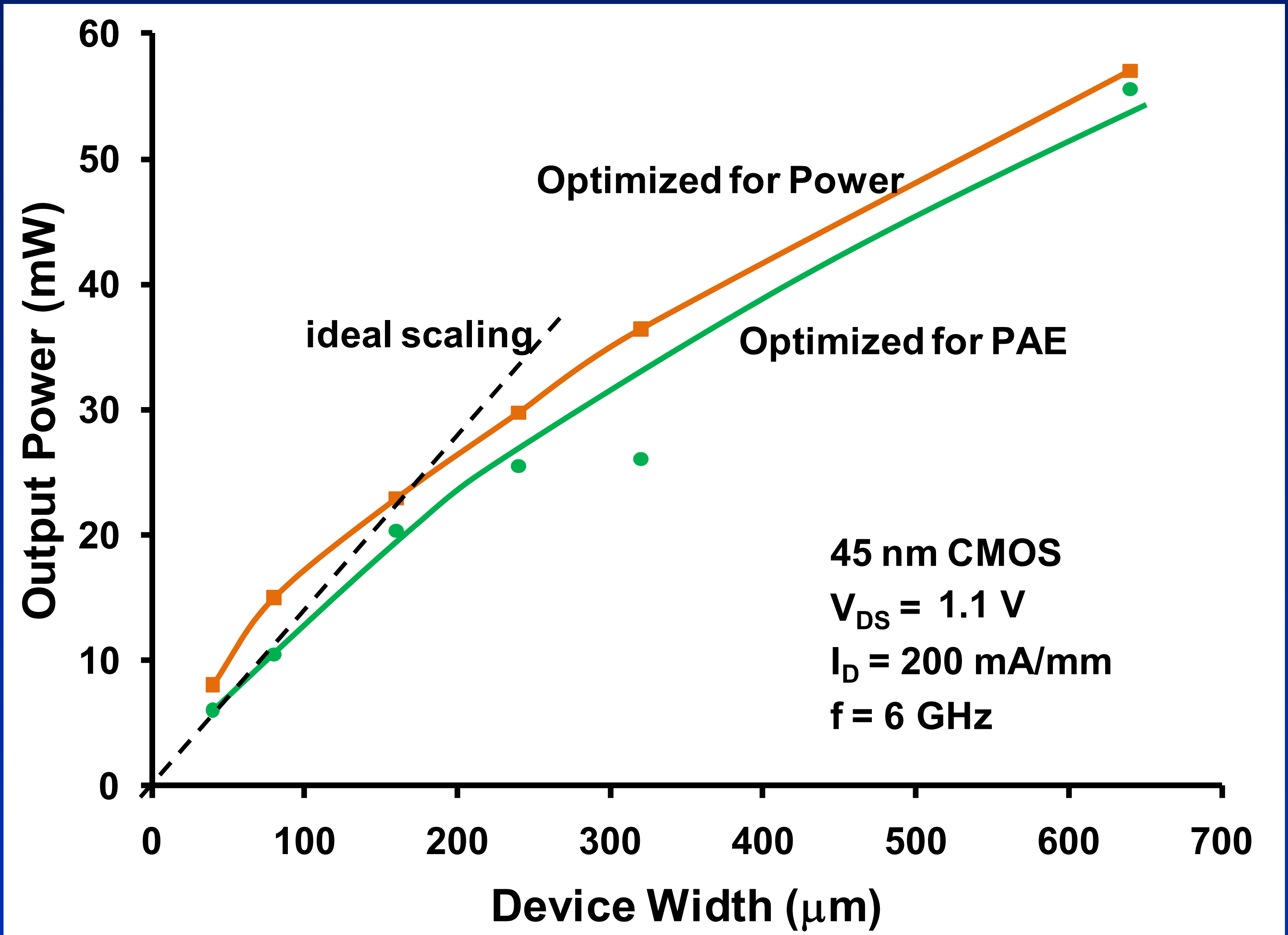
- Frequency dependence is ignored

(for 2-18 GHz, the measured P_{out} is independent of f)

Technology & Measurement Details

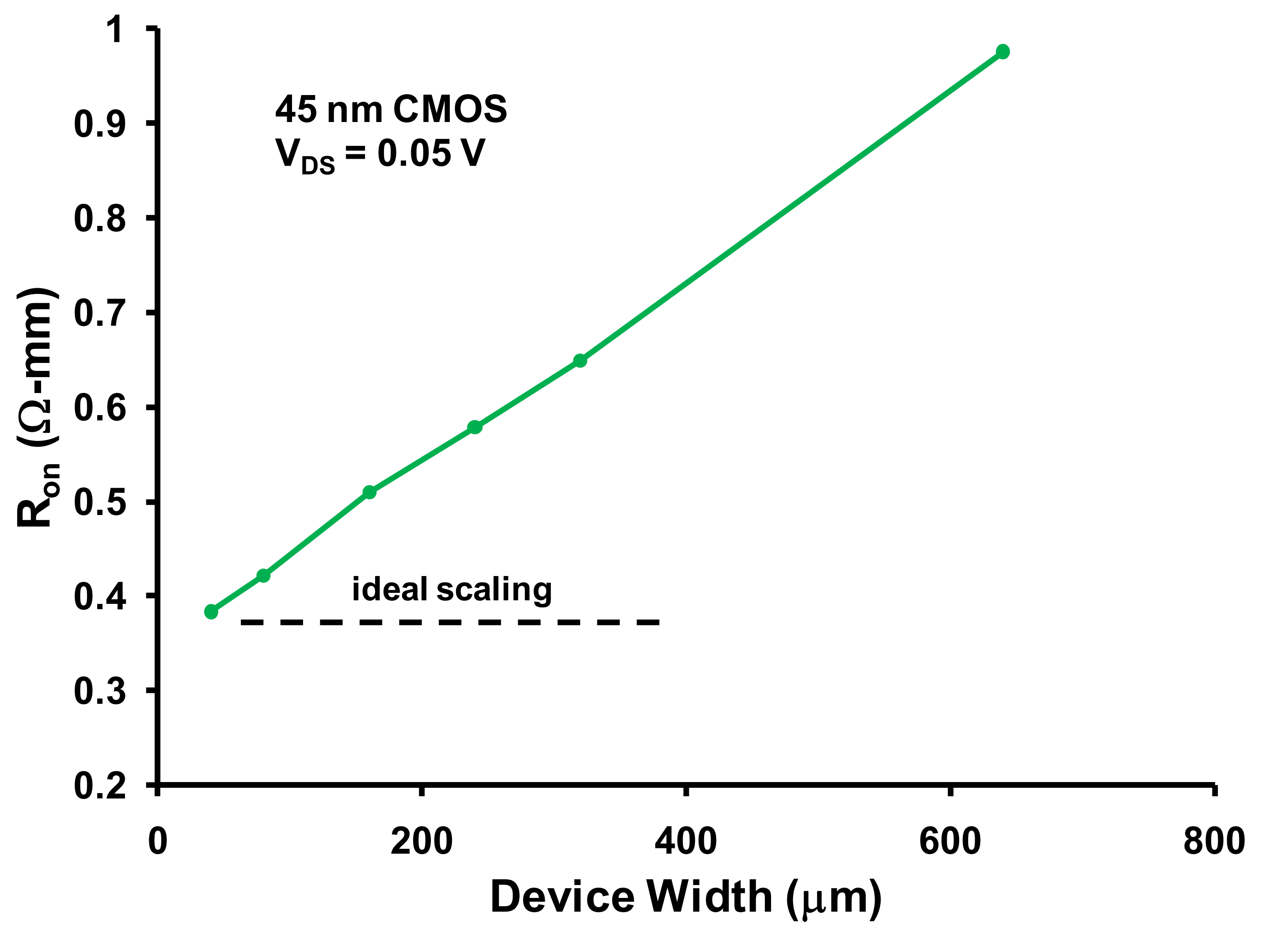
- **Technology:**
  - 45 nm Low Power CMOS Technology from IBM
  - V_{DD} = 1.1 V, Gate Length = 40 nm
  - Total Gate Width = 40 μm to 640 μm
  - W ↑ using multiple unit cells (WF = 2 μm, NF = 20)
- **Measurements:**
  - Load-pull measurements using Maury Microwave system
  - Frequency = 2 - 18 GHz
  - V_{DS} = 1.1V, V_{GS} set to ensure I_D = 200 mA/mm
  - Source and load impedances tuned for (a) max. P_{out} and (b) max. PAE

Measurement Results: P_{out} vs. W



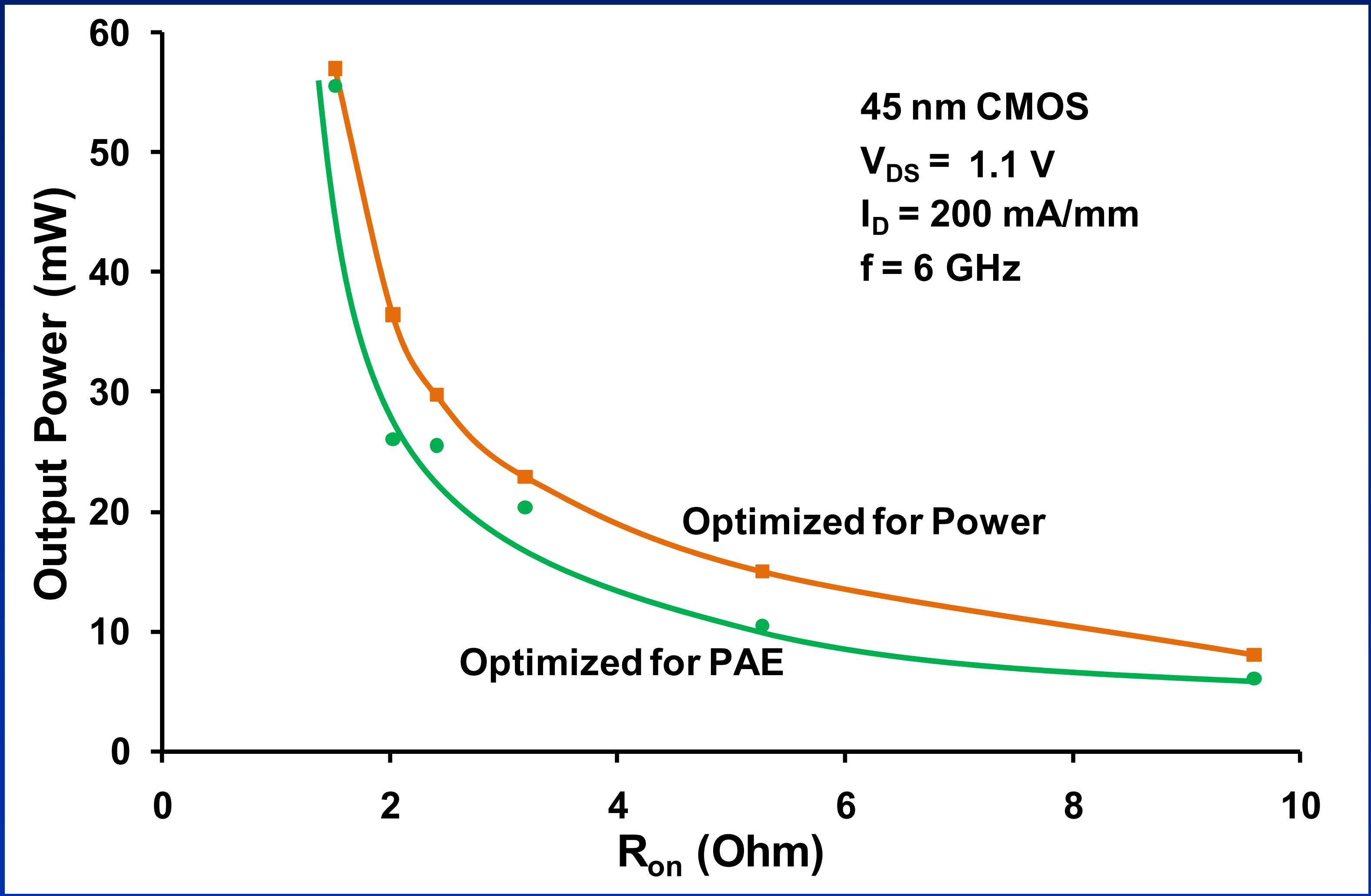
W ↑ ⇒ P_{out}/W ↓

Measurement Results: R_{on} vs. W



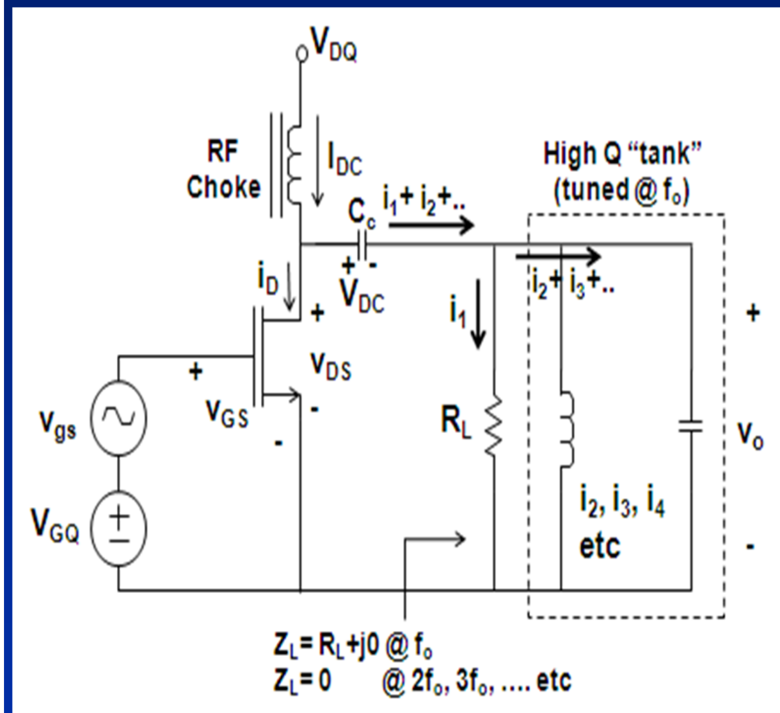
R_{on} does not scale ideally with width

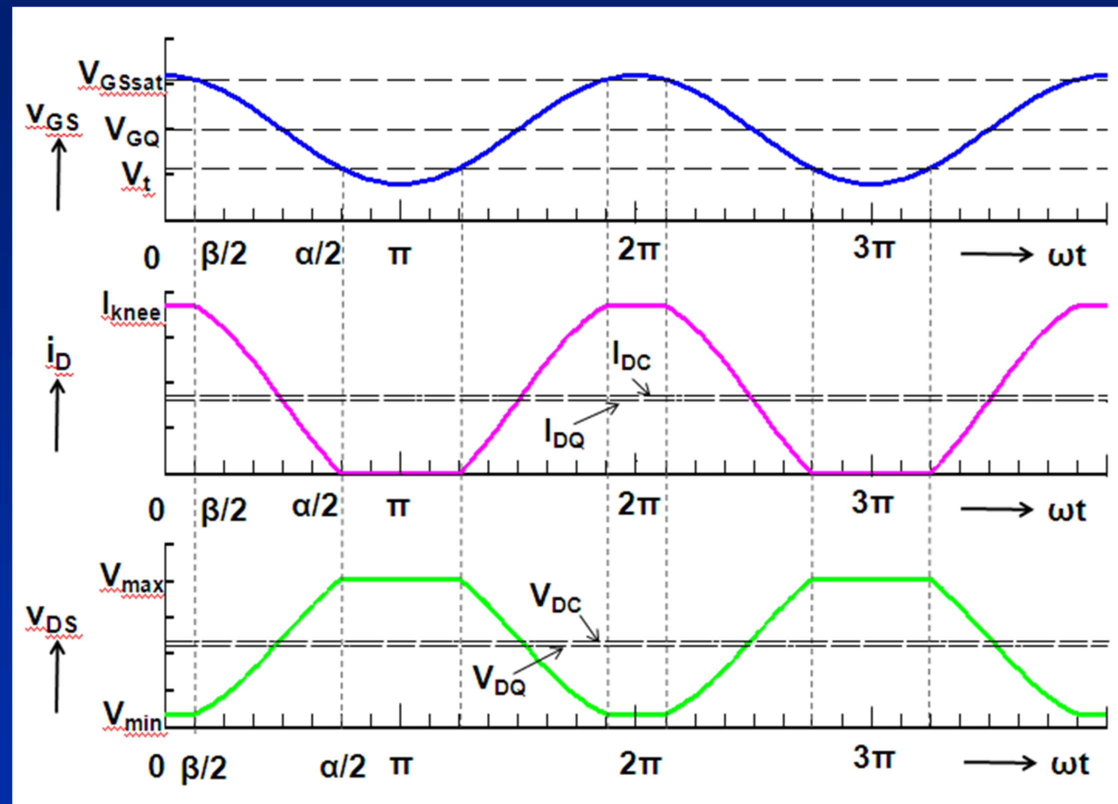
Measurement Results: P_{out} vs. R_{on}



$R_{on} \uparrow \Rightarrow P_{out} \downarrow$ $\qquad$ $P_{out} \propto 1/R_{on}$

Model Description





Assumptions: $V_{min} = I_{knee} * R_{on}$

$$V_{max} = 2*V_{DQ} - V_{min}$$

Ref: Cripps, RF power amplifiers for wireless communications, 2006

Model Equations

$$i_D(\omega t) = \begin{cases} I_{knee} & -\frac{\beta}{2} \le \omega t \le \frac{\beta}{2} \\ I_{DQ}\left(1 - \frac{\cos\omega t}{\cos\frac{\alpha}{2}}\right) & \frac{\beta}{2} \le |\omega t| \le \frac{\alpha}{2} \\ 0 & \frac{\alpha}{2} \le |\omega t| \le \pi \end{cases}$$

$$v_{DS}(\omega t) = \begin{cases} V_{min} & 0 \le |\omega t| \le \frac{\beta}{2} \\ \frac{V_{min}\cos\frac{\alpha}{2} - V_{max}\cos\frac{\beta}{2}}{\cos\frac{\alpha}{2} - \cos\frac{\beta}{2}} + \frac{(V_{max} - V_{min})\cos\omega t}{\cos\frac{\alpha}{2} - \cos\frac{\beta}{2}} & \frac{\beta}{2} \le |\omega t| \le \frac{\alpha}{2} \\ V_{max} & \frac{\alpha}{2} \le |\omega t| \le \pi \end{cases}$$

$$I_{DC} = \frac{1}{2\pi}\int_{-\pi}^{\pi} i_D(\omega t)\,d(\omega t)$$

$$I_1 = \frac{1}{\pi}\int_{-\pi}^{\pi} i_D(\omega t)\cos\omega t\,d(\omega t)$$

$$V_{DC} = \frac{1}{2\pi}\int_{-\pi}^{\pi} v_{DS}(\omega t)\,d(\omega t)$$

$$V_1 = \frac{1}{\pi}\int_{-\pi}^{\pi} v_{DS}(\omega t)\cos\omega t\,d(\omega t)$$

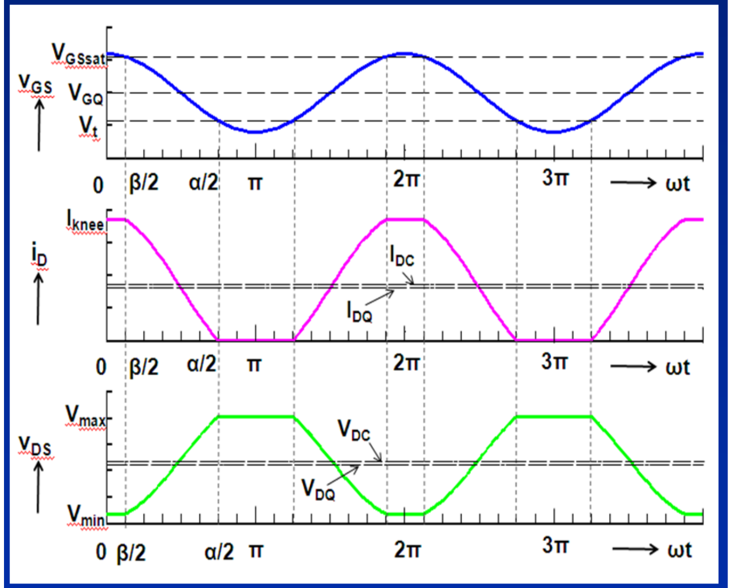
$$P_{DC} = V_{DQ} \cdot I_{DC}$$

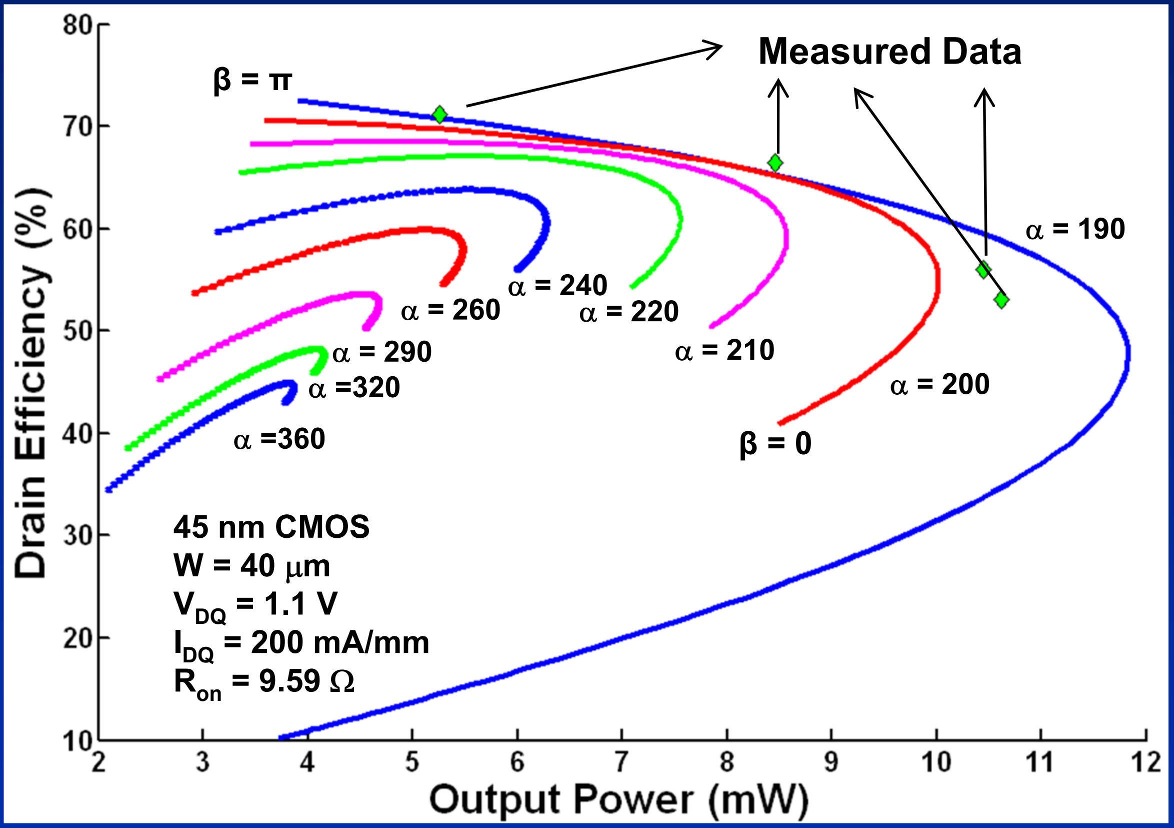
$$\eta_D\,(\%) = \frac{P_{out} * 100}{P_{DC}}$$

$$P_{out} = \frac{I_1}{\sqrt{2}} \cdot \frac{V_1}{\sqrt{2}}$$

$$R_L = \frac{V_{max} - V_{min}}{I_{knee}}$$

Modeled Power-Efficiency Locus





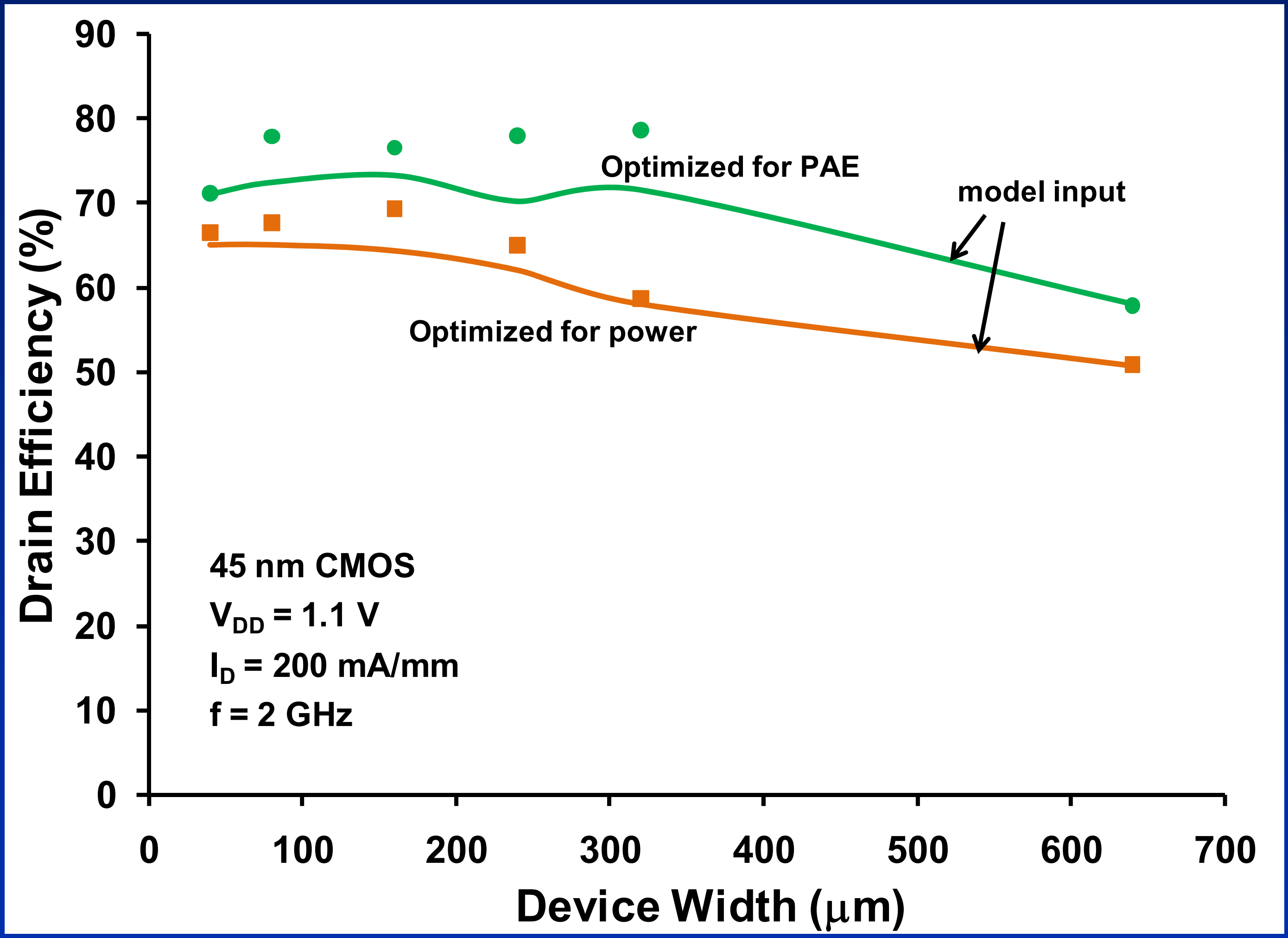
P_{out} - η_D locus can be generated for any given V_{DQ}, I_{DQ}, R_{on}

Model Usage

- **Model generates P_{out} - η_D locus at any operating point**
- **Need to choose either P_{out} or η_D to determine the other**
- **No adjustable parameters in model**

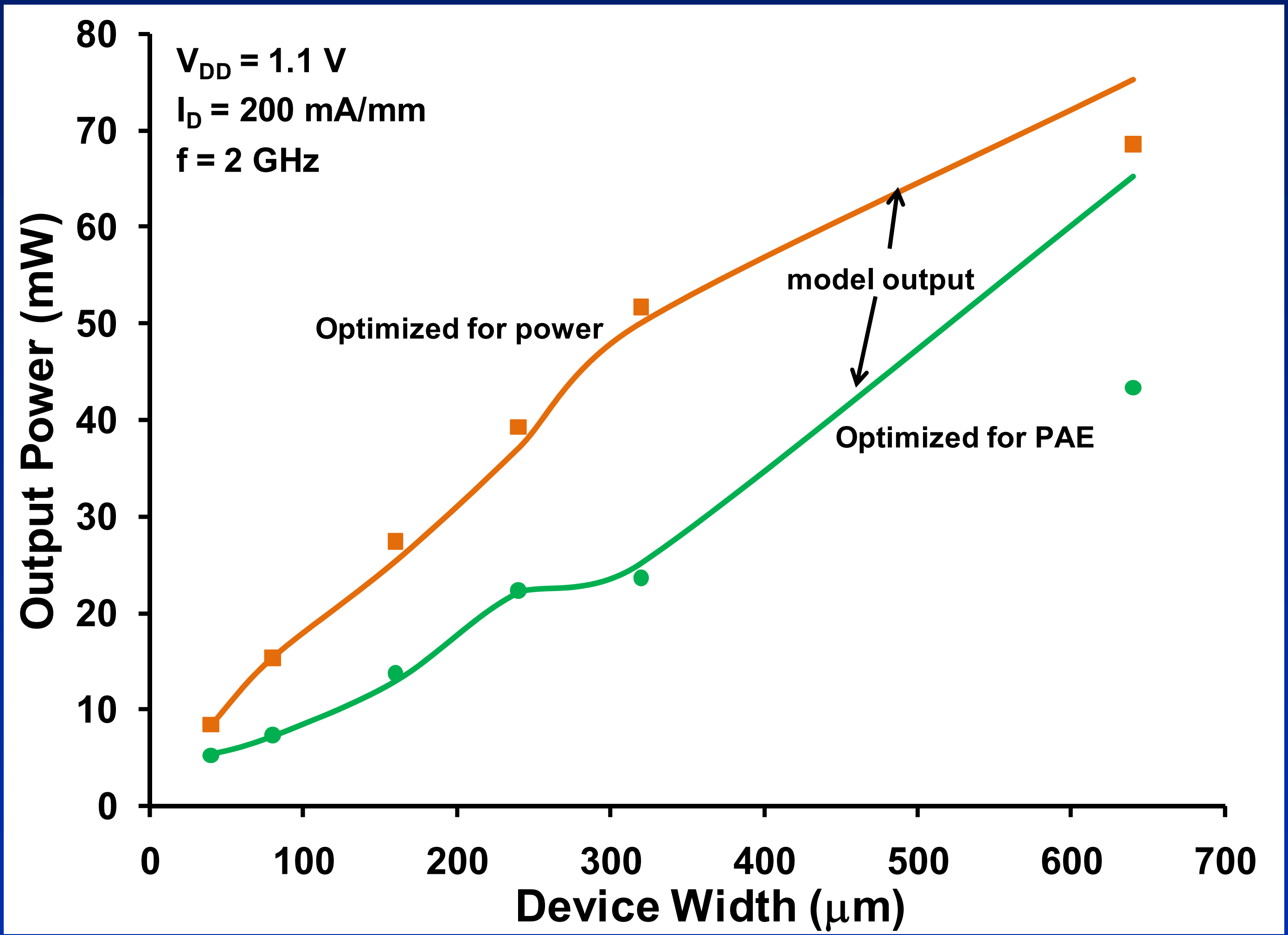
Inputs	**Intermediate**	**Outputs**
V_{DQ}	α	P_{out}
I_{DQ}	β	I_{DC}
R_{on}		R_L
η_D		

Modeled Drain Efficiency vs. W



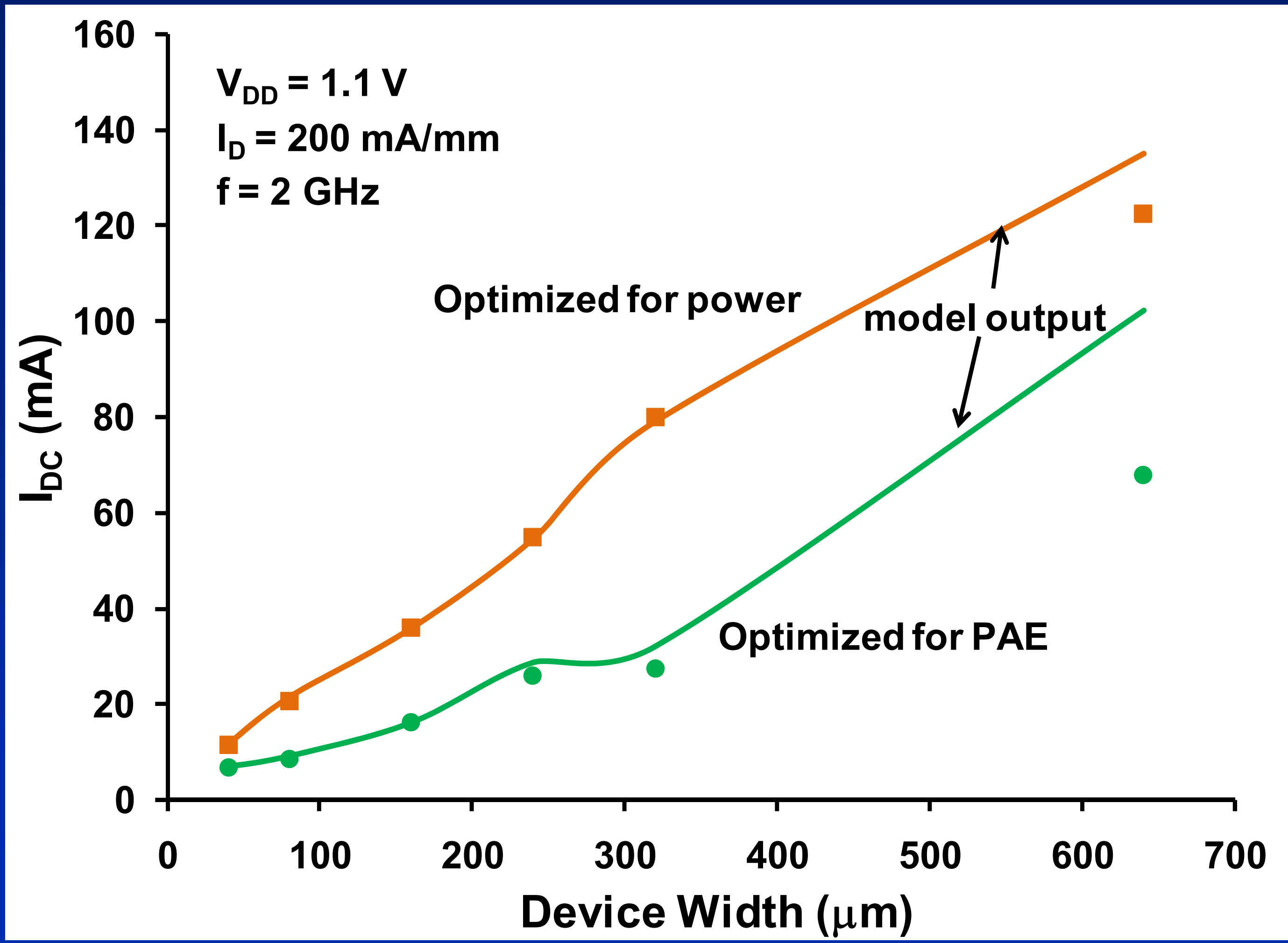
η_D for model input chosen close to measured values

Modeled P_{out} vs. W



Modeled P_{out} in line with measured data except for large W → Self heating?

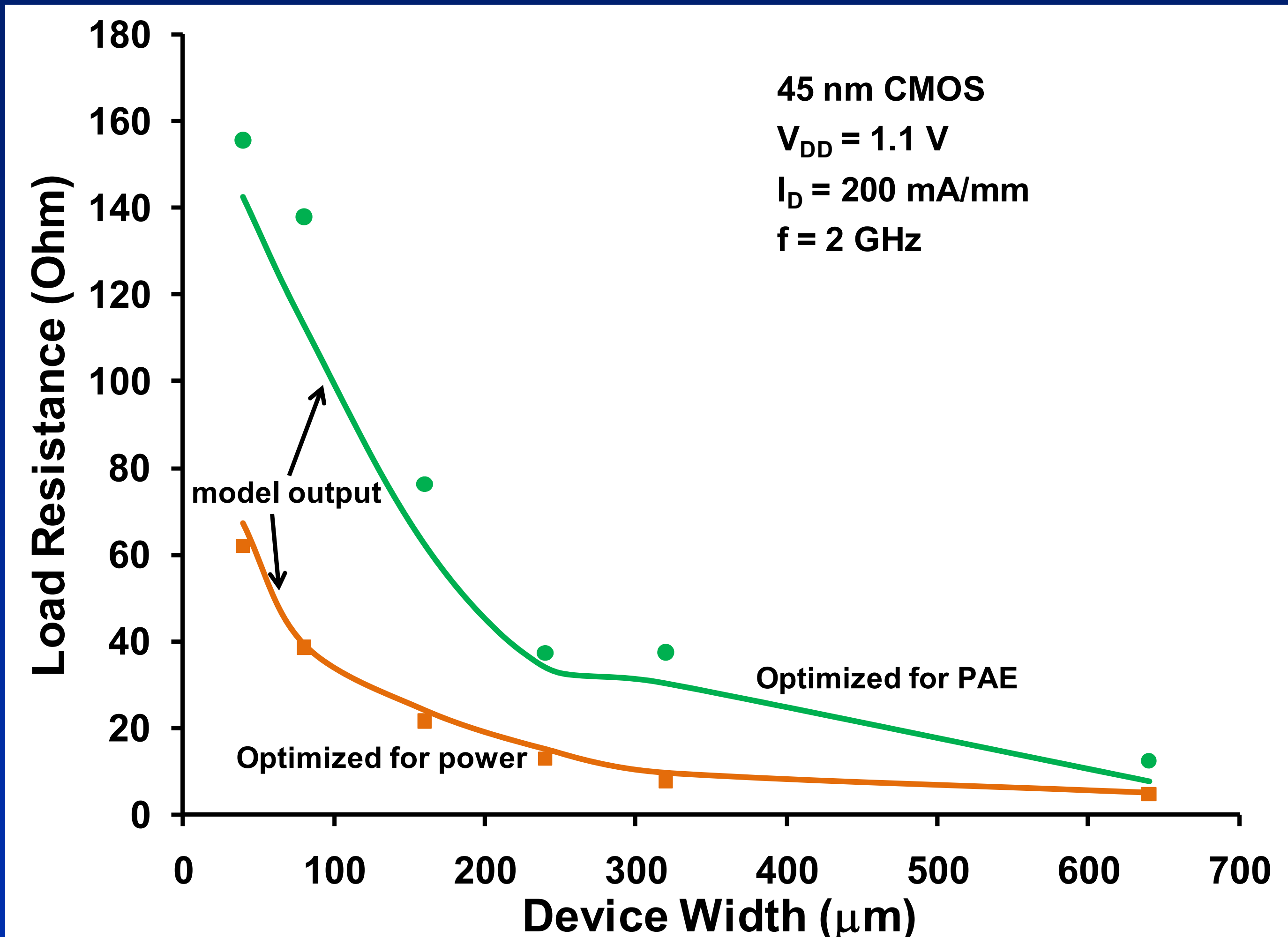
Modeled Average I_D vs. W



Good agreement between I_{DCmeas} and $I_{DCmodel}$ except for large W

Decrease in measured I_{DC} and P_{out} at large W due to self heating

Modeled R_L vs. W



Modeled R_L very close to measured values

Conclusions

- Simple analytical model allows quick calculations of maximum P_{out} and η_D for any CMOS device
  - Inputs: DC operating point and R_{on}
  - Outputs: P_{outmax} and R_L at any given η_D
- Excellent agreement with measured data (45 nm)
- R_D, R_S extracted from layout (parasitic extractions)
  - $\rightarrow$ Model can estimate P_{outmax} for any layout
- R_{on} most significant limiter to P_{out} in CMOS

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