Injection Velocity in Thin-Channel InAs HEMTs

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Abstract

We have experimentally extracted the virtual-source electron injection velocity in InAs HEMTs with a 5 nm thick channel. For long gate lengths, these devices exhibit noticeably worse injection velocity than thicker channel devices of a similar design. However, for very short gate lengths, as the devices approach the ballistic regime, the extracted injection velocity becomes rather independent of channel thickness. From these results, we can conclude that InAs-based QW-FETs with very thin channels have the potential of scaling to very short dimensions.

INTRODUCTION

As conventional Si CMOS scaling approaches the end of the roadmap, III-V based MOSFETs are seriously being considered as an alternative technology to continue Moore's law [1-2]. In the quest to map the potential of III-Vs for future CMOS applications, the High Electron Mobility Transistor (HEMT) has emerged as a valuable model system to understand relevant physics issues. Recently, the outstanding logic and high frequency characteristics of nanometer-scale InAs HEMTs have revealed the unique promise of this channel material for future quantum-well (QW) MOSFETs [3]-[5].

Scalability to 10 nm gate lengths, as needed in a future III-V CMOS technology, will require the use of an extremely thin channel, t_{ch}. As channel thickness scales down, carrier transport in the channel deteriorates, mainly as a consequence of increased carrier scattering [6]. This is a serious concern. Recently, we demonstrated InAs HEMTs with t_{ch} = 5 nm that exhibit excellent logic and high frequency performance and scalability down to 40 nm gate lengths [7]. These devices allow us to examine the impact of channel thickness scaling on the transport figure of merit that matters most for logic. This is the injection velocity at the virtual source, v_{inj} [8]. It is v_{inj} that determines the transistor drain current and its switching speed.

In this work, we have performed a rigorous extraction of the injection velocity in InAs HEMTs with a 5 nm thick channel and compared it with similar measurements on thicker channel (t_{ch} = 10 nm) devices [9]. Our results indicate that while the electron mobility degrades as the channel is thinned down, the injection velocity in very short devices is little affected. Our findings suggest that ultra-thin InAs channel QW-FETs have the potential of scaling down to very short dimensions.

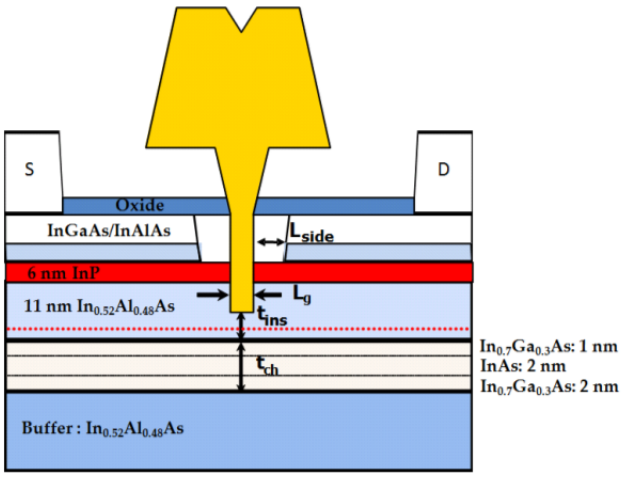

Fig. 1 Schematic diagram of thin-channel InAs HEMT [7]. The heterostructure features a 5 nm total channel thickness that includes a 2 nm InAs core channel layer.

DEVICE TECHNOLOGY

Fig. 1 shows a schematic cross sectional view of the devices studied in this work. The device heterostructure and the fabrication process were described in [7]. In essence, the channel consists of a multilayer structure with a 2 nm thick pure InAs core surrounded by a 1 nm $In_{0.7}Ga_{0.3}As$ top cladding and a 2 nm $In_{0.7}Ga_{0.3}As$ bottom cladding layer. In an

epi wafer with an identical heterostructure except for a simpler 10 nm InGaAs capping layer with $1x10^{18}$ /cm^3 Si doping, the Hall mobility and carrier density were 9,950 cm^2/V-s and 2.5 x 10^{12} /cm^3, respectively. This mobility is about 30% lower than the value obtained in a 10 nm thick channel InAs HEMT heterostructure with a 5 nm InAs core [9]. This is a manifestation of the increased carrier scattering that comes with channel thickness scaling [6]. In addition to the devices demonstrated in [7] featuring an InAlAs barrier thickness of 7 nm (measured by TEM), we have separately fabricated a new batch of devices with a thinner barrier estimated to be t_{ins} = 3 nm.

The measured transconductance (g_m) for devices with L_g = 40 nm is 1.6 S/mm for t_{ins} = 3 nm and 1.75 S/mm for t_{ins}=7 nm at V_{DS} = 0.5 V. Also, the extracted R_s for t_{ins} = 3 nm is 0.275 Ohm-mm in contrast with 0.255 Ohm-mm for t_{ins} = 7 nm.

Fig. 2 shows typical subthreshold characteristics of L_g = 40 nm HEMTs of both types. The two devices exhibit excellent behavior, but as expected, the thinner insulator device shows distinct advantages. The t_{ins} = 3 nm device is enhacement-mode with V_T = 0.11 V defined at I_D = 1 mA/mm. A subthreshold swing of 65 and DIBL of 50 mV/V have been obtained in the t_{ins} = 3 nm device. For the t_{ins} = 7 nm device, these figures are 71 mV/dec and 65 mV/V, respectively. These are excellent results at this gate length.

For the microwave characteristics, values of f_T = 465 and f_{max} = 315 GHz have been obtained for the t_{ins} = 3 nm at V_{DS}=0.5 V while values of f_T = 432 GHz and f_{max} = 337 GHz were obtained for the t_{ins} = 7 nm at V_{DS} = 0.5 V.

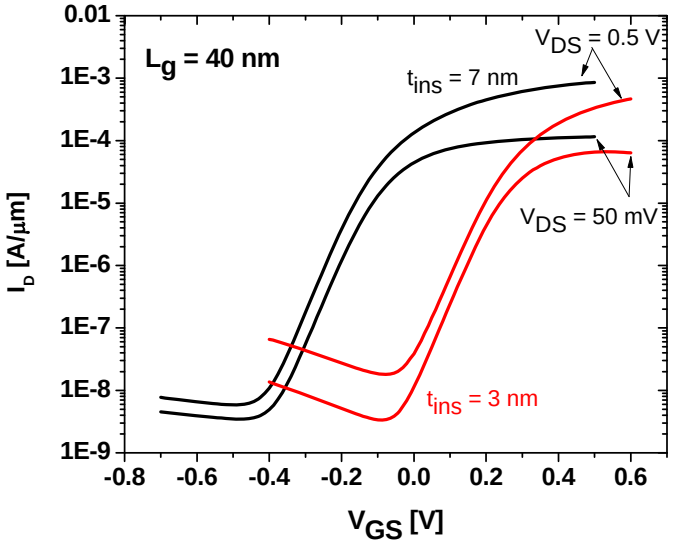

Fig. 2 Subthreshold characteristics of L_g = 40 nm InAs HEMTs with 3 nm and 7 nm insulator thickness and t_{ch} = 5 nm.

INJECTION VELOCITY

The normalized drain current (I_D) in an FET in saturation is given by the product of the areal charge density (Q_{i_xo}) and the electron velocity at the top of the energy barrier in the channel near the source [8]. This is the so called "virtual source", v_{inj}. To extract the injection velocity, we follow the methodology described in [9]. In essence, we start by estimating Q_{i_xo} and then v_{inj} is obtained from $v_{inj} = I_D/Q_{i\_xo}$.

The first step is to obtain the total gate capacitance, $C_g = C_{gs} + C_{gd}$, from high frequency S-parameter measurements at various V_{GS} values and at V_{DS} = 10 mV. Next, we remove the parasitic portion of C_g by subtracting C_g (V_{GSi} - V_T = - 0.2 V). We do this in devices with different gate lengths, as shown in **Fig. 3** for the t_{ins}=3 nm devices. From this, by plotting $C_g - C_g(V_{GSi} - V_T$ = - 0.2 V) vs L_g at a fixed gate overdrive, we extract the intrinsic capacitance per unit area, C_{gi}. The slope of the linear dependence is C_{gi}. This is shown in **Fig. 4**. By integration, we obtain Q_{i_xo}. Both are shown in **Fig. 5** for the t_{ins} = 3 nm devices. This procedure requires the measurement of R_s and R_d.

From I-V measurements, we separately extract the intrinsic transfer characteristics at V_{DS} = 0.5 V. **Fig. 6** shows I_D as a function of intrinsic gate overdrive for t_{ins} = 3 nm devices. From the ratio of current to charge and after appropriately correcting for DIBL [9], we can finally extract the injection velocity.

Fig. 7 shows the extracted v_{inj} against V_{GSi} - V_T for t_{ins} = 3 nm devices with L_g from 40 nm to 200 nm at V_{DS} = 0.5 V. We observe a general increase of v_{inj} as L_g is decreased suggesting the existence of some scattering in this gate length regime. At L_g = 40 nm, the peak injection velocity is 3.3 x 10^7 cm/s.

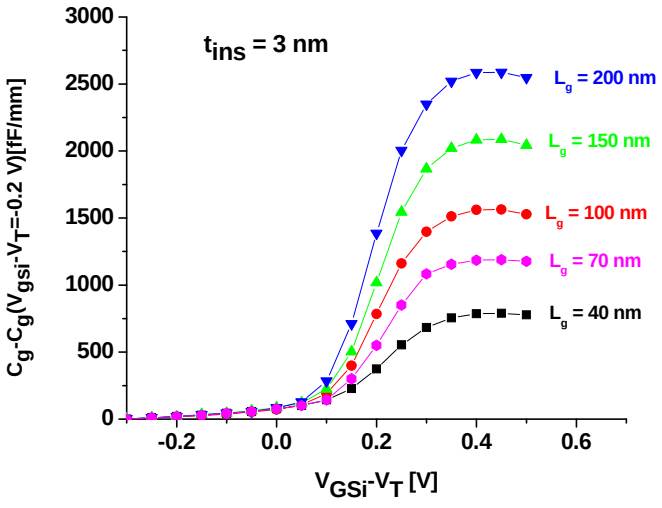

Fig. 3 Measured gate capacitance (C_g) as a function of gate overdrive ($V_{GSi} - V_T$) for t_{ins} = 3 nm InAs HEMTs at V_{DS} = 10 mV.

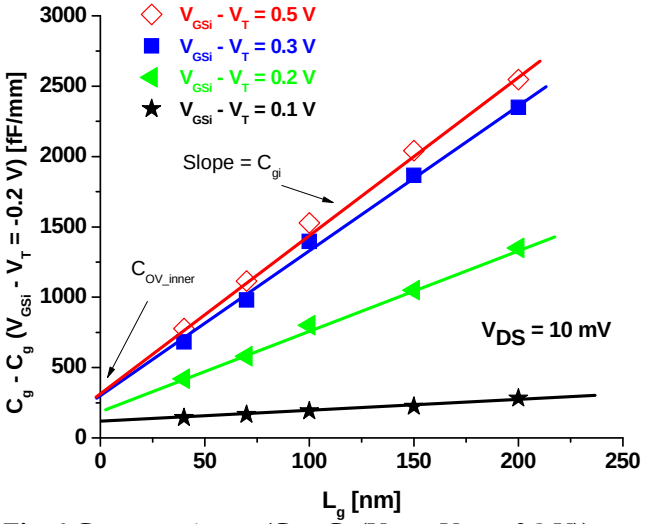

Fig. 4 Gate capacitance ($C_g - C_g$ ($V_{GSi} - V_T$ = - 0.2 V)) as a function of L_g for different values of gate overdrive at V_{DS} = 10 mV for t_{ins} = 3 nm.

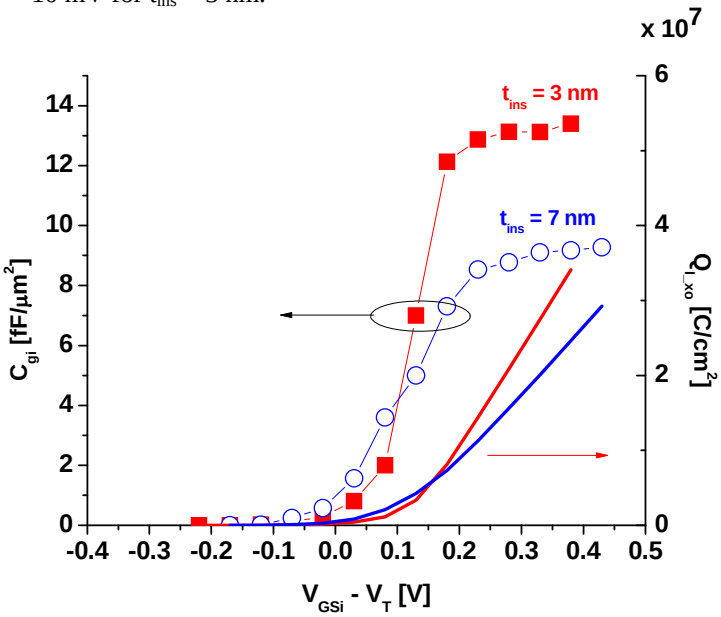

Fig. 5 Extracted intrinsic gate capacitance C_{gi} as a function of $V_{GSi} - V_T$ at V_{DS} = 10 mV for t_{ins}=3 nm and 7 nm devices. The integral of C_{gi} provides Q_{i_xo}.

Fig. 8 shows similar data for devices with t_{ins} = 7 nm. The general trends are similar with the peak v_{inj} being 2.8 x 10^7 cm/s. The decrease in injection velocity for a thicker barrier design is probably a consequence of a lower electron concentration and worse short-channel effects which are known to impact the velocity. This is also consistent with f_T measurements.

Fig. 9 shows extracted injection velocity against $V_{GSi} - V_T$ at different values of V_{DS} for a 40 nm device with t_{ins} = 7 nm. We observe a general decrease of v_{inj} as V_{DS} decreases or $V_{GSi} - V_T$ increases beyond a certain point as the device enters the linear regime.

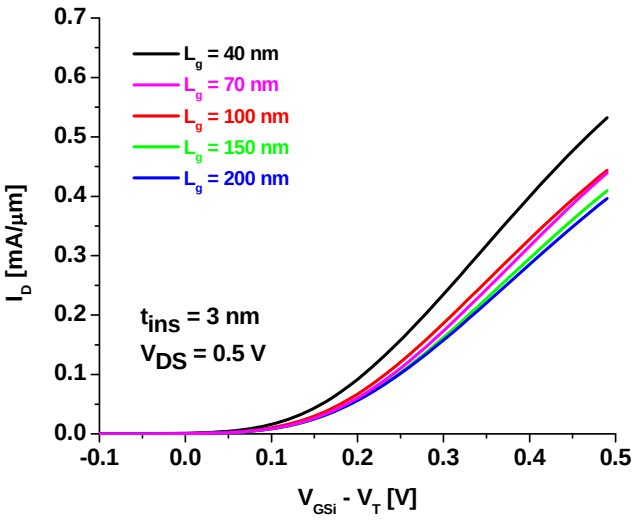

Fig. 6 Typical transfer characteristics for t_{ins} = 3 nm HEMTs of different gate lengths as a function of gate overdrive at V_{DS} = 0.5 V.

Fig. 10 summarizes the peak velocities as a function of L_g obtained at V_{DS} = 0.5 V and compares them with results obtained in [9] for thicker channel InAs HEMTs with t_{ins} = 4 nm. For long gate lengths, the InAs thin channel devices exhibit significantly worse injection velocity than the thicker channel InAs devices of about the same t_{ins} [9]. This is a consequence of the increased scattering as manifested in the reduced mobility. However, for very short gate lengths and for devices with about the same barrier thickness, as the devices become nearly fully ballistic, their injection velocities converge regardles of mobility. This is to be expected since for short enough devices, electron velocity reflects the band structure and is less affected by scattering.

This results are important because they suggest that very thin channel device designs offer the potential of scaling to very short dimensions without degradation in their transport characteristics.

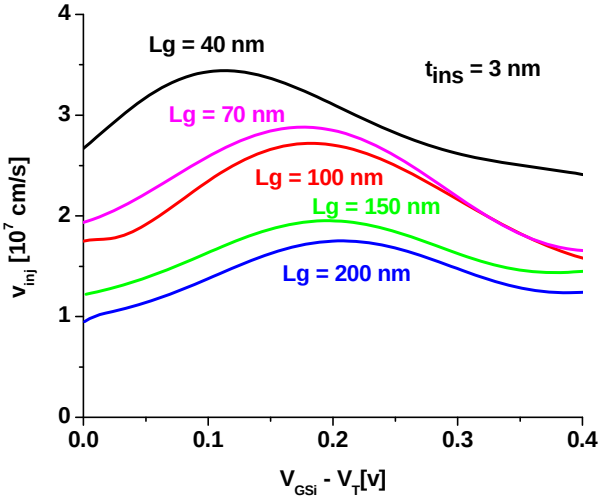

Fig. 7 Extracted v_{inj} as a function of V_{GSi}–V_T for devices with different values of L_g for t_{ins} = 3 nm at V_{DS} = 0.5 V.

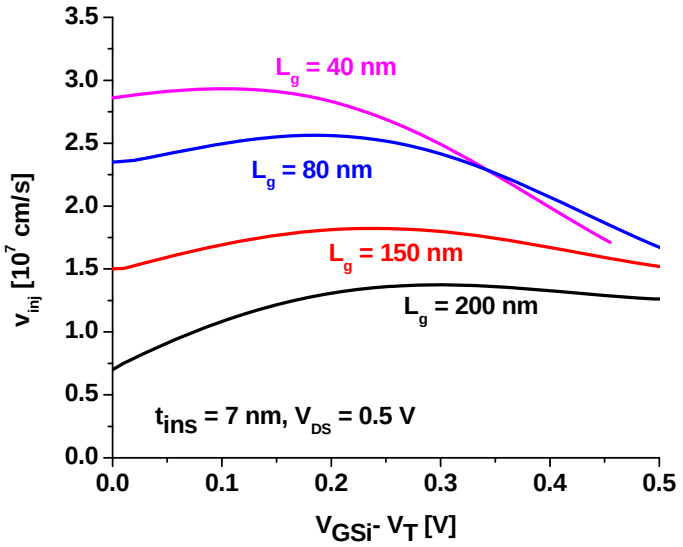

Fig. 8 Extracted v_{inj} as a function of $V_{GSi} - V_T$ for devices with different values of L_g for t_{ins} = 7 nm devices at V_{DS} = 0.5 V.

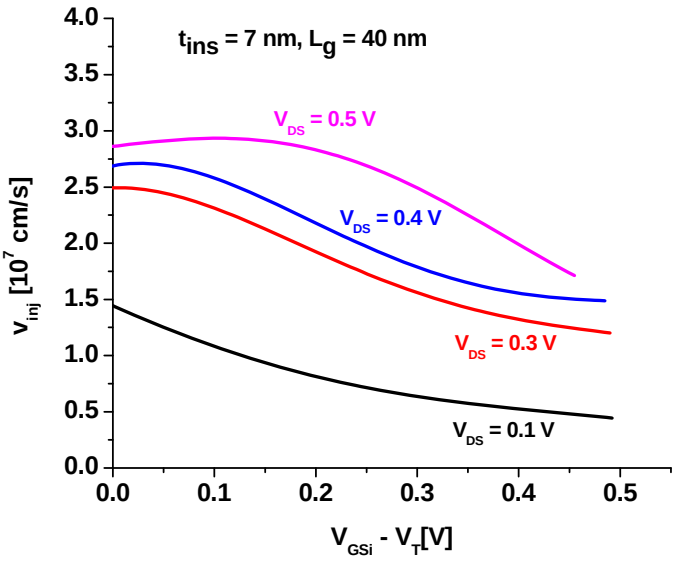

Fig. 9 Extracted v_{inj} as a function of $V_{GSi} - V_T$ for a device with L_g = 40 nm and t_{ins} = 7 nm, at different values of V_{DS}.

CONCLUSION

We have performed a rigorous extraction of the injection velocity in thin-channel InAs HEMTs. Although the electron mobility degrades in thin channels, the injection velocity does so much less. In a L_g = 40 nm gate HEMT with a 5 nm thin InAs channel, we have measured an injection velocity of 3.3 x 10^7 cm/s. This works suggest that InAs-based thin channel QW-FETs have the potential of scaling to very short dimensions.

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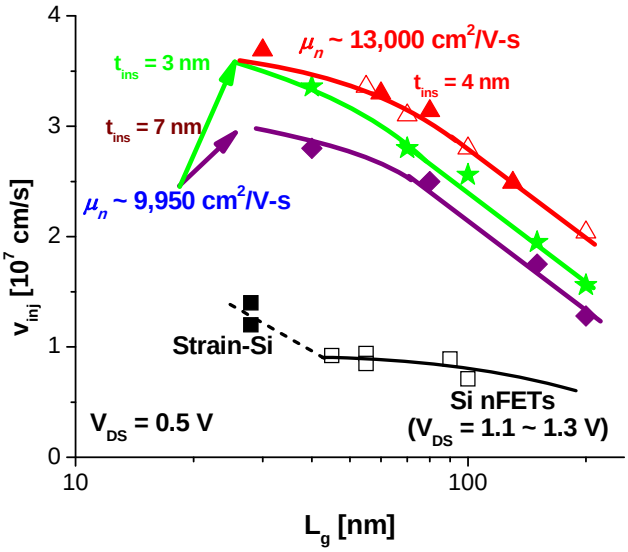

Fig. 10 Extracted v_{inj} vs. L_g for various InAs HEMTs with different channel and barrier thickness at V_{DS} = 0.5 V, together with those of advanced Si nFETs at V_{DS} = 1.1 ~1.3 V.