Impact of Gate Placement on RF Degradation in GaN High Electron Mobility Transistors

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Abstract

We have investigated RF degradation in GaN high electron mobility transistors (HEMTs) with different gate placement in the source-drain gap. We found that devices with a centered gate show different degradation behavior from those with the gate placed closer to the source. In particular, centered gate devices degraded through a mechanism that has a similar signature as that responsible for high-voltage DC degradation in the OFF state and is likely driven by voltage. In contrast, offset gate devices showed a large R_S increase due to the combination of high voltage and high current stress condition.

I. Introduction

GaN high electron mobility transistors (HEMTs) have demonstrated outstanding RF power performance. However, the reliability of these devices is still a bottleneck preventing wide adoption of this technology. While DC reliability has been studied extensively [1-2], much less attention has been given to the RF reliability of this technology [3-6]. In order to improve RF reliability of GaN HEMTs, detailed understanding of the mechanisms behind RF degradation is essential.

Towards this goal, we have developed a methodology to systematically investigate RF reliability and to compare it with DC reliability [6]. In a previous study, we found that RF stress introduces much more severe degradation than DC stress at a given bias point and that the degradation increases as the input power level increases. Unlike DC stress, RF stress was found to result in a prominent increase in source resistance. The pattern of degradation was very different from that induced by high-voltage OFF state stress in similar devices [2]. In fact, the degradation was traced to the simultaneous application of high voltage and high current stress during the RF swing [6].

In this work, we investigate how the placement of the gate in the source-gate gap impacts RF degradation. We find a markedly different pattern of degradation that resembles that of high-voltage DC stress in this technology.

II. Experimental

This research is carried out on a four-channel Accel-RF life-test system AARTS RF10000-4/S. The built-in switching matrix in the Accel-RF system allows us to temporarily stop RF stressing and characterize the device under test through an external semiconductor parameter analyzer [6].

During a typical experiment, we monitored several DC and RF figures of merit, including I_{Dmax} (defined at V_{DS}=5 V and V_{GS}=2 V), I_{Goff} (defined at V_{DS}=0.1 and V_{GS}=-5 V), R_S, R_D, and saturated P_{out} (measured at V_{DS}=28 V and I_{DQ}=250 mA/mm with P_{in}=23 dBm). These were measured every 5 minutes at T_{base}=50 °C. At selected times during the experiment, we also carried out a more comprehensive RF characterization and measured current collapse (defined as the relative change in I_{Dmax} after applying 1 s V_{DS}=0 and V_{GS}=-10 V pulse) and permanent degradation in I_{Dmax}. These figures of merit were measured at room temperature after a detrapping step. The detailed setup and experimental procedure are described in [6].

We have performed DC and RF step-P_{in} experiments on 4x100 μm GaN MMICs with gates centered in the source-drain gap. The main purpose of this experiment was to compare with our previous results in [6] that were obtained on similar offset-gate devices where the gate was shifted towards the source by 1 μm. We first stressed the device under DC condition with V_{DS}=40 V and I_{DQ}=250 mA/mm for 5 hours. Then, in order to understand the impact of small-signal RF input, we applied RF signal with P_{in}=1 dBm on top of this DC bias for an additional 5 hours. This was followed by large-signal RF step-stress stress with increasing P_{in} from 20 to 27 dBm (Figure 1). The MMIC device was stressed for 5 hours at each step, and the step size was 1 dBm. T_{base} for stress was constant at 50 °C throughout the experiment.

III. Result and Discussion

As shown in Figure 1, we observe a typical critical behavior with device degradation characterized by a relatively sharp onset [7]. During DC and RF stress with small P_{in}=1 dBm, there is relatively little degradation for all figures of merit except for some soft degradation. As we increase the input power to 20 dBm, there is a sudden rise in I_{Goff}. At the same time, I_{Dmax} and R_D start to degrade visibly, and the degradation accelerates as P_{in} is increased. However, the source resistance did not change throughout the experiment (Figure 1).

In Figure 1, spikes in I_{Dmax} and R_D can be seen between P_{in} steps. These spikes are due to a short detrapping period that

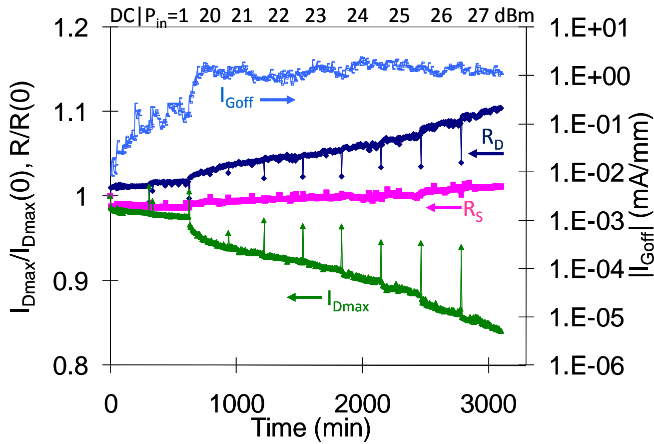

Figure 1. Change in I_{Dmax}, R_S, R_D, and I_{Goff} in DC and RF step-P_{in} stress tests. A DC stress at V_{DS}=40 V and I_{DQ}=100 mA/mm was followed by RF stress steps around that bias point with varying P_{in}=1 to 27 dBm. These measurements were done at T_{base}=50 °C.

we introduce when transitioning to a new stress condition. This short detrapping phase produces a partial recovery in R_D and I_{Dmax}. This suggests that stress introduces significant trapping. The fact that the original values of R_D and I_{Dmax} are not reached after electron detrapping indicates that there is additional permanent degradation that is introduced as a result of stress. In Figure 1, the envelopes of the spikes in I_{Dmax} and R_D represent the permanent degradation.

This interpretation is confirmed in Figure 2 where we show current collapse, permanent I_{Dmax} degradation (in a fully detrapped condition), and output power degradation measured at the transition point between P_{in} values after a detrapping step. As it can be seen, all of these device parameters start to sharply degrade beyond P_{in}=20 dBm. The increase in current collapse shows that traps are being created as a result of stress. As in our previous results [4, 6], we observe good correlation between P_{out} and I_{Dmax} degradation (Figure 3). A 1dB degradation in P_{out} corresponds to a 9% degradation in I_{Dmax}.

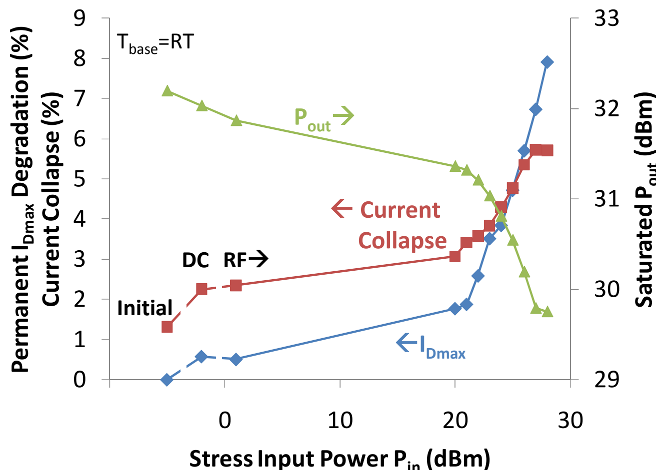

Figure 2. Change in current collapse, permanent I_{Dmax} degradation, and output power in the experiment of Figure 1. These measurements were taken with T_{base}=RT.

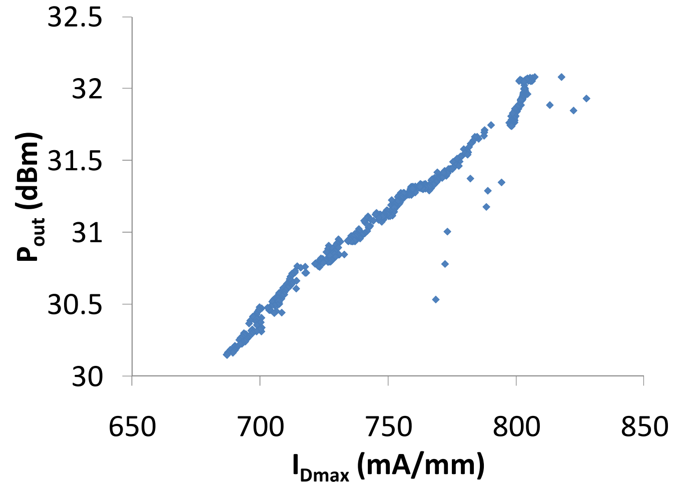

Figure 3. Correlation between P_{out} and I_{Dmax} degradation. 1dB degradation in P_{out} corresponds to 9% degradation in I_{Dmax}.

Figure 4 shows the output power characteristics before and after the stress experiment. Although the small-signal gain (at P_{in}=10 dBm) was slightly decreased, the saturated output power (at P_{in}=23 dBm) shows much larger degradation. This is because at larger P_{in}, due to the wider expansion of the RF loadline towards the high V_{DS} OFF-state, a larger electric field induces more current collapse, which in turn decreases I_{Dmax} beyond the permanent degradation, and thus the current swing and P_{out} decrease. This is consistent with the correlation between P_{out} and I_{Dmax} degradation in Figure 3. The degradation in I_{Dmax} in Figure 3 includes both current collapse and permanent components as it was measured without a detrapping phase.

A significant difference between this work and that of [6] is that the source resistance R_S does not increase even after degradation at the highest P_{in} level. Consistent observations

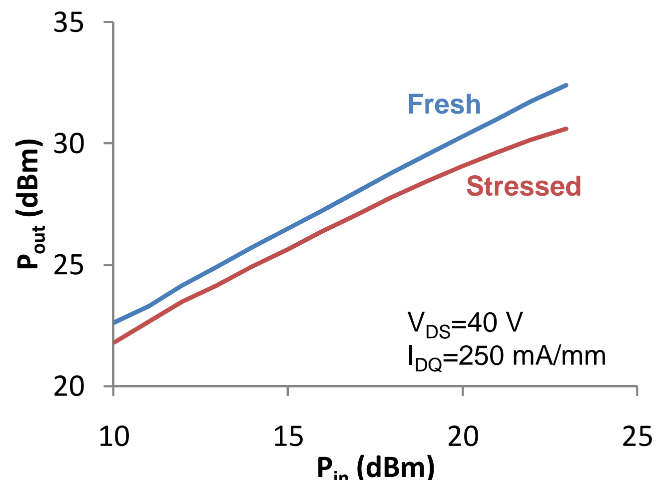

Figure 4. Change in output power characteristics before and after the stress test in Figure 1. The bias condition is VDS=40 V and IDQ=250 mA/mm.

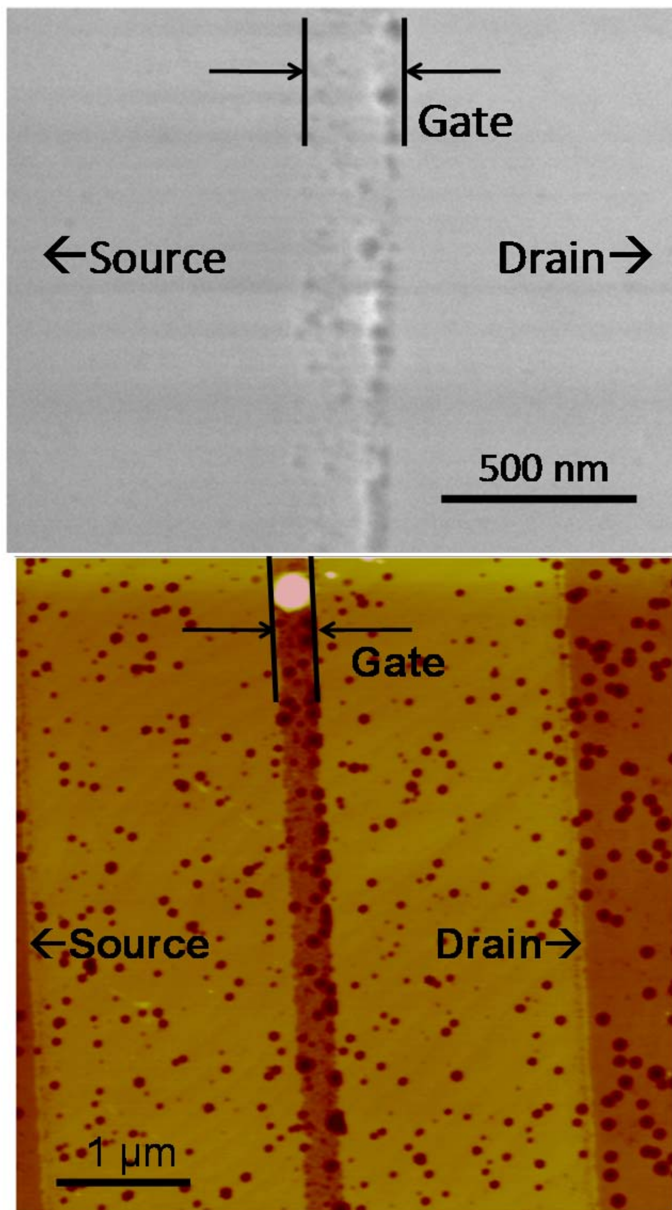

Figure 5. Plan-view SEM (top) and AFM (bottom) images of a degraded device with centered gate stressed under RF. SiN passivation and gate metal were removed to expose the semiconductor surface area. The stress condition was similar to the experiment in Figure 1.

were made in two other devices with centered-gate. This indicates that in the present work, we are in front of a different degradation pattern that suggests that the dominant degradation mechanism under RF stress is strongly influenced by the gate placement.

In order to understand the degradation mechanisms in more detail, we have investigated the structural degradation through a recently developed plan-view technique [8-9]. Figure 5 shows plan-view SEM and AFM images of a centered-gate device that was stressed under similar conditions as in Figure 1 and degraded following a similar pattern. It can be seen that

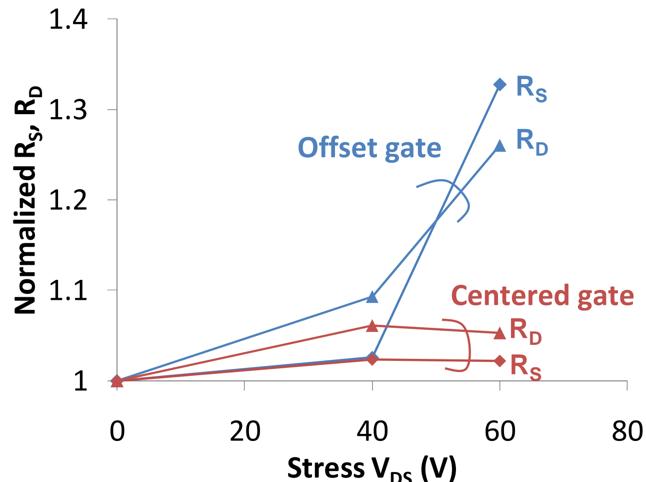

Figure 6. Change in R_S under pulsed stress tests at room temperature. The pulse width is 500 us and the duty cycle is 0.05%. 100 pulses were applied. The current level at the pulse was 950 mA/mm. Pulse stress under these conditions mimics well the RF degradation of the offset-gate devices but does not do the same for the centered-gate transistors.

pits are formed along the drain side of the gate edge just as observed in devices stressed at high voltage in DC in the OFF-state [8-9]. This is consistent with the critical behavior seen in I_{Goff} and other figures of merit in the RF stress test and thus suggests that these devices are likely to degrade due to the same mechanism observed in typical high-voltage OFF-state DC stress. In contrast, an offset-gate device stressed and analyzed under similar conditions did not show any visibly structural degradation. This indicates that offset-gate devices in our previous RF reliability study [6] suffer from a different degradation mechanism that is not present in the centered devices that we tested in this work.

In our earlier RF stress study in offset-gate devices, we were able to replicate the observed RF device degradation by applying high power pulses [6]. We have performed similar pulsed stress experiments with high V_{DS} and I_D on the present devices. As shown in Figure 6, we found that the device with centered-gate does not exhibit any increase in R_S under high power pulse stress though it exhibits some level of R_D increase.

Our results indicate that devices with different gate placement in the source-drain gap are affected by different degradation mechanisms under RF stress. In the present devices, it is the high voltage that seems to be the dominant degrading factor. In the offset-gate devices, it is the simultaneous occurrence of high current and high voltage that degrades the device [6]. The physical origin of the peculiar degradation of the offset devices in [6] still remains to be understood.

IV. Conclusion

In conclusion, we have investigated RF degradation of GaN HEMTs with different gate placement in the source-drain

gap. We found that devices with centered-gate show a similar degradation mode as under high-voltage DC stress. These devices were not affected by high power pulsed stress. The pattern of degradation is very different from similar devices with the gate offset towards the source that were studied earlier.

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