Impact of Gate Placement on RF Degradation in GaN HEMTs

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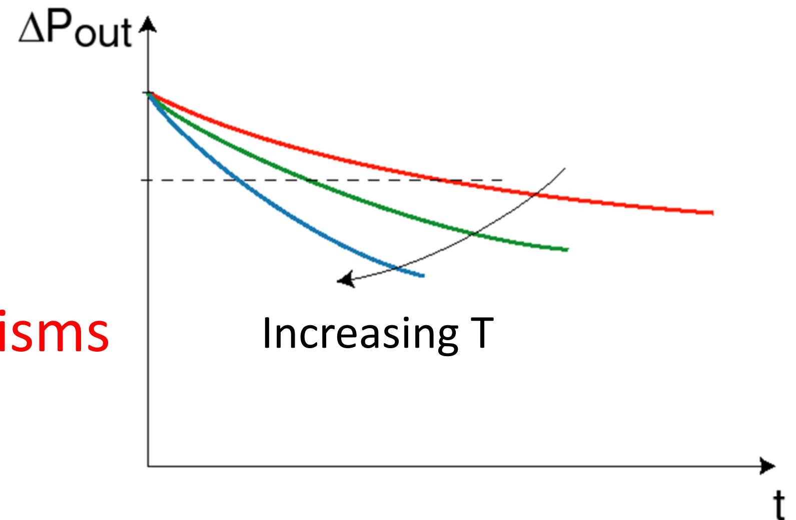
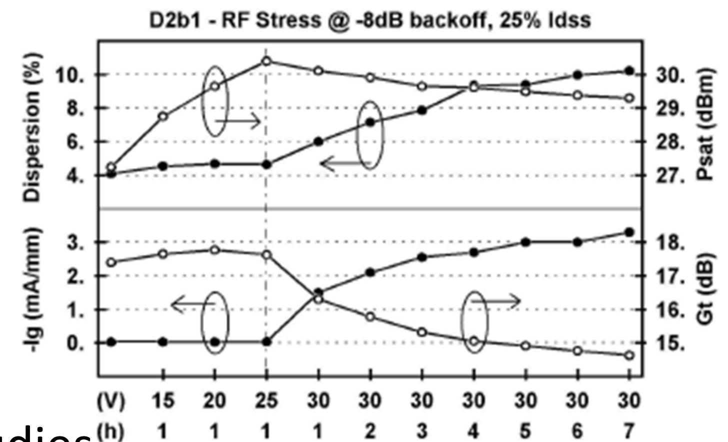
Motivation

- RF reliability – main concern in GaN HEMT RF power amplifier
- Compared to DC stress, little known about degradation mechanisms under RF stress
  - P_{out}↓, Gain↓
  - I_D↓, dispersion↑, g_m↓, $|I_G|$↑
  - RF introduces more degradation than DC [Conway, IRPS 2007; Joh, ROCS 2008; Chini, IEDM 2009; Joh, IEDM 2010]
- Goal:
  - Develop methodology for RF reliability studies
  - Identify dominant RF degradation mechanisms
  - Correlate RF and DC reliability



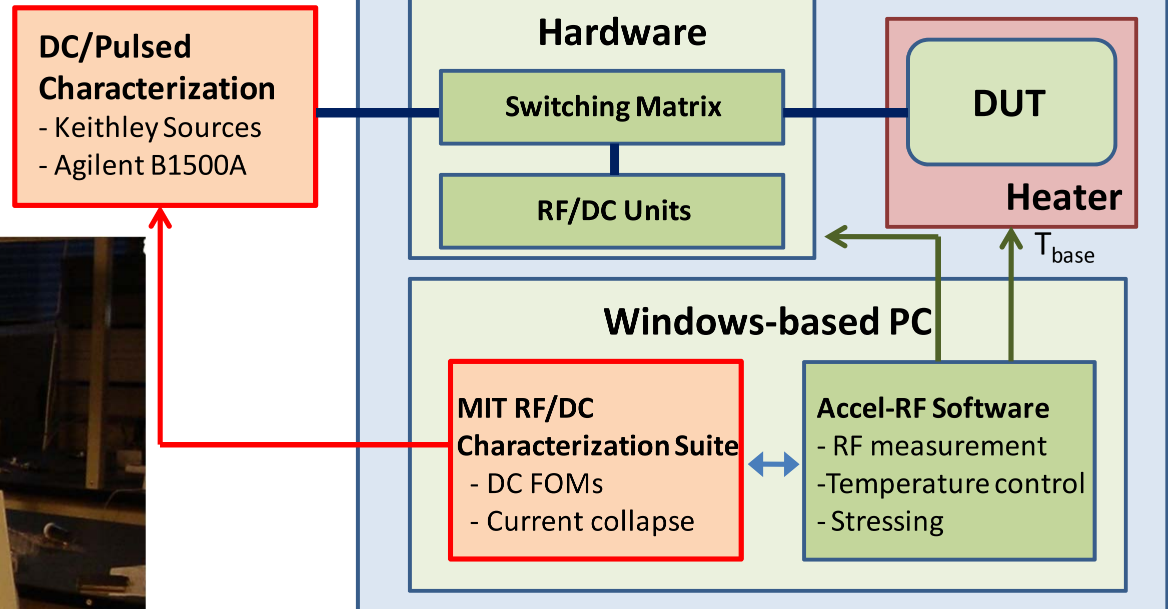


Chini, IEDM 2009

Experimental Setup

Accel-RF AARTS RF10000-4/S system:

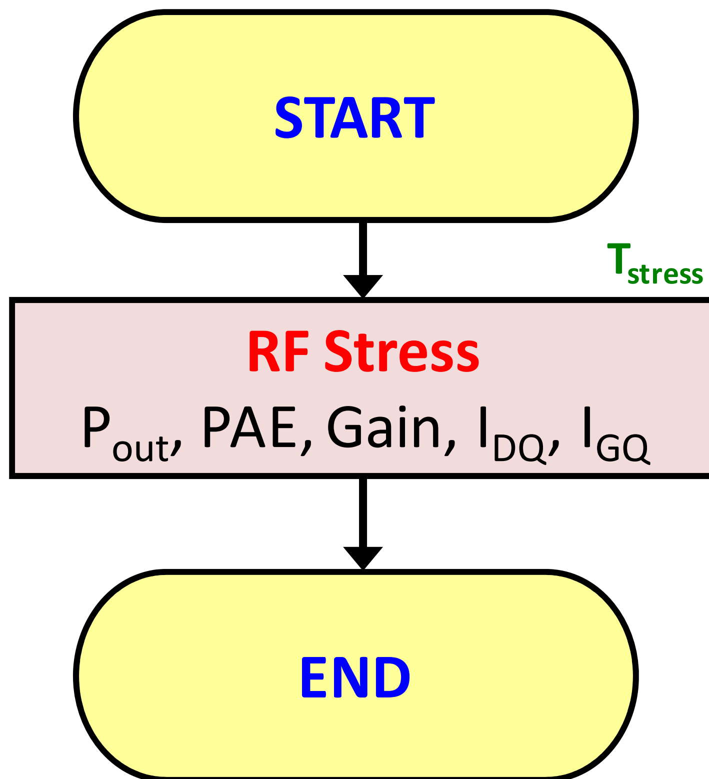
- two 2-4 GHz channels
- two 7-12 GHz channels
- Max P_{in}=30 dBm
- T_{base}=50-200 °C



Accel-RF system augmented with:

- external instrumentation for DC/pulsed characterization
- software to control external instrumentation and extract DC and RF FOMs

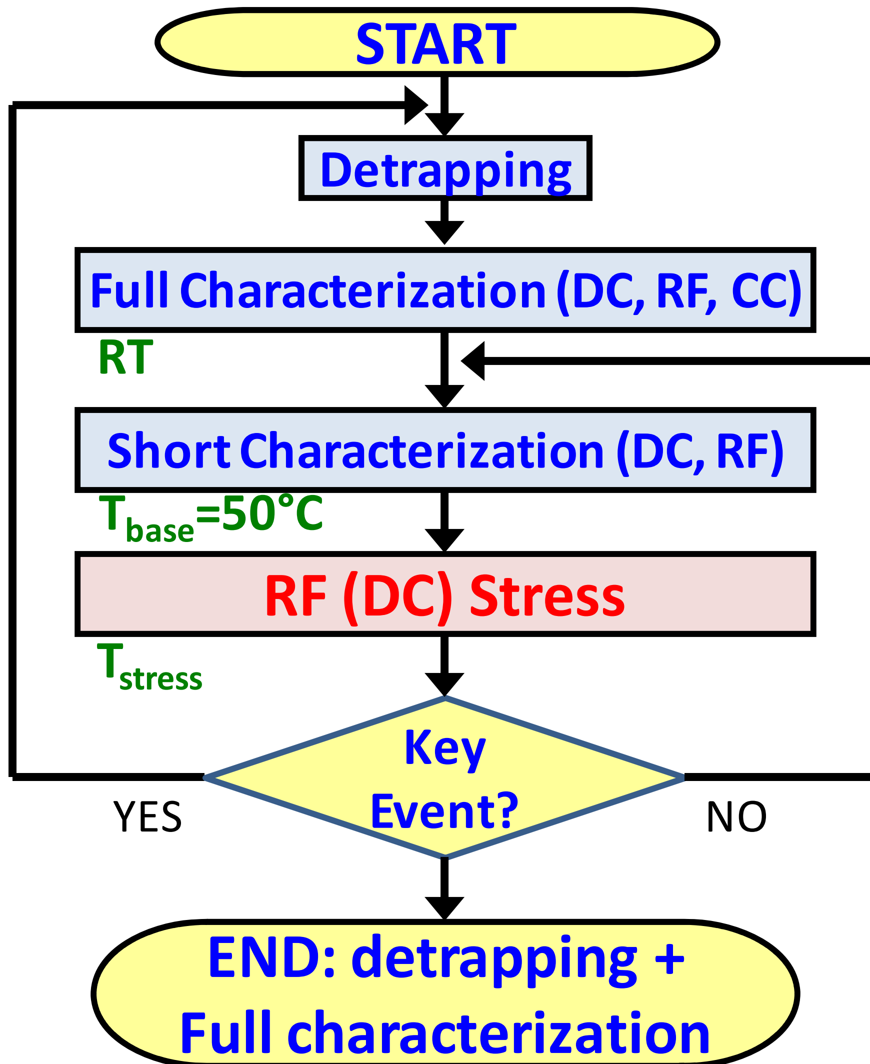
RF Experiment Flowchart: Conventional Approach



Limitations:

- Bias point shifts during stress
- Limited RF characterization
- No DC characterization
- No trap characterization
- If examining different RF conditions, RF characterization confusing

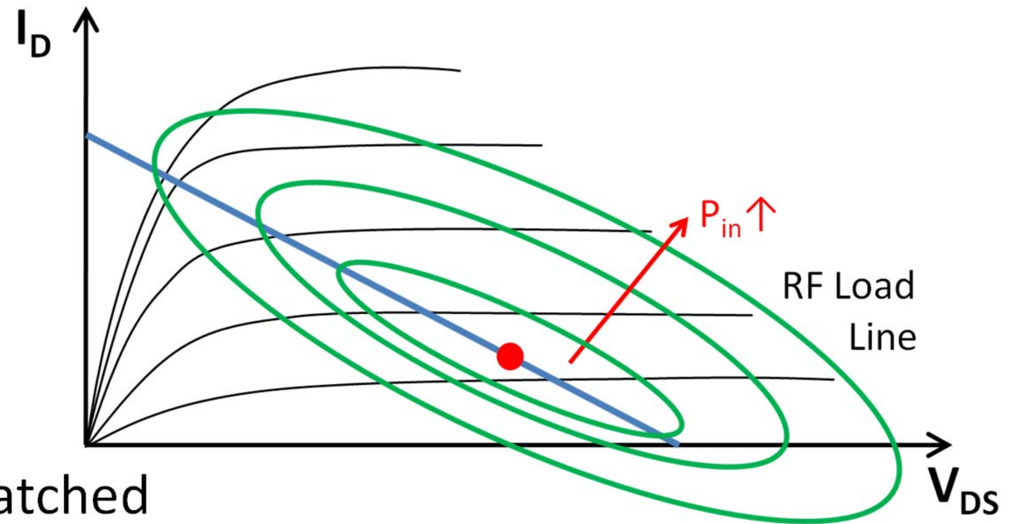
RF Experiment Flowchart: Improved Approach



- Short characterization:
  - Every few minutes at T_{base}=50 °C
  - DC FOMs: I_{Dmax}, R_S, R_D, V_T, I_{Goff}, …
  - RF FOMs @ V_{DS}=28 V & I_{DQ}=100 mA/mm
    - Saturated conditions (P_{in}=23 dBm): $P_{out,sat}$, G_{sat}, PAE
    - Linear conditions (P_{in}=10 dBm): G_{lin}
- Full Characterization:
  - After key events at room temperature
  - Full DC I-V sweep
  - Current collapse (after 1” V_{DS}=0, V_{GS}=-10 V pulse)
  - Full RF power sweep @ V_{DS}=28 V, I_{DQ}=100 mA/mm
- Detrapping: T_{base}=100°C for 30 mins

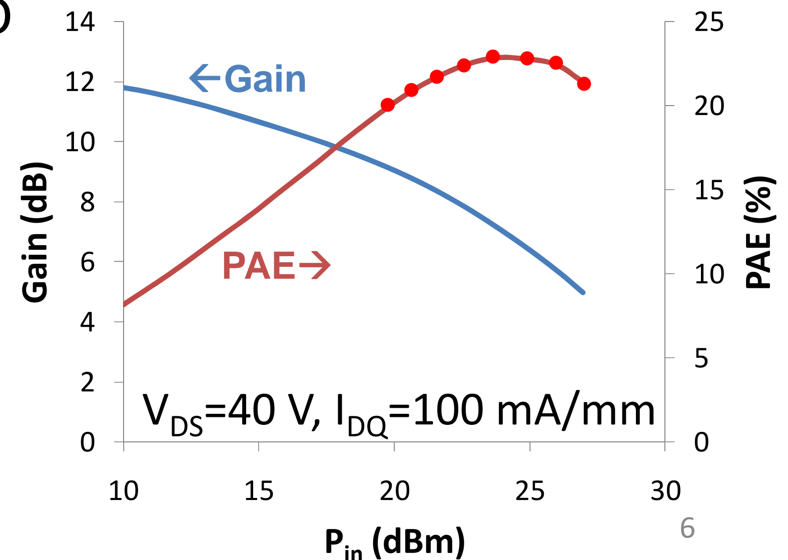
P_{in} Step-Stress: Centered Gate

- Motivation:
  - higher P_{in} → larger V waveform at output



- MMIC:
  - single-stage internally-matched
  - 4x100 μm GaN HEMT
  - Gate placed at the center btw S & D

- Step P_{in} stress:
  - V_{DS} = 40 V, I_{DQ} = 100 mA/mm
  - P_{in} = 0 (DC), 1, 20-27 dBm
  - 300 min stress at each step
  - T_{stress}=50 °C



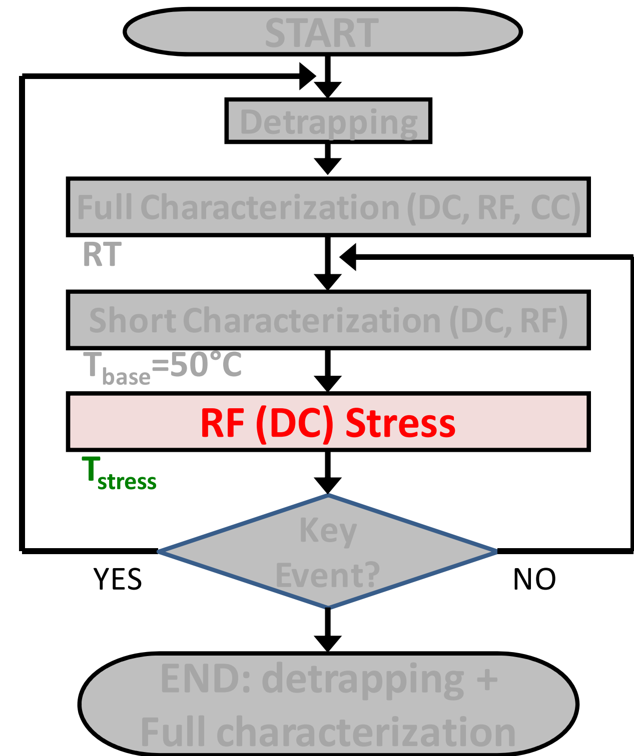
Characterization during RF Stress

P_{in}

P_{out}

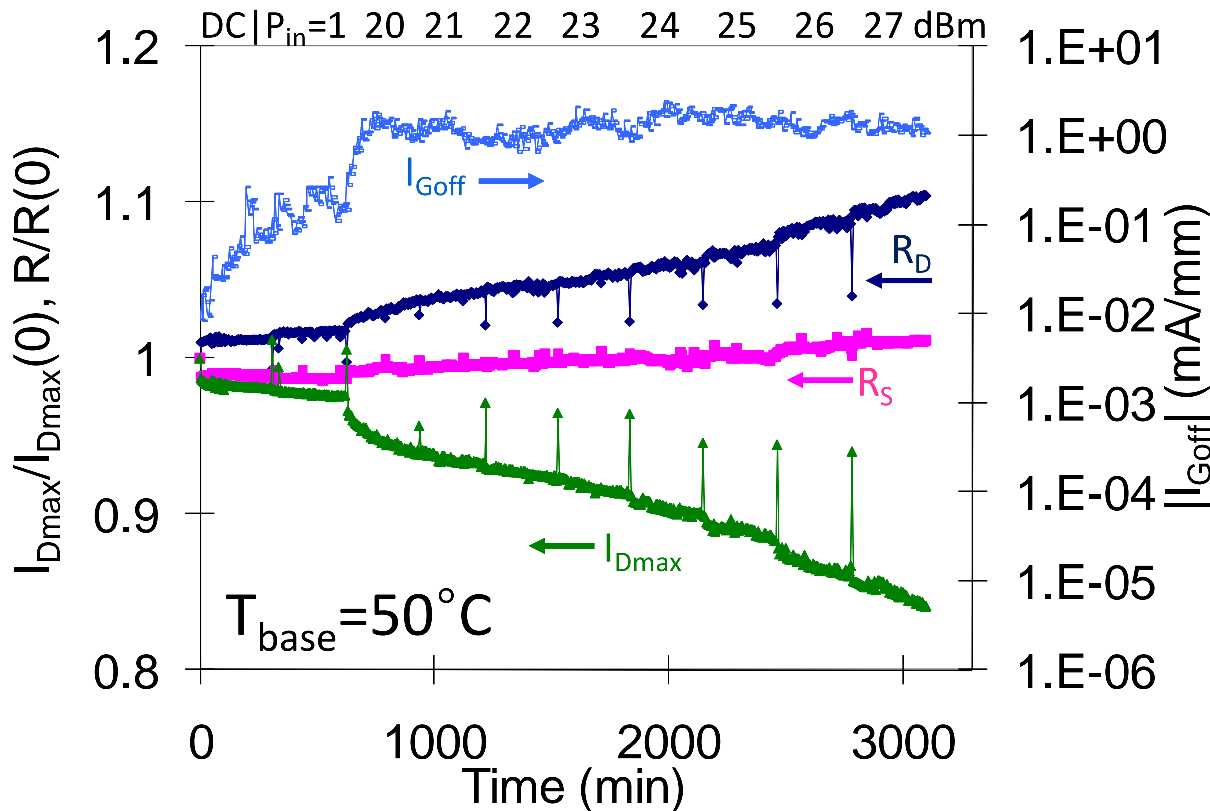
I_{DQ}

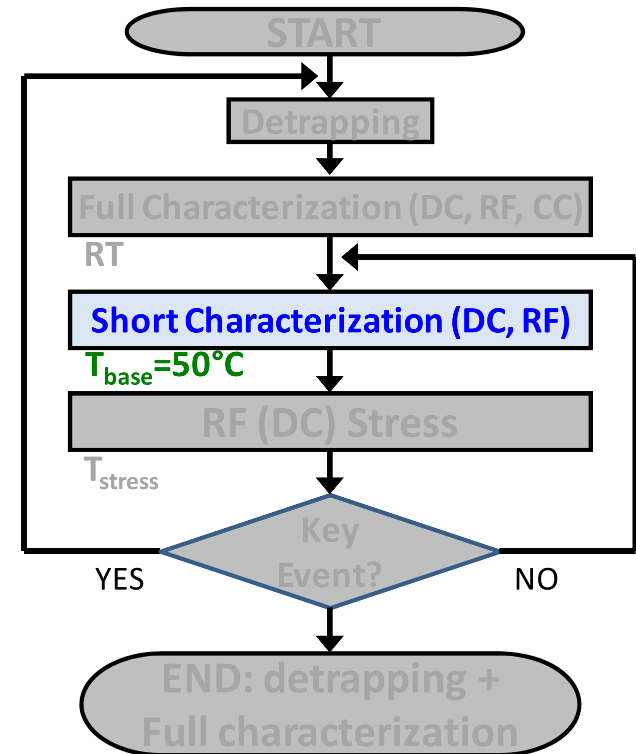
PAE



- RF FOMs changing because P_{in} changing
- Degradation apparent but not easily quantifiable

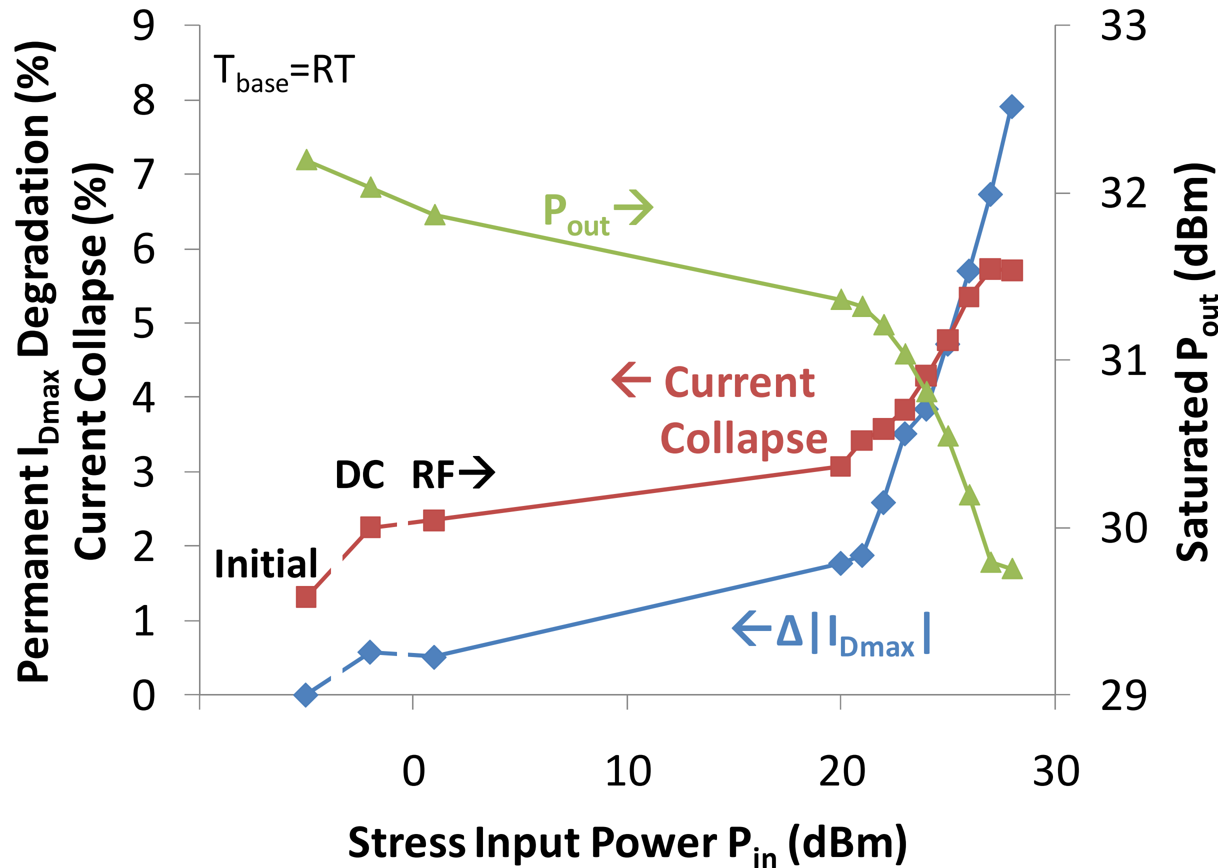
DC FOM during Short Characterization

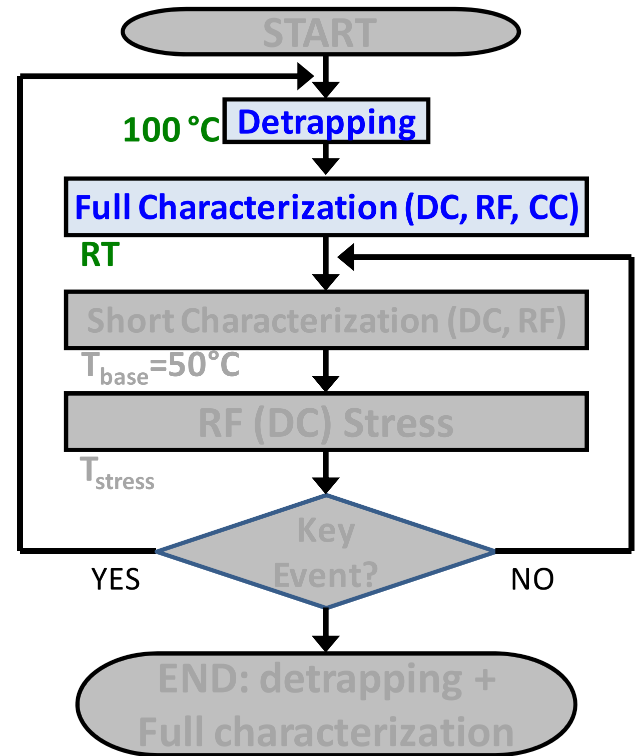




- Little degradation under DC and low P_{in}
- Beyond P_{in}=20 dBm:
  - RF induces degradation of I_{Dmax} and R_D
  - Sharp degradation in I_{Goff}

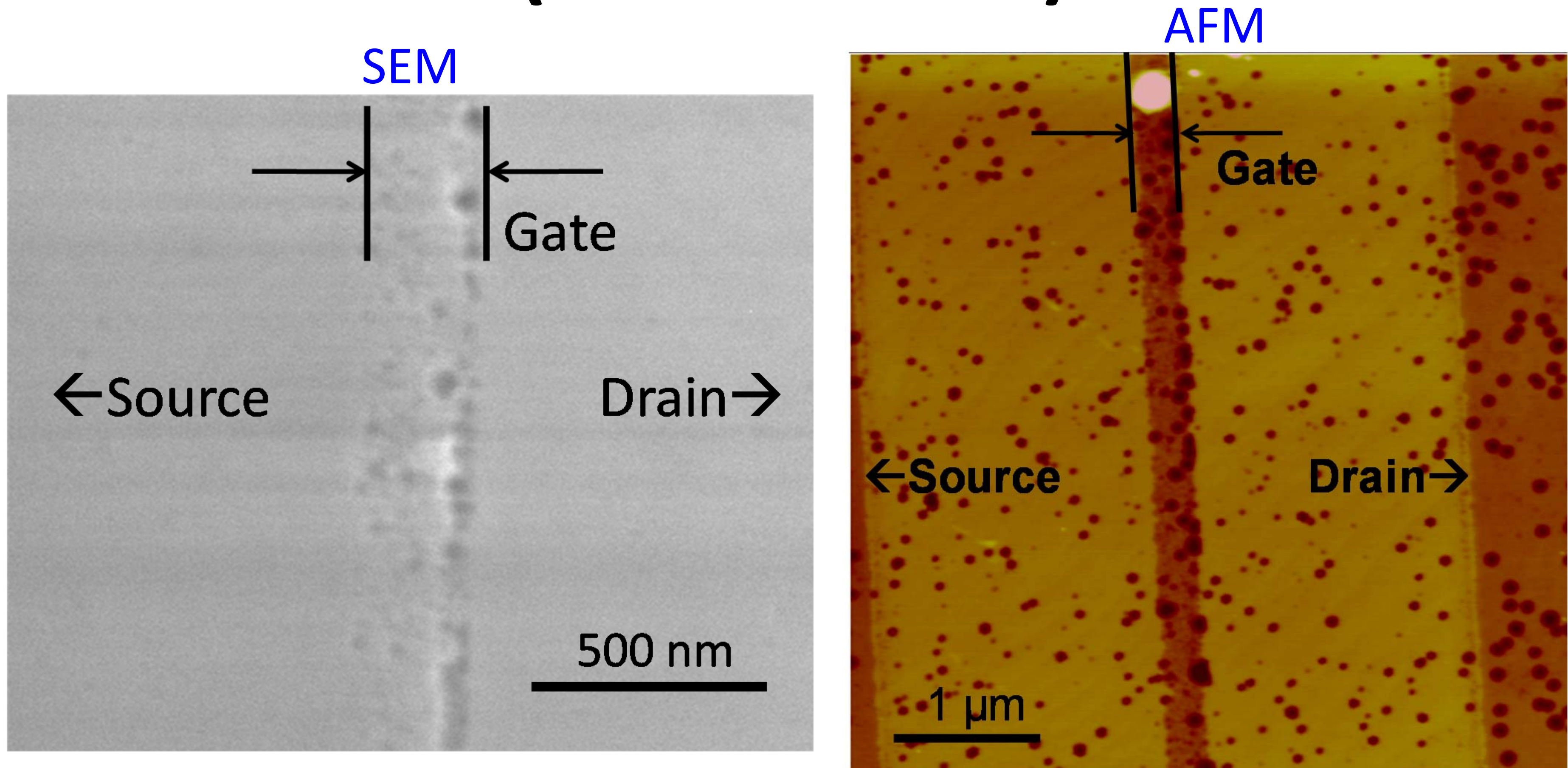
DC/RF/CC Full Characterization





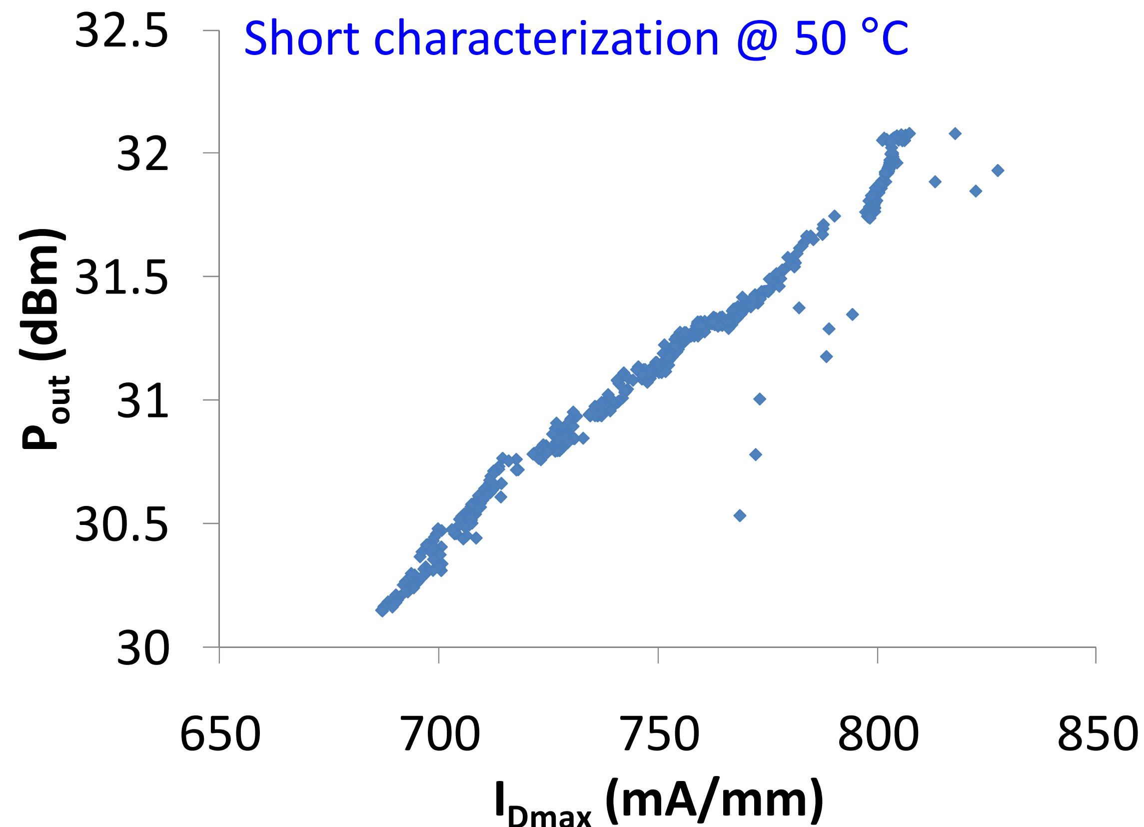
- Similar critical behavior. Beyond P_{in}=20 dBm:
  - Sharp P_{out} degradation
  - permanent degradation of I_{Dmax}
  - Evidence of new traps created (increased CC)

Structural Degradation (Planar View)



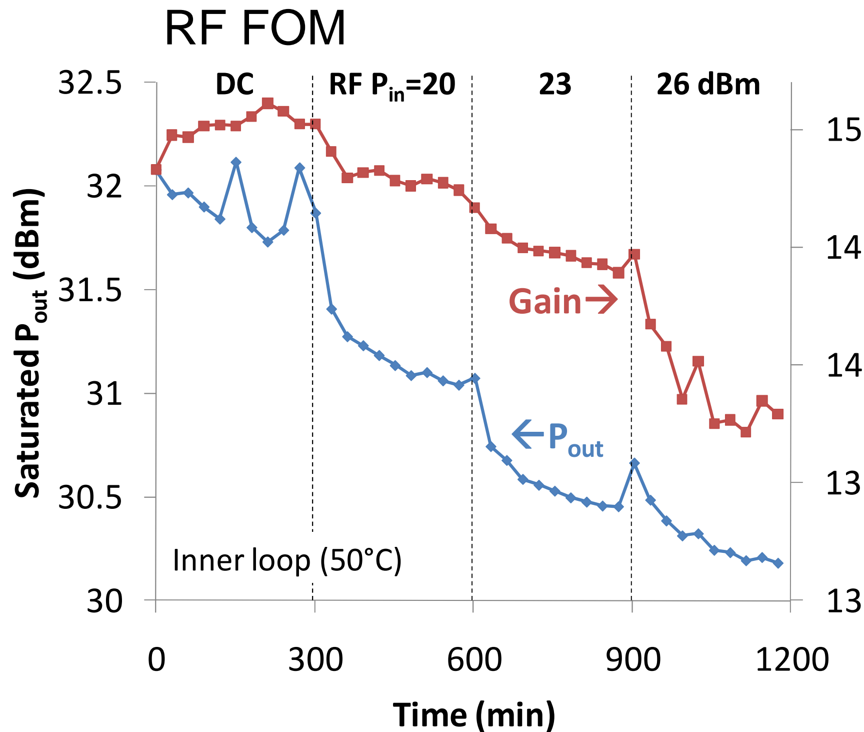
- Pit formation along the drain side of gate edge
- Same degradation mechanism as in DC high field OFF-state

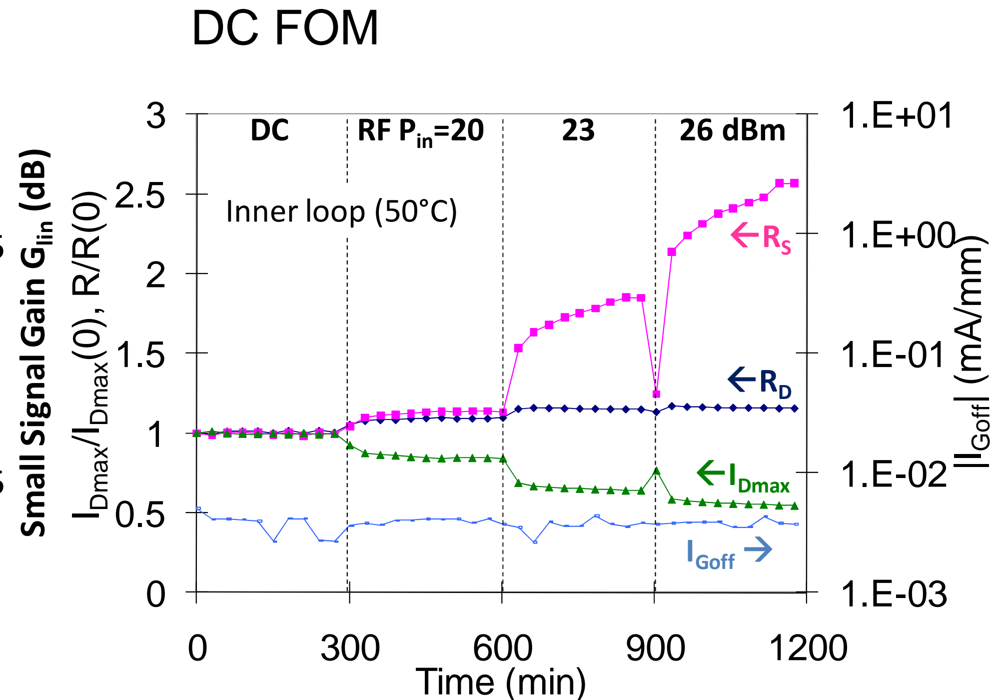
Correlation between DC and RF FOM



- Good correlation between P_{out} and I_{Dmax} degradation
  ΔP_{out}=1 dB ↔ ΔI_{Dmax} =9%

Step P_{in} Stress: Offset Gate

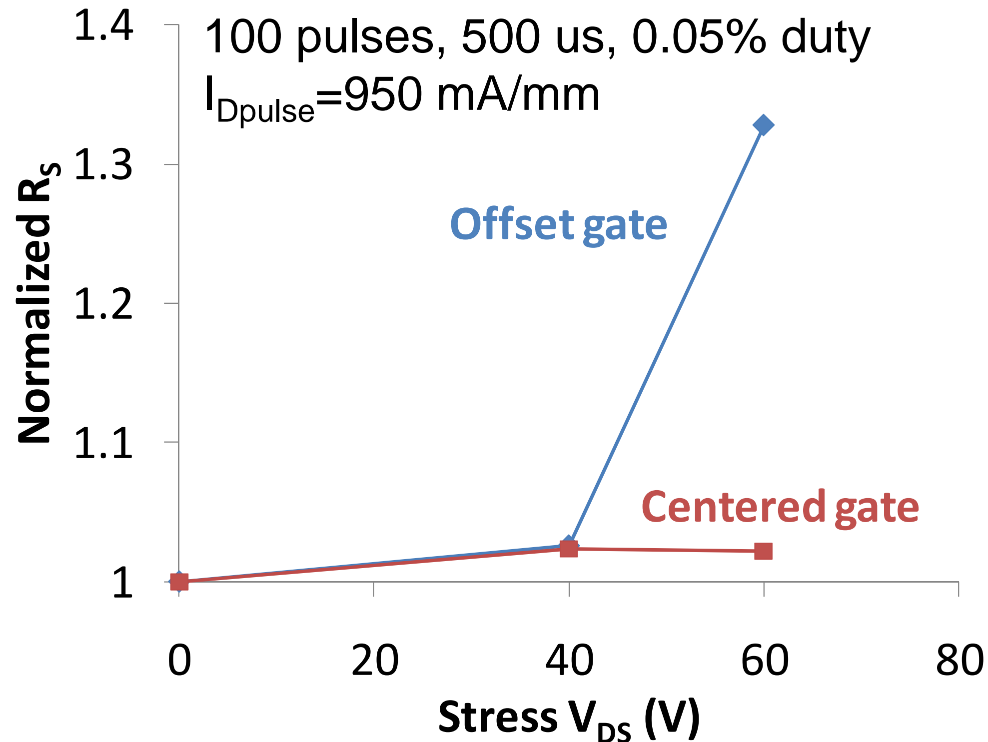


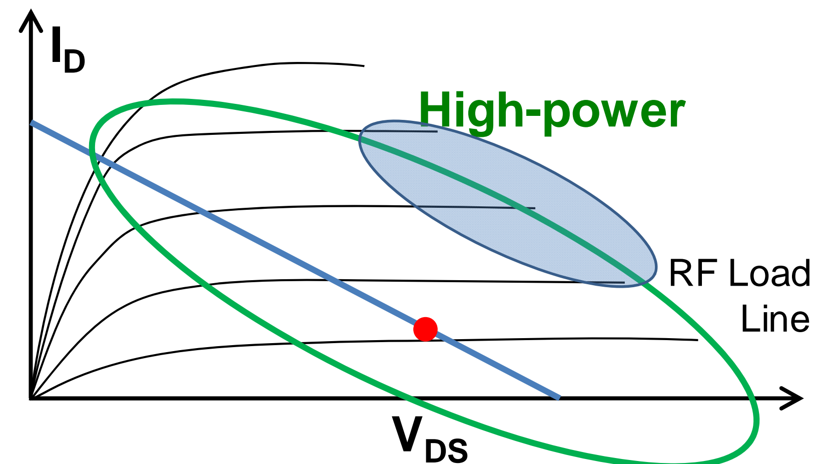


Joh, IEDM 2010

- More degradation under RF stress @ high P_{in}
- No I_{Goff} degradation (high V_{crit})
- Degradation in I_{Dmax} and R_S, not in R_D
- No structural degradation

Pulsed Stress: High-power State





- High-power stress not accessible in DC → pulsed stress
- Pulsed stress reproduces large R_S degradation in offset gate
- No R_S degradation in centered gate

Summary

- Developed new RF reliability testing methodology
- Critical behavior in RF stress on *centered gate*:
  - P_{in}↑ → P_{out}↓ (>> DC stress)
  - I_{Dmax}↓, current collapse↑, I_{Goff}↑
  - Good correlation between DC and RF FOMs
  - Structural degradation on drain-side gate edge
  - Same degradation mechanism under high-voltage OFF-state DC stress
- *Offset gate*:
  - Different degradation mechanism is present
  - Significant R_S degradation