III-V CMOS:

the key to sub-10 nm electronics?

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Microsystems Technology Laboratories, MIT

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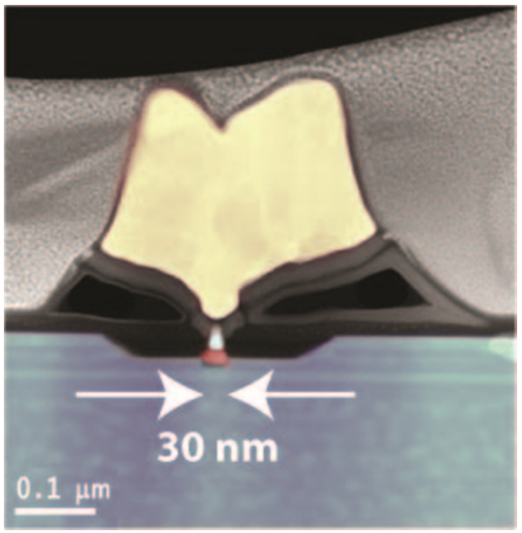
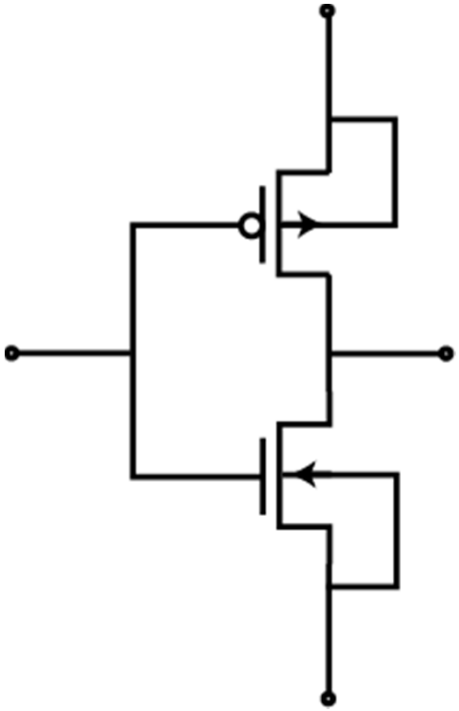
- Labs at MIT: MTL, NSL, SEBL



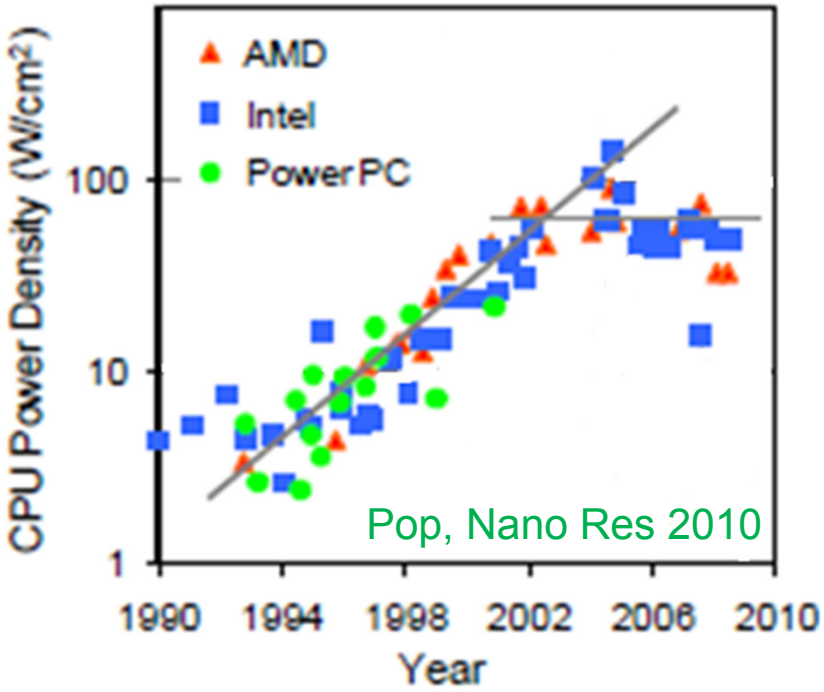
Outline

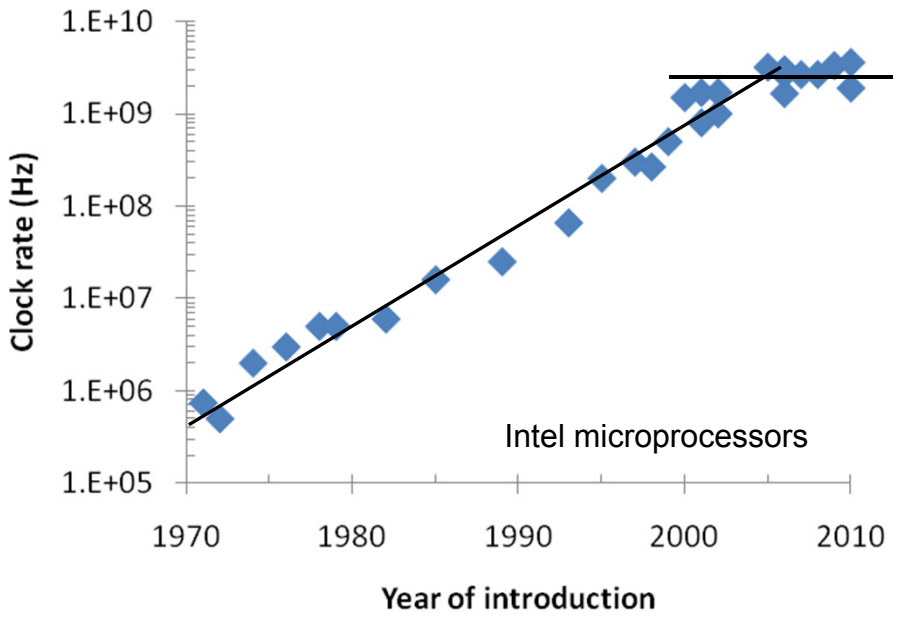


- Why III-Vs for CMOS?
- Lessons from III-V HEMTs
- The challenges for III-V CMOS
  - Critical problems
- How will a future 10 nm class III-V FET look like?
- Conclusions

CMOS scaling in the 21st century

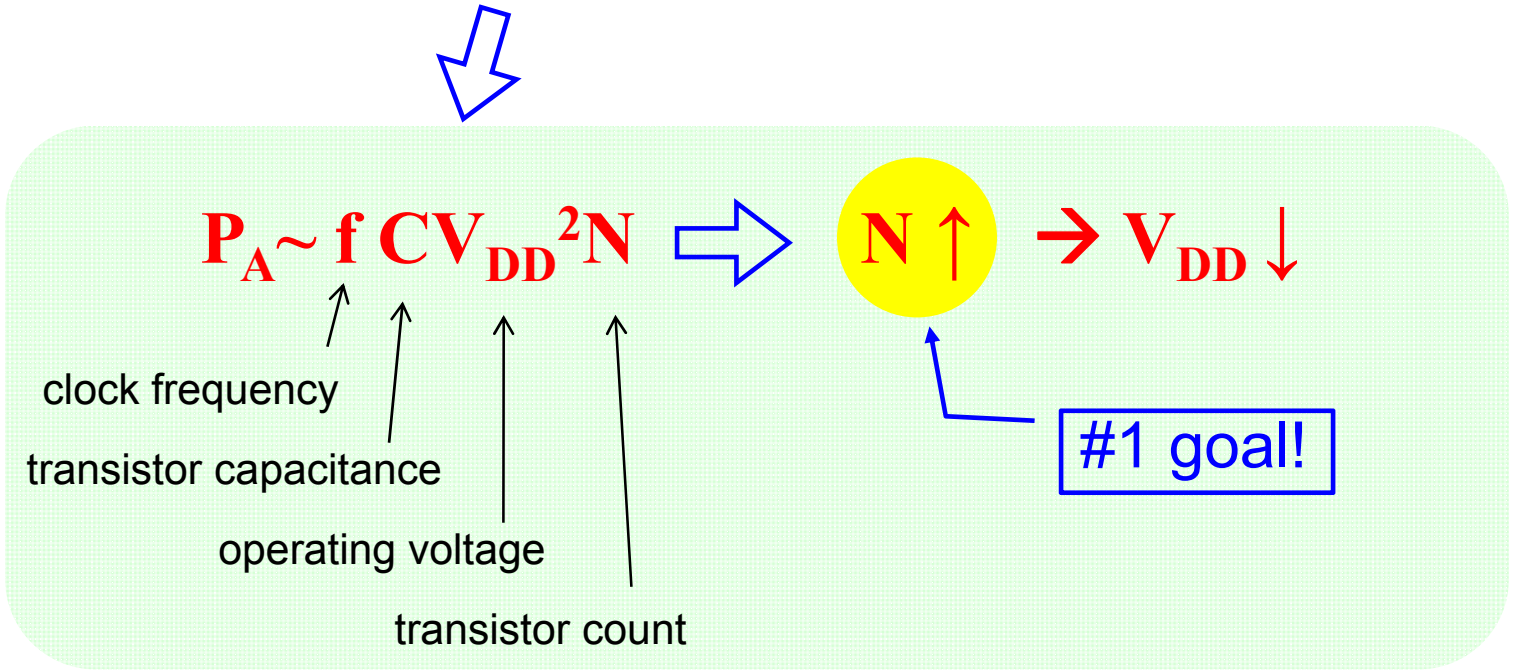
- Si CMOS has entered era of *"power-constrained scaling":*
  - Microprocessor power density saturated at ~100 W/cm^2
  - Microprocessor clock speed saturated at ~ 4 GHz





Consequences of Power Constrained Scaling

Power = active power + stand-by power

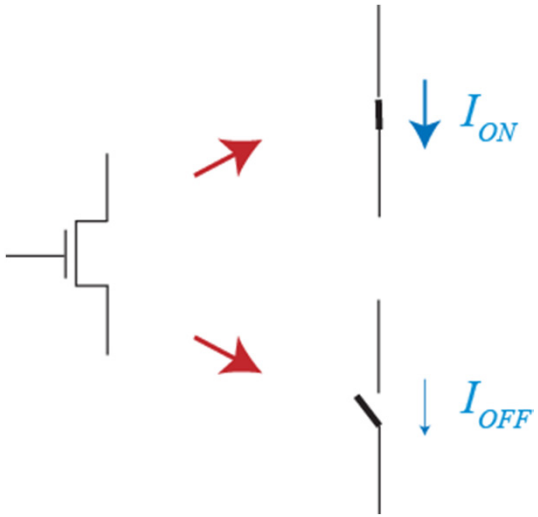


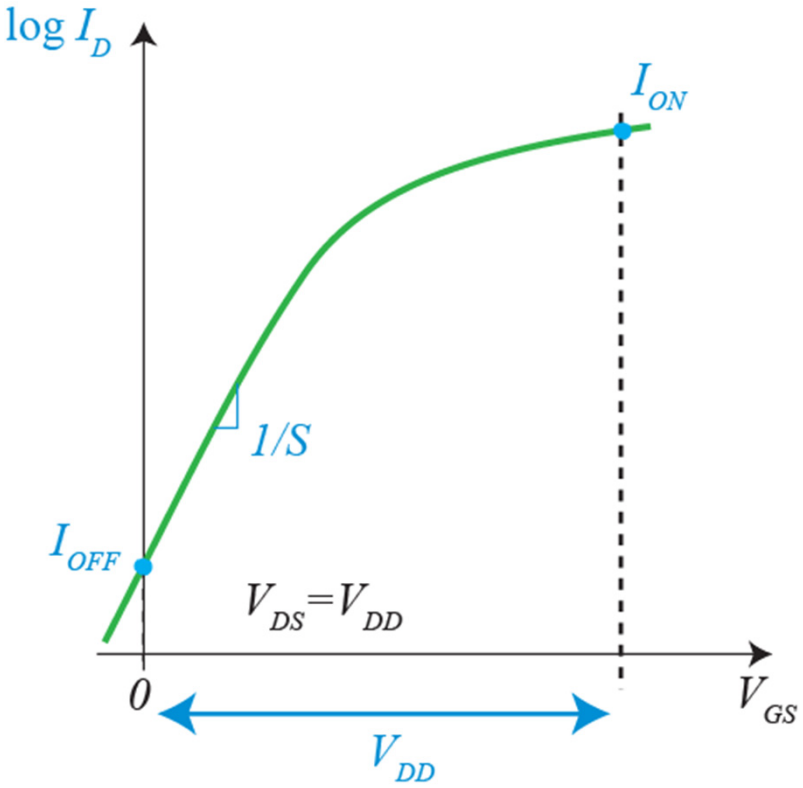
→ Transistor scaling requires reduction in supply voltage

→ Not possible with Si: performance degrades too much

How III-Vs allow further V_{DD} reduction?

- Goals of scaling:
  - reduce transistor footprint
  - extract maximum I_{ON} for given I_{OFF}





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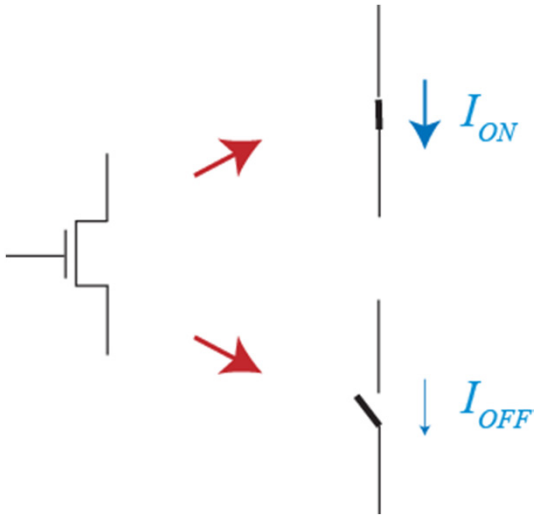
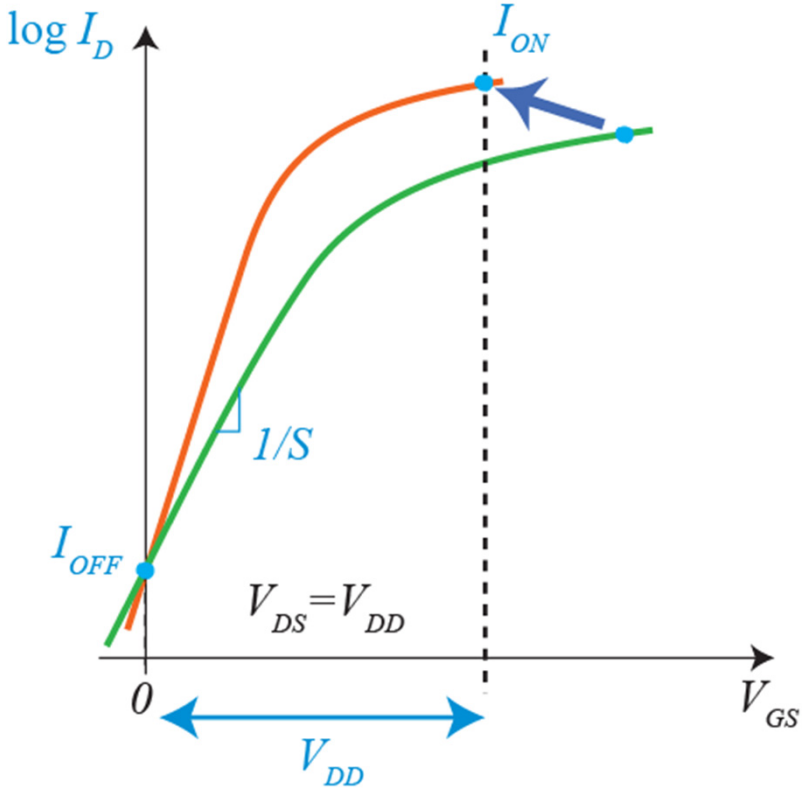
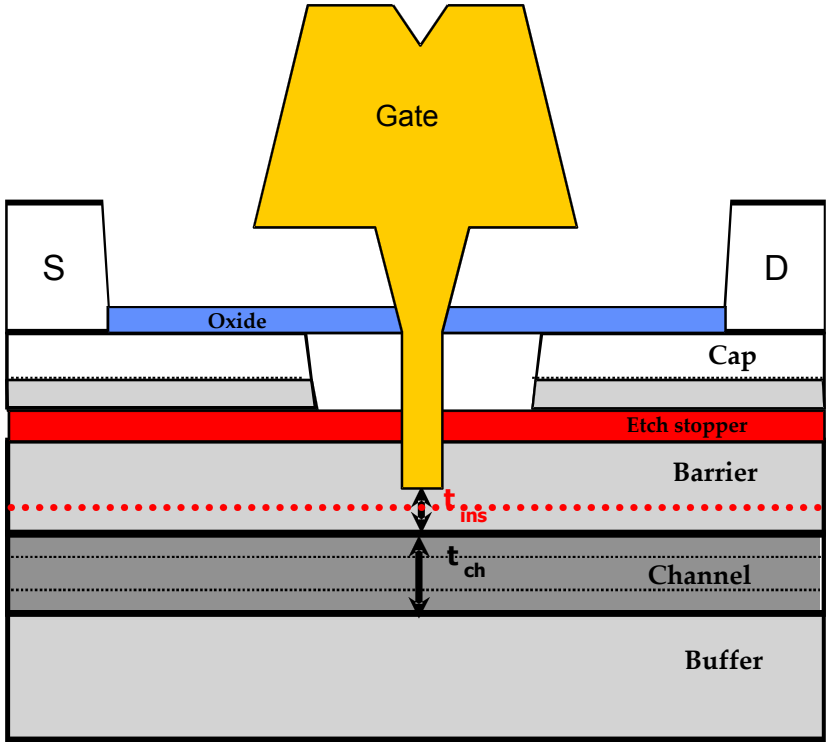
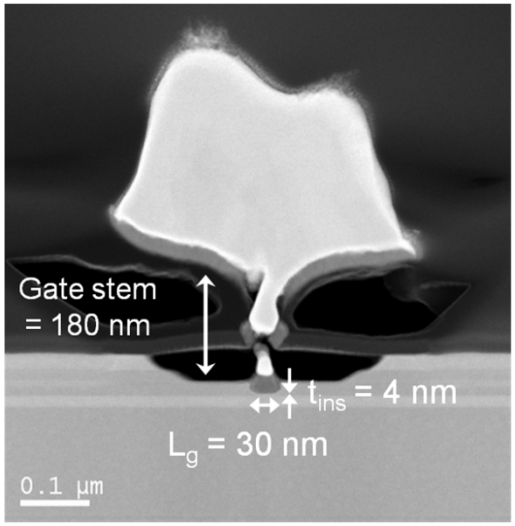




- III-Vs:
  - higher electron velocity than Si → I_{ON} ↑
  - tight carrier confinement in quantum well → S ↓ → sharp turn on

InAs High Electron Mobility Transistors



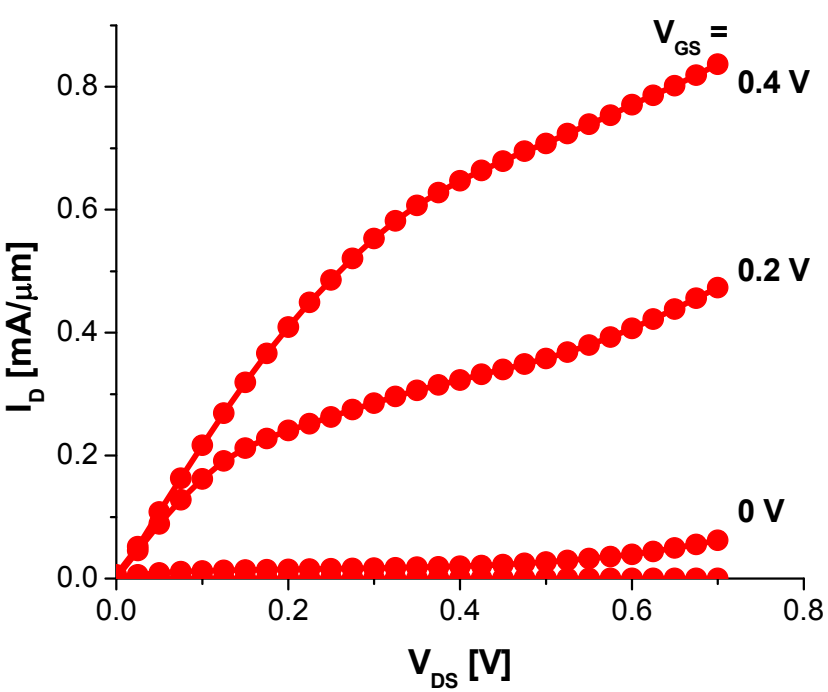


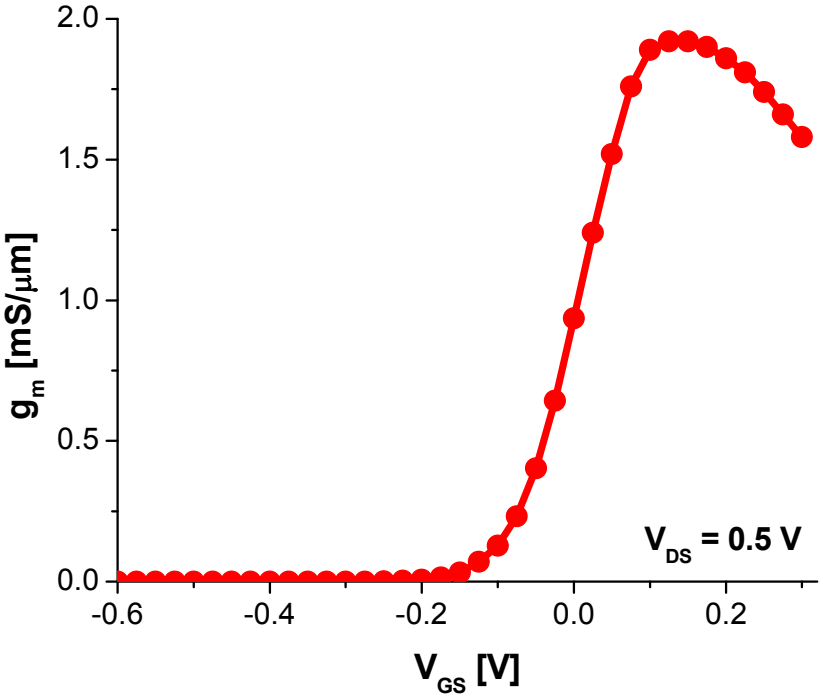
- QW channel (t_{ch} = 10 nm):
  - InAs core (t_{InAs} = 5 nm)
  - InGaAs cladding
- $\mu_{n,Hall}$ = 13,200 cm^2/V-sec
- InAlAs barrier (t_{ins} = 4 nm)
- Ti/Pt/Au Schottky gate
- L_g=30 nm

Kim, EDL 2010

L_g=30 nm InAs HEMT

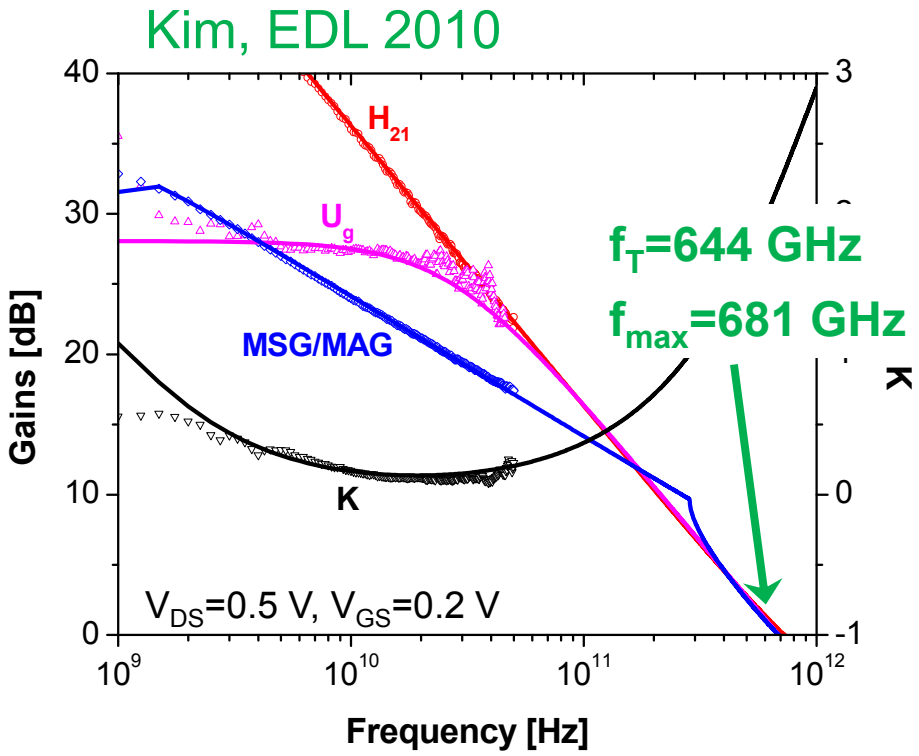
Kim, EDL 2010

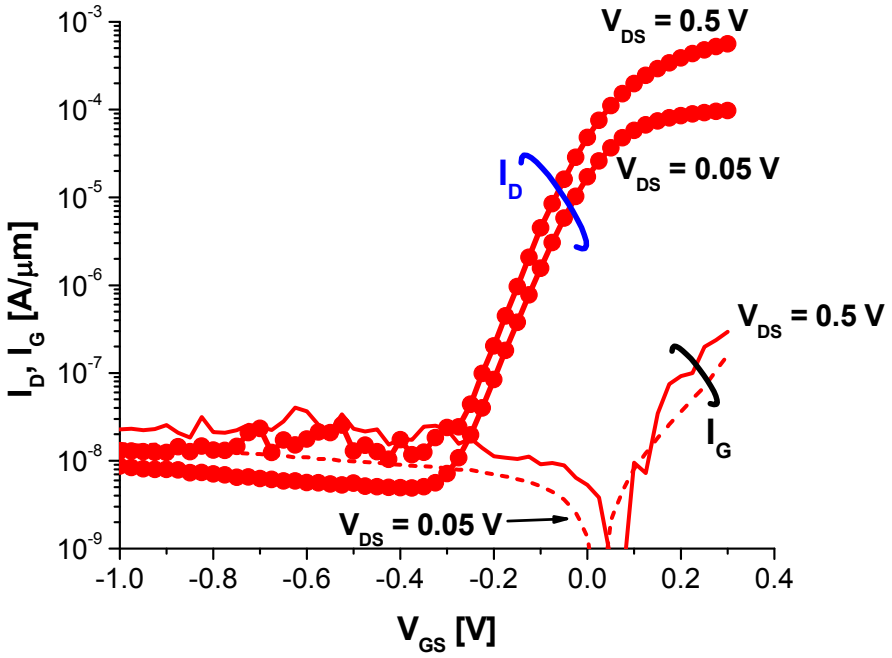




- Large current drive: I_{ON}>0.5 mA/μm at V_{DD}=0.5 V
- V_T = -0.15 V, R_S=190 ohm.μm
- High transconductance: g_{mpk}= 1.9 mS/μm at V_{DD}=0.5 V

L_g=30 nm InAs HEMT

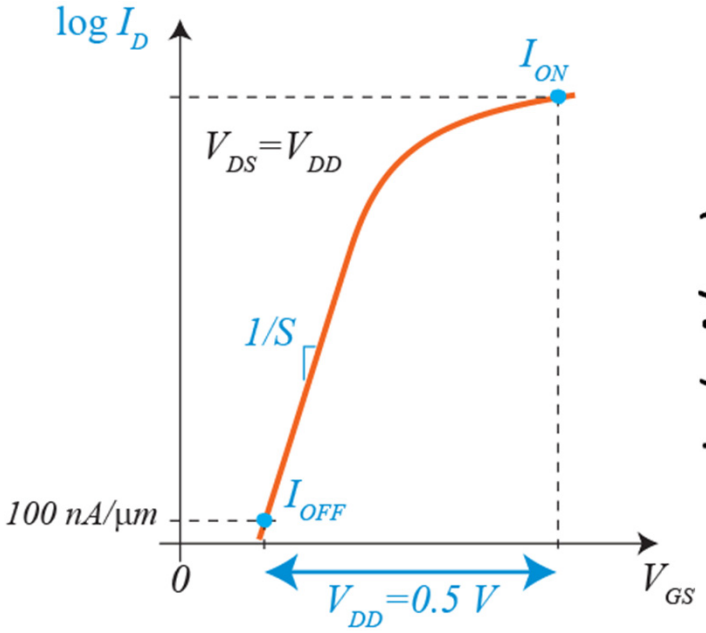


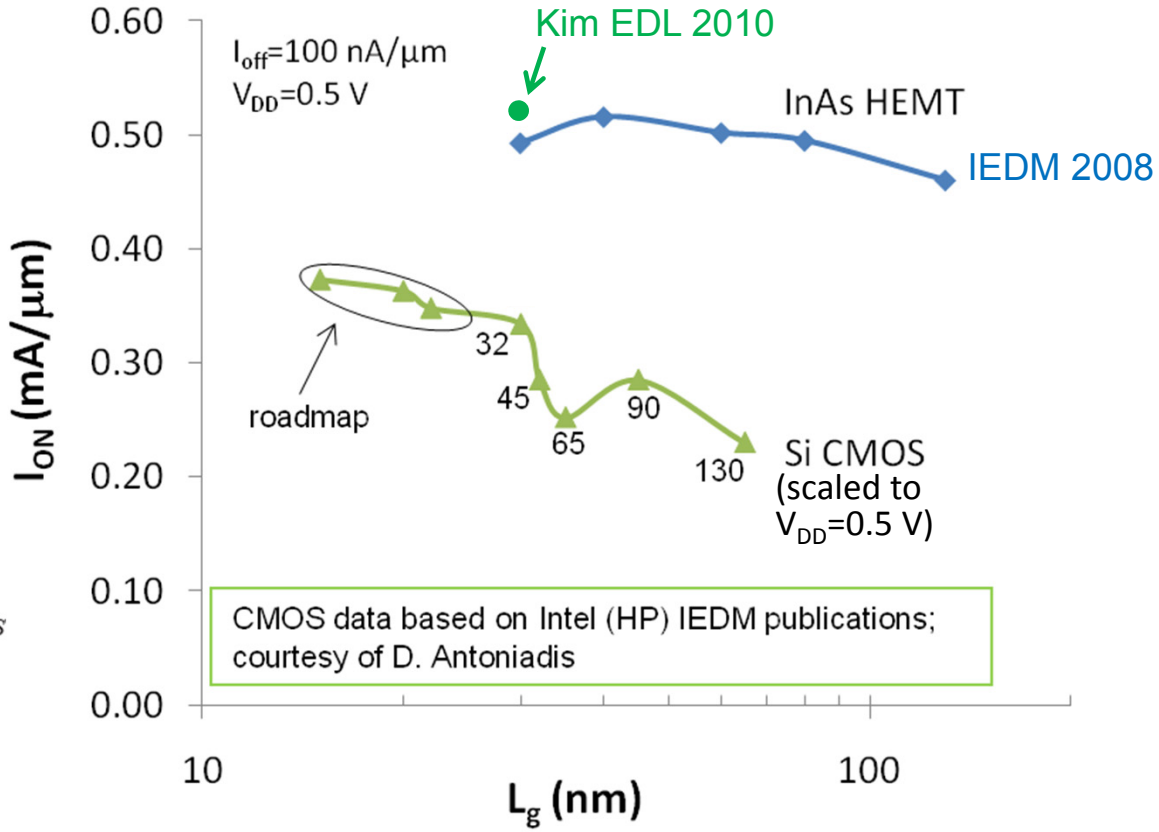


- FET with highest f_T in any material system
- Only transistor of any kind with both f_T and f_{max} > 640 GHz
- S = 74 mV/dec, DIBL = 80 mV/V, I_{on}/I_{off} ~ 5x10^3
- All FOMs at V_{DD}=0.5 V

InAs HEMTs: Benchmarking with Si

- FOM that integrates short-channel effects and transport:
  I_{ON} @ I_{OFF}=100 nA/μm, V_{DD}=0.5 V

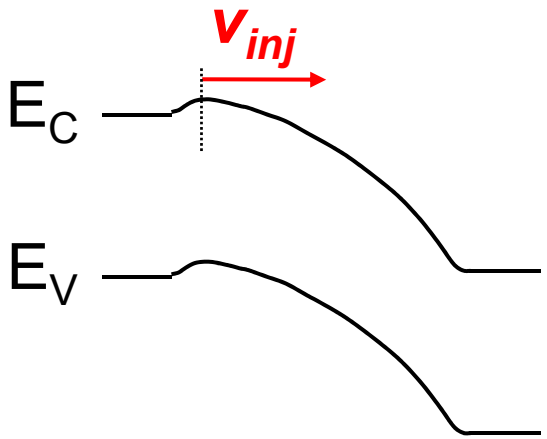




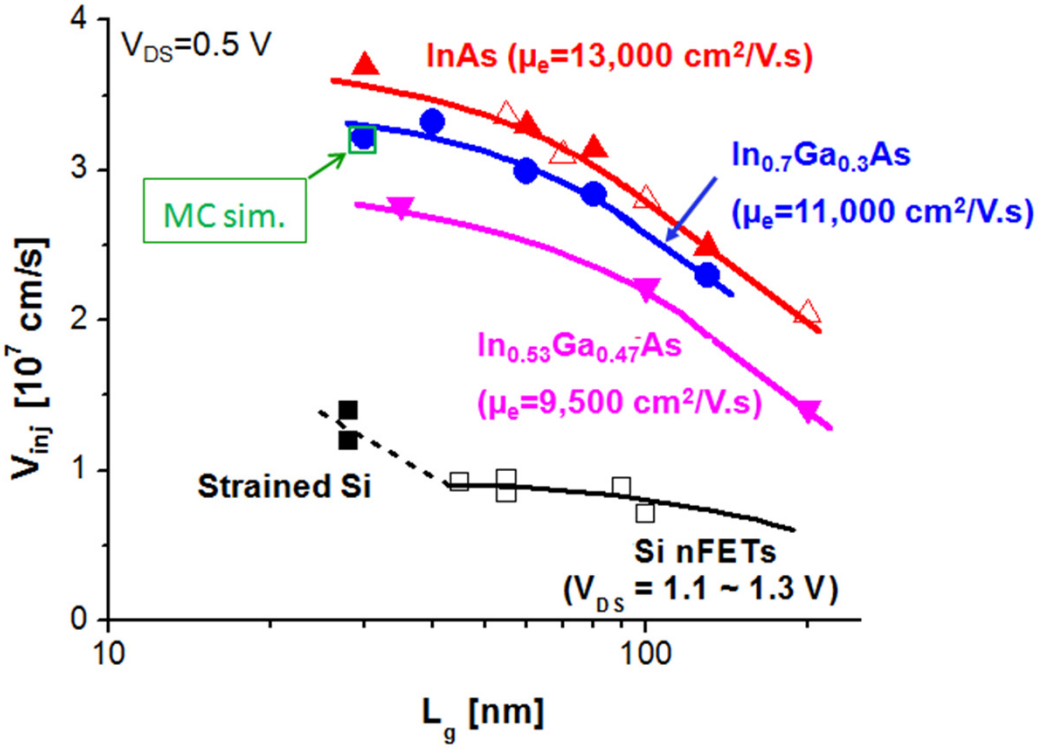
InAs HEMTs: higher I_{ON} for same I_{OFF} than Si

Why high I_{ON}?

1. Very high electron injection velocity at the virtual source



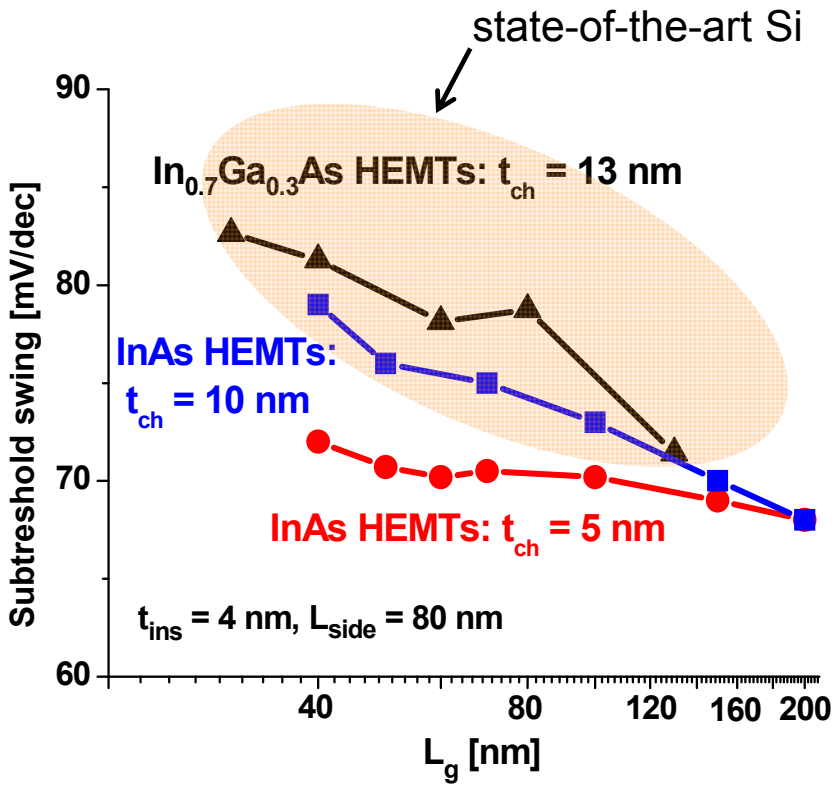
Kim, IEDM 2009
Liu, Springer 2010



- v_{inj}(InGaAs) increases with InAs fraction in channel
- v_{inj}(InGaAs) > $2v_{inj}$(Si) at less than half V_{DD}

Why high I_{ON}?

2. Sharp subthreshold swing due to quantum-well channel

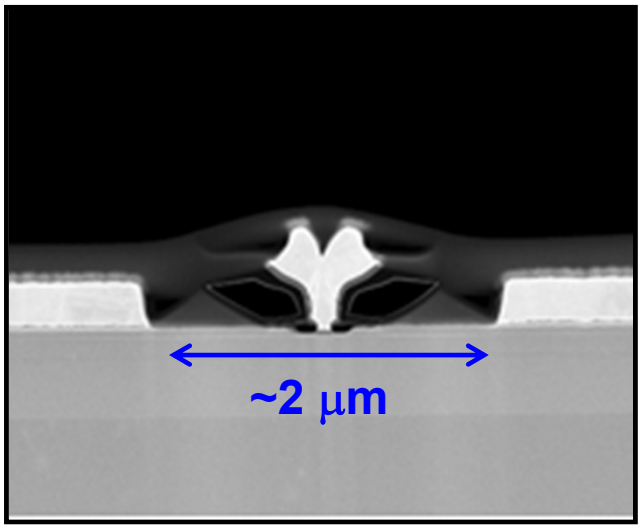


Kim, IPRM 2010

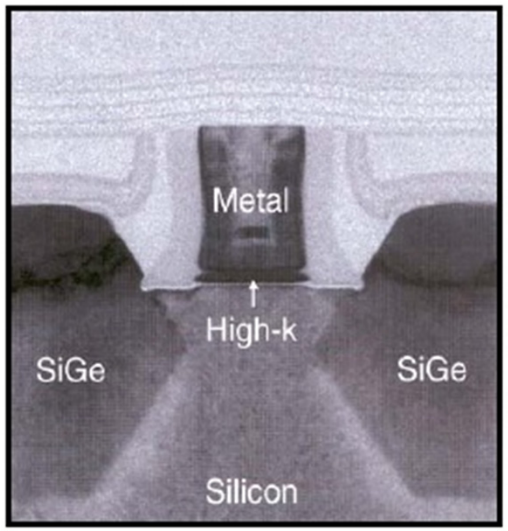
- Dramatic improvement in short-channel effects in thin channel devices

The Challenges for III-V CMOS: III-V HEMT vs. Si CMOS

III-V HEMT



Intel's 45 nm CMOS

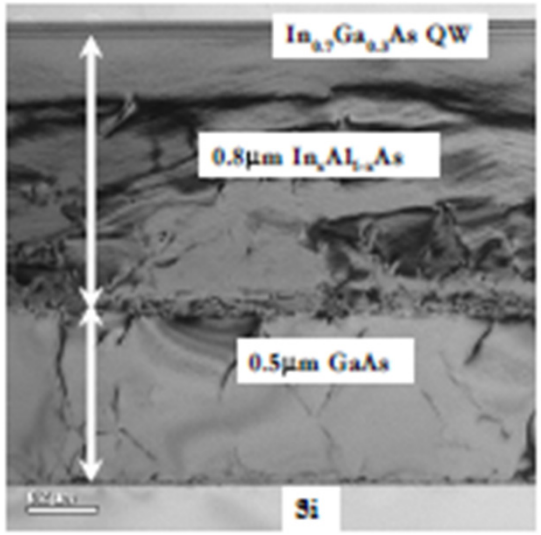


Critical issues:

- Schottky gate → MOS gate
- Footprint scaling [1000x too big!]
  - → Need self-aligned design
- p-channel device
- III-V on Si

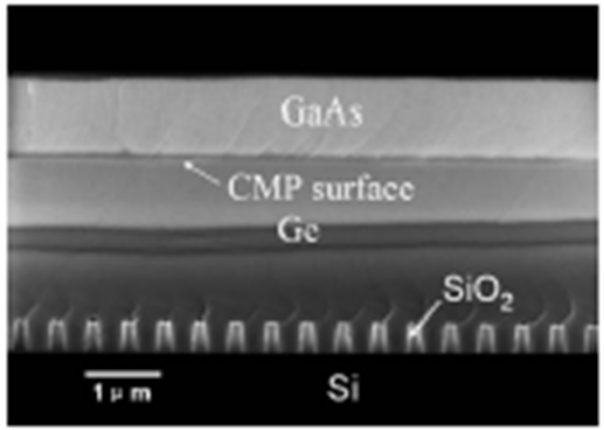
III-V's on Si

- The challenge:
  - III-V heterostructures on large-area Si wafers
  - Thin buffer layer
  - Low defectivity
- Some notable work:



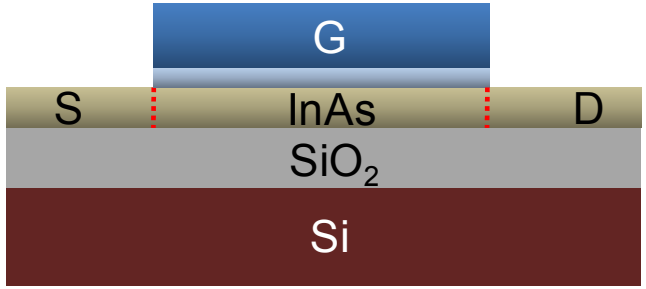
Direct III-V MBE on Si (Intel)

Hudait, IEDM 2007



Aspect Ratio Trapping + Epitaxial Lateral Overgrowth (Amberwave)

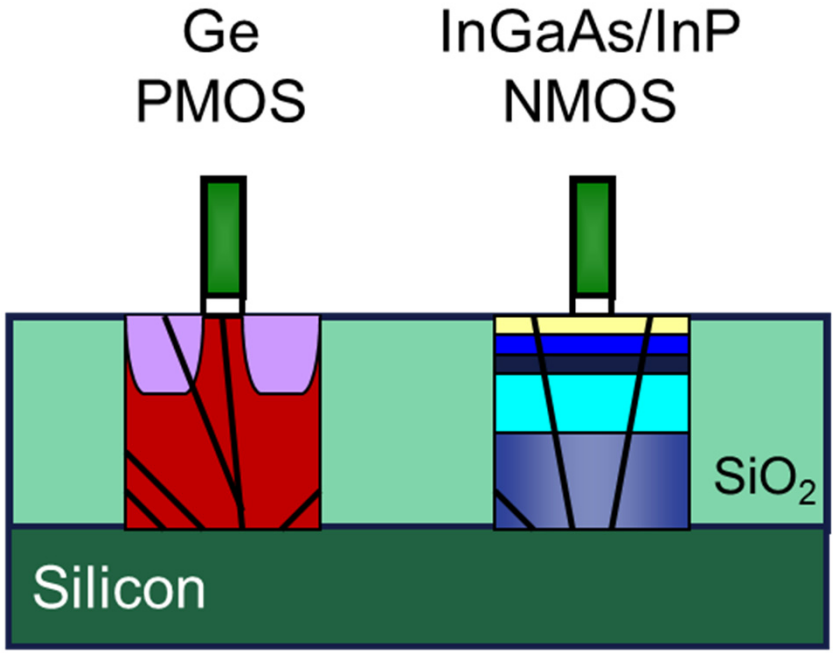
Fiorenza, ECS 2010



InAs Nanoribbon MOSFETs on Insulator (UC Berkeley)

Ko, Nature 2010

Critical problem: Integration of two different layer structures side-by-side on Si



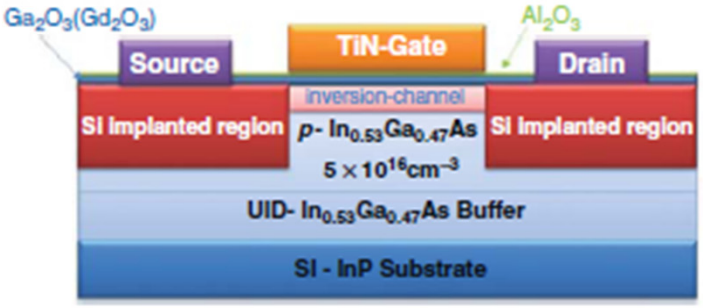
Fiorenza ECS 2010

Key issues:

- different lattice constants
- planar surface
- compact

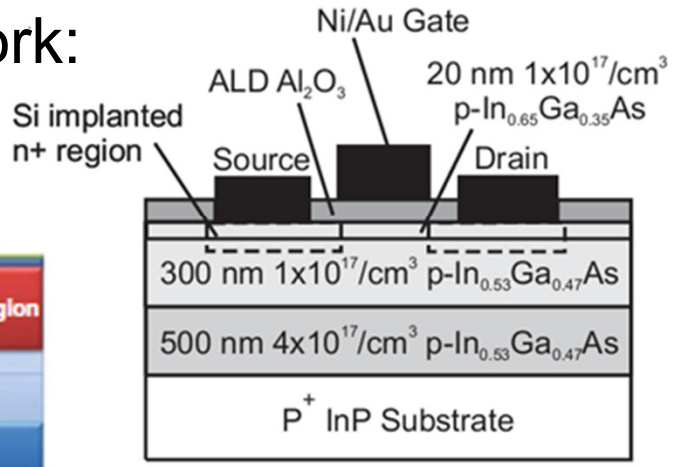
The gate stack

- Challenge: metal/high-K oxide gate stack
  - Fabricated through *ex-situ* process
  - Very thin oxide (EOT<1 nm)
  - Low leakage (I_G<10 A/cm^2)
  - Low D_{it} (<10^{12} eV^{-1}.cm^{-2} in top ~0.3 eV of bandgap)
  - Reliable
- Some notable work:



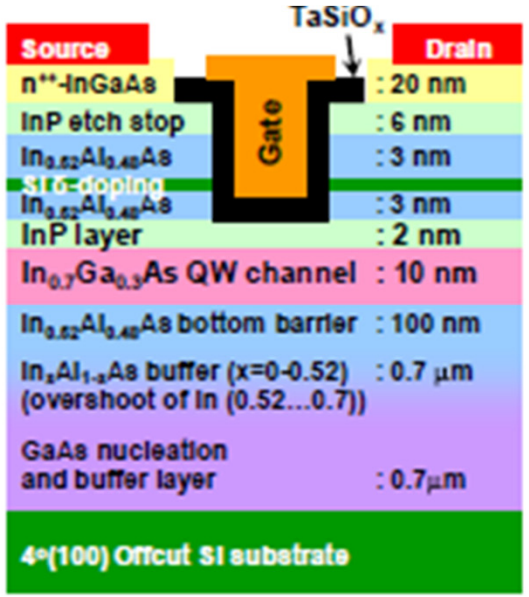
Al_2O_3 /GGO on InGaAs by MBE/ALD (Tsinghua)

Hong, MRS Bull 2009



Al_2O_3 by ALD (Purdue)

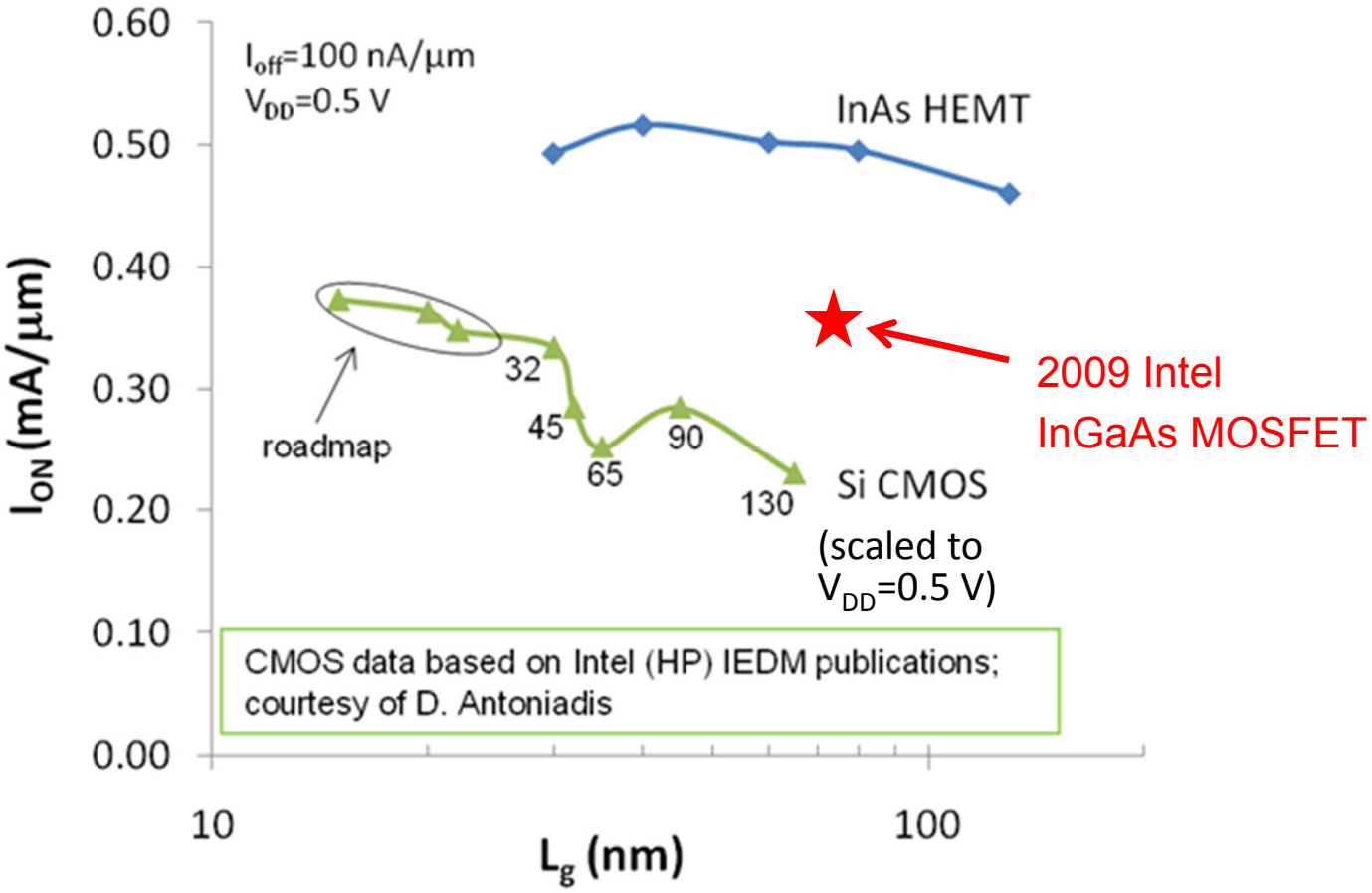
Wu, EDL 2009



$TaSiO_x$ on InGaAs by ALD (Intel)

Radosavljevic, IEDM 2009

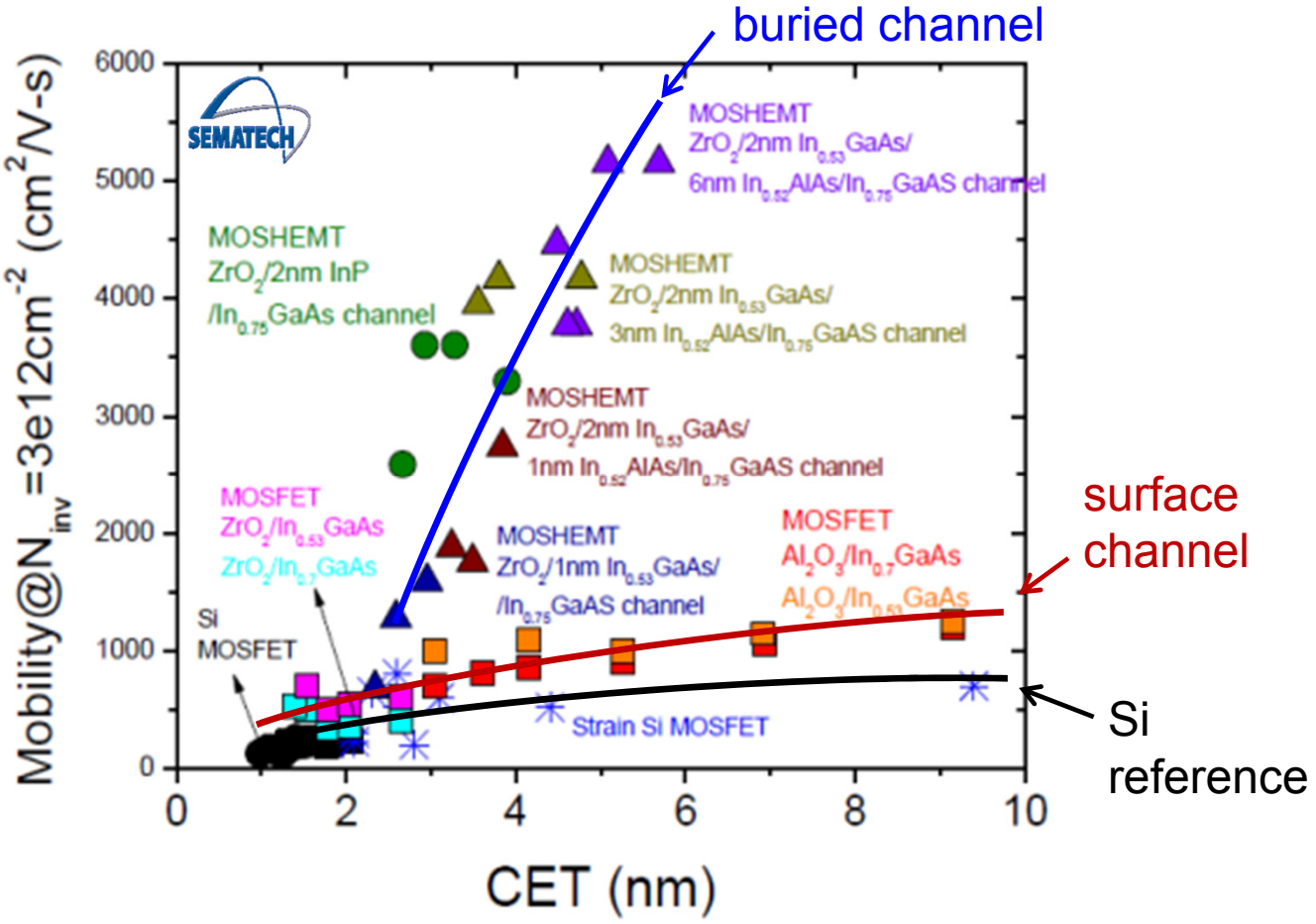
$In_{0.7}Ga_{0.3}As$ Quantum-Well MOSFET



L_g=75 nm InGaAs MOSFET outperforms state-or-the-art Si NMOS at 0.5 V

Radosavljevic, IEDM 2009

Critical problem: Mobility degradation in scaled gate stacks

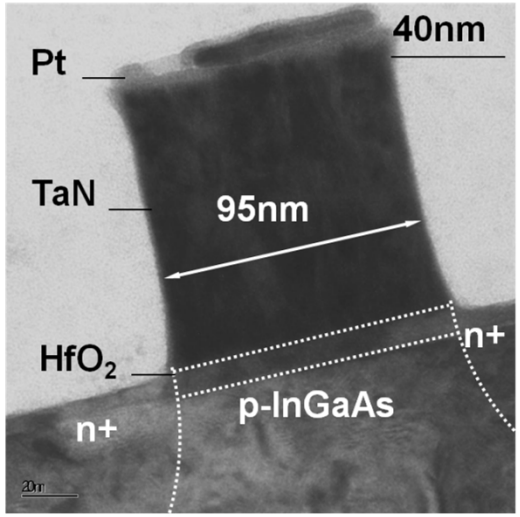


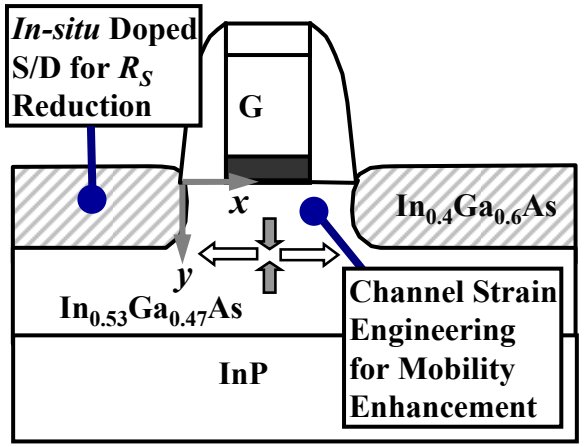
Graph courtesy of Prashant Majhi (Sematech)

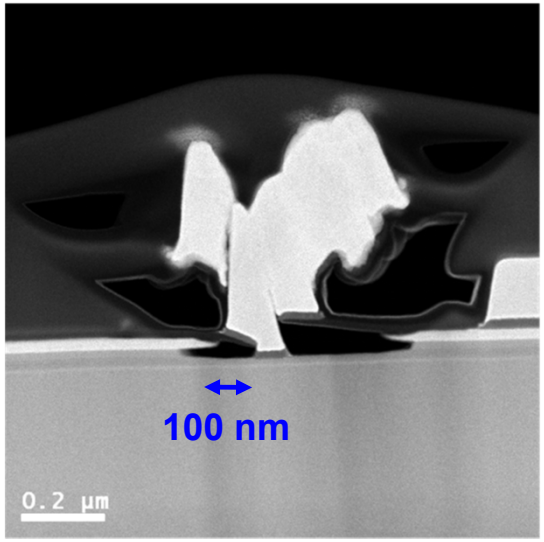
- μ advantage over Si erodes away in thin barrier structures
- Remote Coulomb scattering at oxide/semiconductor interface

Self-aligned device architecture

- The challenge:
  - MOSFET structures with scalability to 10 nm
  - Self-aligned gate design
- Some notable work:







Ion-implanted self-aligned InGaAs MOSFET (NUS)

Lin, IEDM 2008

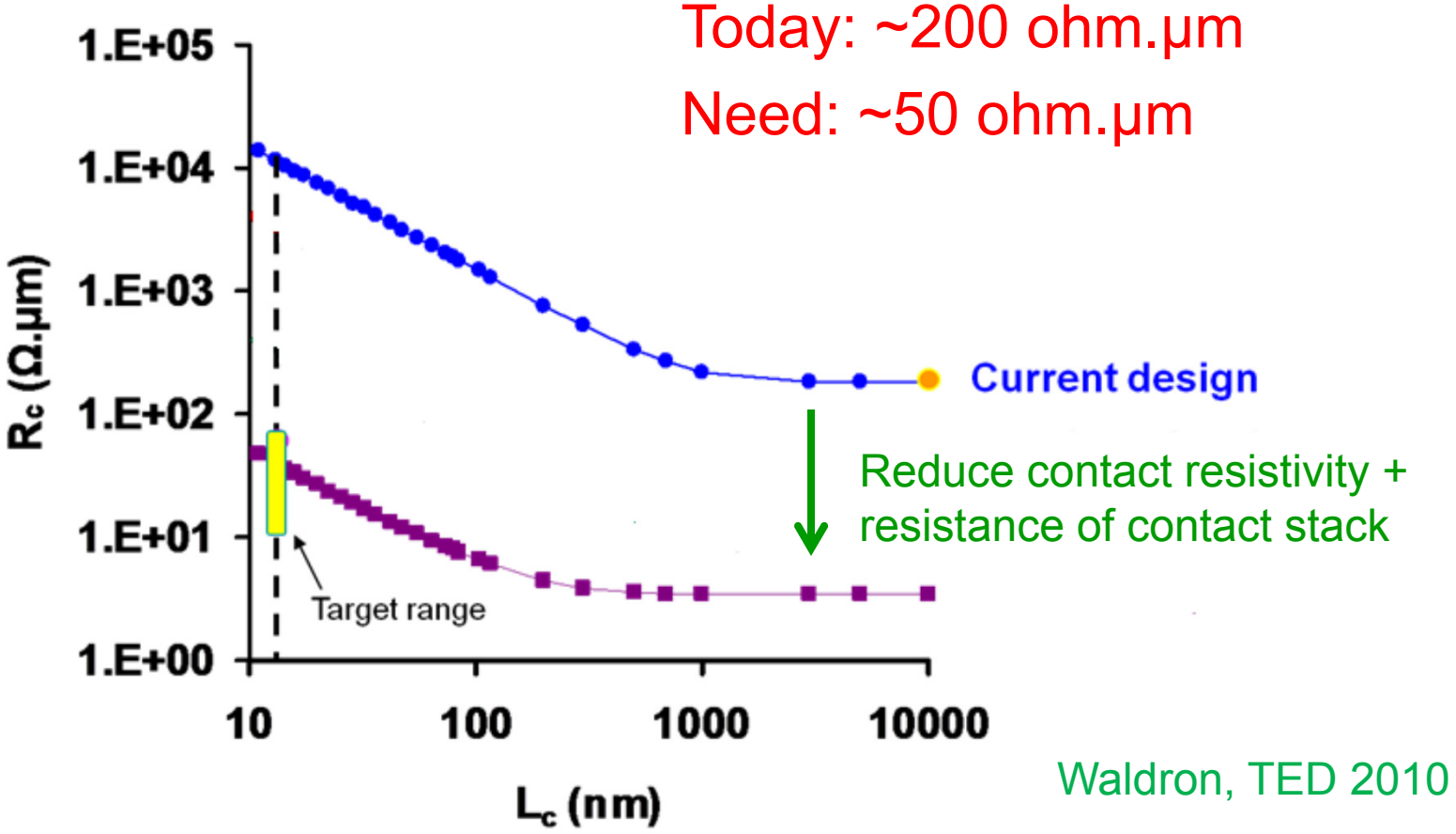
Regrown ohmic contact MOSFET (NUS)

Chin, EDL 2009

Quantum-well FET with self-aligned Mo contacts (MIT)

Kim, IEDM 2010

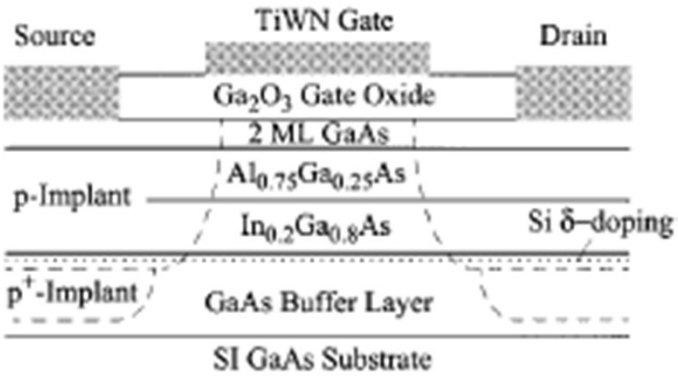
Critical problem: contact scaling



Current contacts to III-V FETs are >100X off in required contact resistance

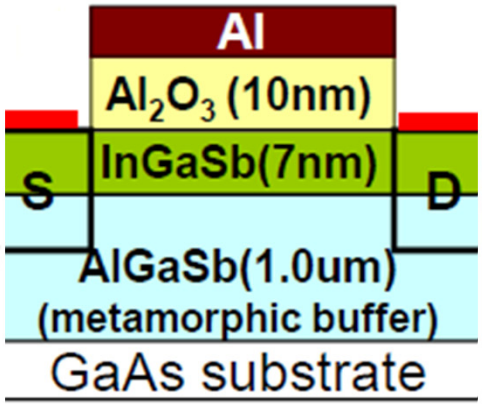
P-channel MOSFETs

- The challenge:
  - Performance >1/3 that of n-MOSFETs
  - Capable of scaling to <10 nm gate length regime
  - Co-integration with III-V NMOSFET on Si
- Some notable work:



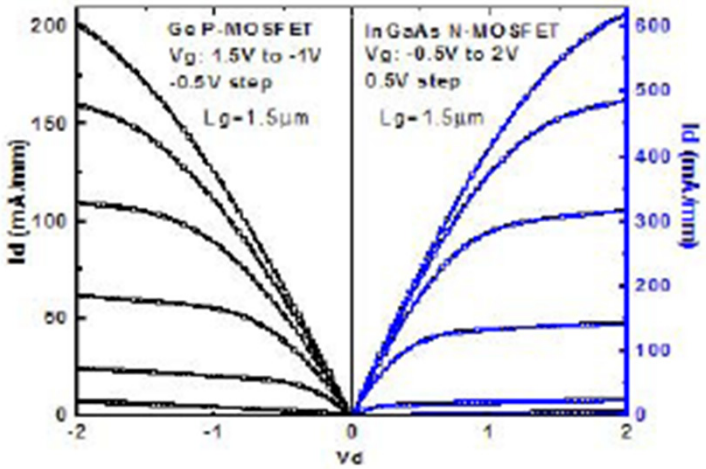
Ga_2O_3/AlGaAs/GaAs MOSFET (Motorola)

Passlack, EDL 2002



Al_2O_3/InGaSb QW-MOSFET (Stanford)

Nainani, IEDM 2010

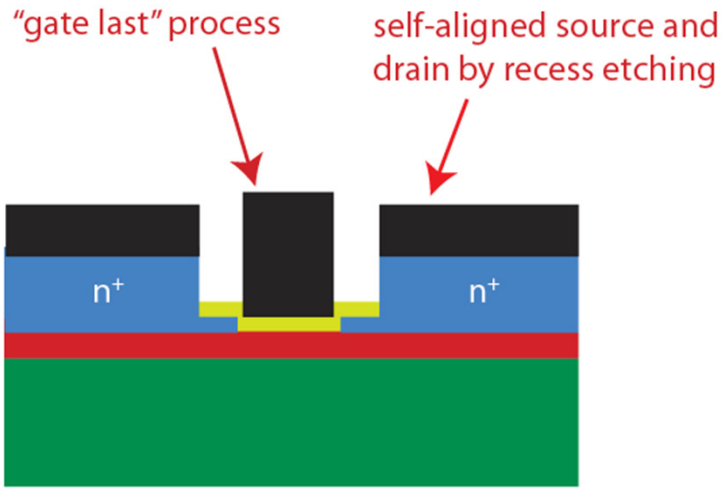


Al_2O_3 by ALD on InGaAs and Ge MOSFETs (IMEC)

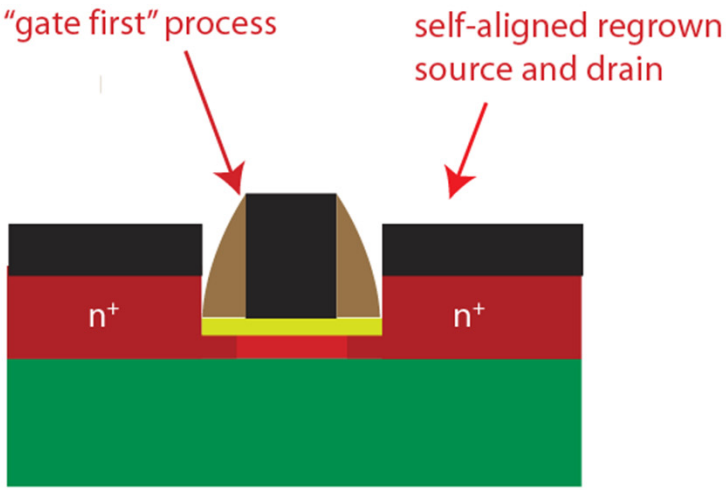
Lin, IEDM 2009

How will a future 10 nm-class III-V MOSFET look like?

- Quantum well + raised source/drain + self-aligned gate
- Two designs:



Recessed gate



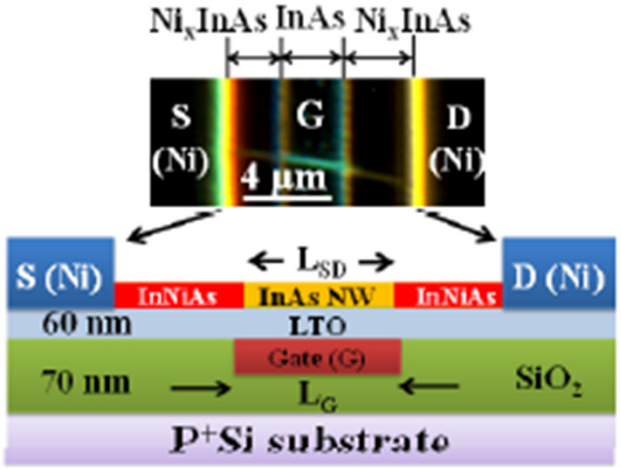
Regrown source and drain

- QW extends under S/D
  → high μ preserved
- Critical interface protected until late in process

- More freedom for S/D region design
- Uniaxial strain possible

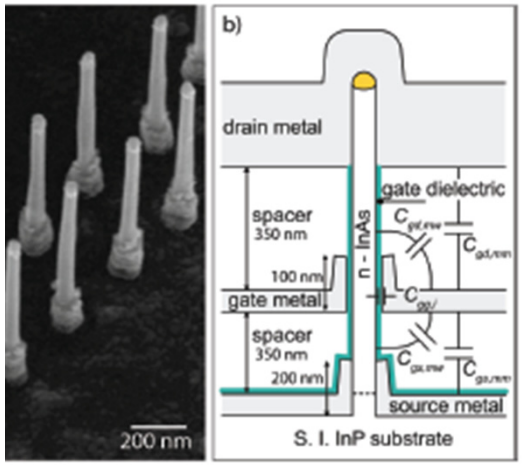
Critical problem: planar FET might not meet electrostatics requirements

- Electrostatic integrity might demand 3D III-V MOSFET structures
- Some notable work:



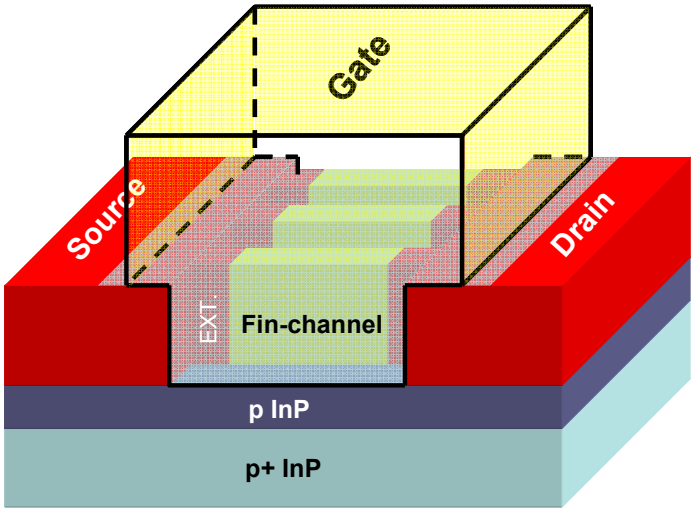
InAs Nanowire FETs (UC Berkeley)

Chueh, NanoLett 2008



InAs Vertical Nanowire FETs (Lund)

Egard, NanoLett 2010



InGaAs FinFET (Purdue, Intel)

Wu, IEDM 2009
Radosavljevic, IEDM 2010

Conclusions

- III-Vs attractive for CMOS: key for low V_{DD} operation
  - Electron injection velocity > 2X that of Si at 1/2X V_{DD}
  - Quantum-well channel yields outstanding short-channel effects

- Impressive recent progress on III-V CMOS
  - Ex-situ ALD and MOCVD on InGaAs yield interfaces with unpinned Fermi level and low defect density
  - Sub-100 nm InGaAs MOSFETs with I_{ON} > than Si at 0.5 V demonstrated

- Lots of work ahead
  - Demonstrate 10 nm III-V N-MOSFET that is better than Si
  - P-channel MOSFET
  - N-channel + P-channel cointegration