Time Evolution of Electrical Degradation under High-Voltage Stress in GaN High Electron Mobility Transistors

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***Abstract*—In this work, we investigate the time evolution of electrical degradation of GaN high electron mobility transistors under high voltage stress in the OFF state. We found that the gate current starts to degrade first, followed by degradation in current collapse and eventually permanent degradation in I_D. We also found that the time evolution of gate current degradation is unaffected by temperature, while drain current degradation is thermally accelerated.**

Keywords-GaN, HEMT, reliability, degradation, time evolution

I. INTRODUCTION

In GaN high electron mobility transistors (HEMTs), electrical reliability remains a key concern. To address reliability issues, it is critical to develop detailed physical understanding of the mechanisms behind device degradation. High-voltage stress has been found to result in device degradation with a critical voltage behavior [1-2] and characterized by trap formation and trapping [3-4]. To date, few studies have investigated the time evolution of degradation under high-voltage stress conditions [3, 5-8]. Some of these studies focused on the evolution of the gate/drain leakage current [6, 8]. Although there have been efforts to understand the time evolution of the drain current [3], its detailed nature is still largely unknown. This is important in order to develop degradation models that can predict device lifetime under given operational conditions.

In this work, we investigate the time evolution of degradation in the gate and drain currents and other figures of merit under high voltage stress with voltages in excess of the critical voltage. In particular, we separately monitor permanent and trapping-related degradation of the drain current, as well as degradation in the gate current [9]. We have found that there is an *incubation time* during which degradation does not take place and that this incubation time is different for different device figure of merits. The temperature dependence of this incubation time is also different. The incubation time for gate current degradation was found to be almost temperature independent while that of the drain current degradation was thermally activated.

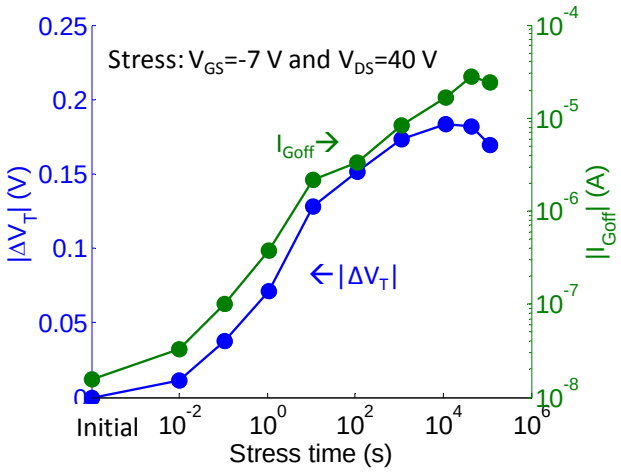
II. EXPERIMENTAL

We have studied 0.25 μm GaN HEMTs on SiC [10]. The device width is 2x25 μm. We performed OFF-state stress at V_{GS}=-7 V and V_{DS}=40 V. This voltage was much larger than the critical voltage at which sudden gate current degradation takes place (typical V_{DGcrit} for these devices is about 20 V at 150 °C) [1]. These experiments were performed at various base-plate temperatures between 75 and 150 °C. Throughout the experiment, at regular intervals, we performed detailed device characterization at 30°C, including comprehensive trapping analysis [4]. The effect of stress times as short as 10 ms and as long as several days was studied.

Among various figures of merit that we monitored at 30°C, we focused on reverse-bias gate leakage current I_{Goff} (I_G at V_{GS}=-5 V, V_{DS}=0.1 V), permanent degradation in I_{Dmax} (I_D at V_{GS}=2 V, V_{DS}=5 V) and I_{Dlin} (I_D at V_{GS}=1 V and V_{DS}=0.5 V), and drain current collapse (a measure of trapping related degradation). We have also monitored linear threshold voltage (defined as V_{GS} at I_D=1 mA/mm for V_{DS}=0.1 V). Permanent degradation was defined as the decrease in uncollapsed I_{Dmax} (or I_{Dlin}) that is measured after a detrapping step where the device was illuminated with microscope light for 30 s. We use the term "permanent" because this degradation is completely irreversible after light illumination, heating up to 150 °C, or waiting for 1 month. This is unlike drain current collapse which can be reversed by electron detrapping. Our definition of uncollapsed or permanent I_D reflects device behavior with most of the traps empty after a detrapping step [4].

In order to measure drain current collapse, we performed I_D transient measurements where trapping was produced by applying a 1 s voltage pulse with V_{GS}=-10 V and V_{DS}=0 V [4]. The collapsed value of I_{Dlin} was measured 10 ms after the removal of the pulse. We used I_D in the linear regime for the current collapse measurements in order to suppress self-heating and measurement-induced trapping [4]. Current collapse was defined as the relative change in I_{Dlin} before and after the trapping pulse.

These experiments were performed on devices that are located side by side in a small chip (~10 mm^2) and thus have closely matched characteristics. This allowed us to compare different stress conditions in a consistent manner.



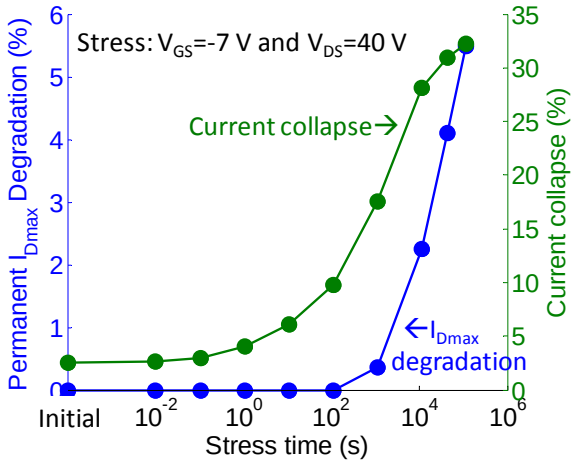


Fig. 1. Time evolution of I_{Goff}, V_T (actual change is negative. See Fig. 4), current collapse, and permanent I_{Dmax} degradation for a device stressed in the OFF state (V_{GS}=-7 V, V_{DS}=40 V) at 125 °C. Device characterization was performed at 30 °C.

III. TIME EVOLUTION OF DEGRADATION

Fig. 1 shows the time evolution of V_T, I_{Goff}, I_{Dlin} current collapse, and permanent I_{Dmax} degradation for a device stressed at T_{base}=125 °C. The gate current is seen to increase even after just 10 ms of stressing. It eventually tends to saturate after a 2-3 orders of magnitude increase, although this takes as long as ~10^4 s. The threshold voltage changes in a similar way to I_{Goff}. On the other hand, degradation of the drain current, permanent or trapping related is a significantly slower process. It can be seen that there is an incubation time for which negligible degradation occurs in current collapse and permanent I_{Dmax} degradation (uncollapsed I_{Dlin} behaves in a similar way). Current collapse starts to increase at around 10 s of stress time and tends to saturate at ~10^4 s. Permanent degradation in drain current (non-trapping related) starts even later – it took more than 1000 seconds to see noticeable permanent degradation – and it does not seem to saturate.

Detrapping analyses at various times during the experiment reveal that the increase in current collapse originates from two different sources. As shown in the time constant spectrum (described in more detail in [4]) in Fig. 2, a detrapping component with a well defined time constant (marked as DP1)

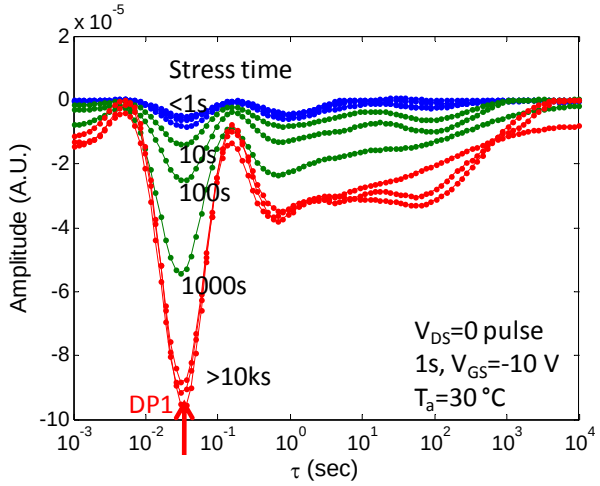


Fig. 2. Time constant spectra of detrapping transients after 1s V_{DS}=0 pulse with V_{GS}=-10 V measured at 30 °C for the same device stressed in Fig. 1 at 125 °C.

abruptly increases for stress times beyond 10 s and saturates after a few hours. A trap with a similar time constant was found in earlier work to sharply increase for stress beyond the critical voltage and to have an energy level of ~0.56 eV [11]. In addition, a broad spectrum of traps with longer detrapping time constants (detrapping time of 1-100 s) emerges with a similar stress time dependency (Fig. 2). The time dependence for the growth of these trapping peaks matches well the time evolution of current collapse in Fig. 5 suggesting that these are different manifestations of the same physics which is prominent trap generation over a time window of 10-10^4 s.

IV. TEMPERATURE DEPENDENCE

The time evolution of gate and drain current degradation exhibits different behavior at different stress temperatures. As shown in Fig. 3, gate current degradation depends little on temperature. At all stress temperatures between 75 and 150 °C, the gate current starts to increase even after 10 ms of stressing. Interestingly, the threshold voltage exhibits a similar behavior to I_{Goff}. As shown in Fig. 4, in an initial stage (t_{stress}<10 s), the

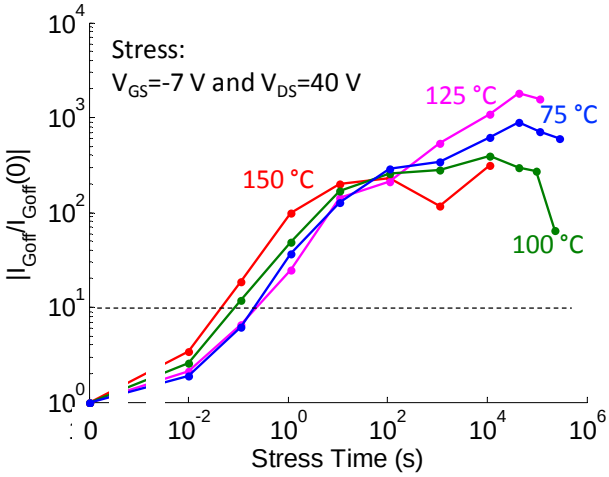


Fig. 3. Evolution of gate current degradation (normalized to initial value) at various stress temperatures. Four different devices were used. The stress condition was V_{GS}=-7 V and V_{DS}=40 V. Device characterization performed at 30 °C.

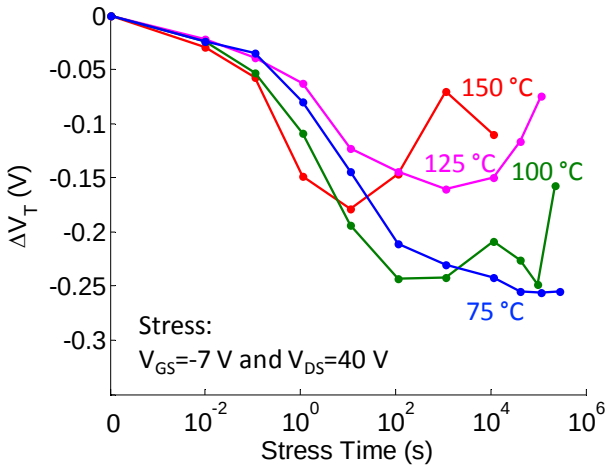


Fig. 4. Evolution of threshold voltage (relative to its initial value) in the experiment of Fig. 3. Device characterization performed at 30 °C.

change in V_T is largely unaffected by temperature. For longer times, ΔV_T tends to saturate. This similarity in the behavior of I_{Goff} and V_T is reasonable because both are mainly affected by degradation in the intrinsic gate region.

In contrast, drain current degradation, both permanent and trapping related, show clear stress temperature dependence (Fig. 5Fig. 6). Degradation in I_{Dlin} current collapse and uncollapsed I_{Dmax} (and I_{Dlin}) start earlier at higher temperatures and the final value also increases as the stress temperature increases. This later observation is consistent with earlier studies [12]. The fact that permanent I_{Dlin} evolves in a similar way as permanent I_{Dmax} (Fig. 6) suggests that the changes that we are observing are taking place in the extrinsic portion of the device, more concretely the drain since that is where the high field region appears during stress.

Our experiments reveal that there is an incubation time for device degradation and that the incubation time is different and evolves in a different way with temperature for the different figures of merit. We have extracted the incubation time for these modes of degradation with the following definitions. For I_{Goff} degradation, the incubation time is defined as the time for I_{Goff} to increase by a factor of 10. For permanent I_{Dmax}

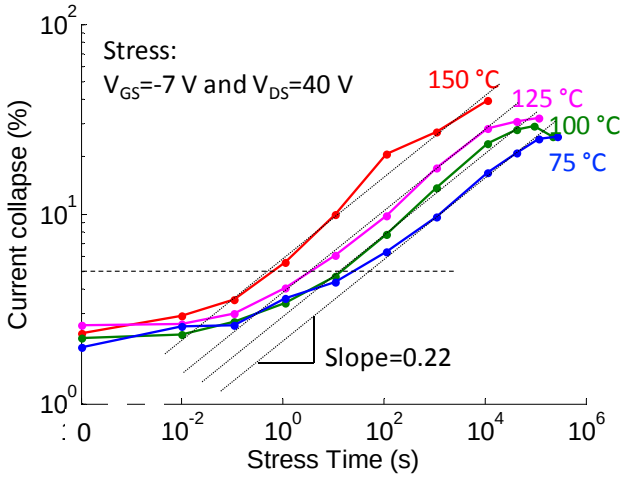


Fig. 5. Evolution of I_{Dlin} current collapse in the experiment of Fig. 3. Current collapse is defined as the relative change in I_{Dmax} after applying 1s V_{DS}=0 pulse with V_{GS}=-10 V at 30 °C.

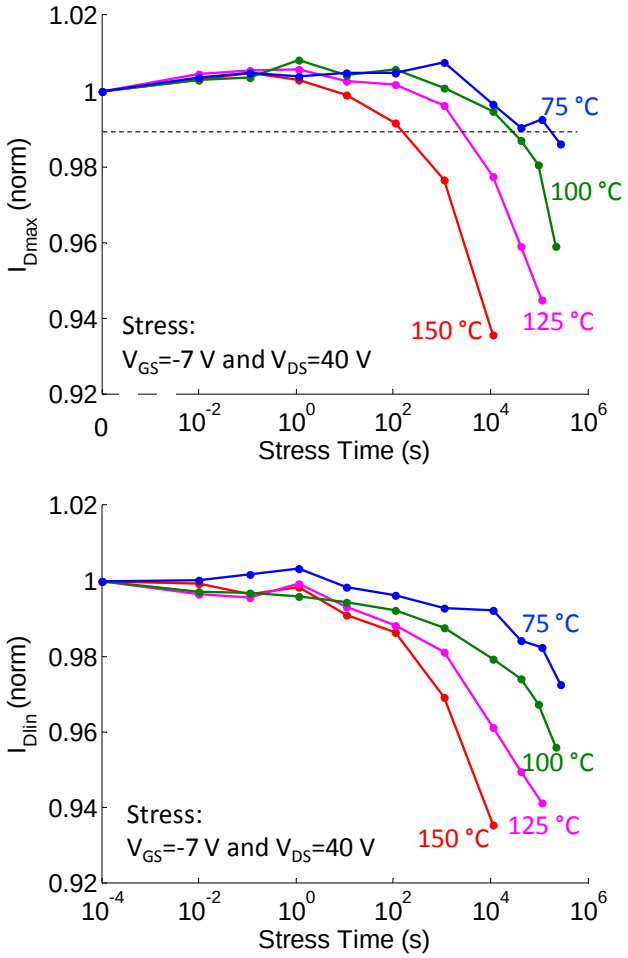


Fig. 6. Evolution of permanent I_{Dmax} and I_{Dlin} degradation in the experiment of Fig. 3. The values are normalized to their unstressed levels. Device characterization performed at 30 °C.

degradation, it is defined when the uncollapsed I_{Dmax} decreases by 1%. For trapping-related (current collapse) degradation, we monitor the time for current collapse to reach 5%.

As shown in Fig. 7, the incubation time for I_{Goff} is almost unaffected by temperature (E_a~0.17 eV). This is consistent with the previous observation in [8]. In contrast, the incubation times for drain current degradation are thermally activated but with different activation energies (1.12 and 0.59 eV, respectively), suggesting that different physical processes are involved. The activation energy for permanent I_{Dmax} degradation is very close to that of I_{Dlin} and that extracted from long-term life test data in similar devices (E_a=1.05 eV) [13]. Also, a similar activation energy was reported for degradation in the DC value of drain current (E_a=1.13 eV) under the stress condition of V_{DS}=40 V and I_D=200 mA/mm in different devices by a separate team [3].

V. Discussion

It is interesting to compare the electrical results obtained in this work with the structural analysis performed in GaN HEMTs after high voltage stress as performed in [7]. In that earlier study, we investigated the time evolution of structural defect formation under high voltage electrical stress with

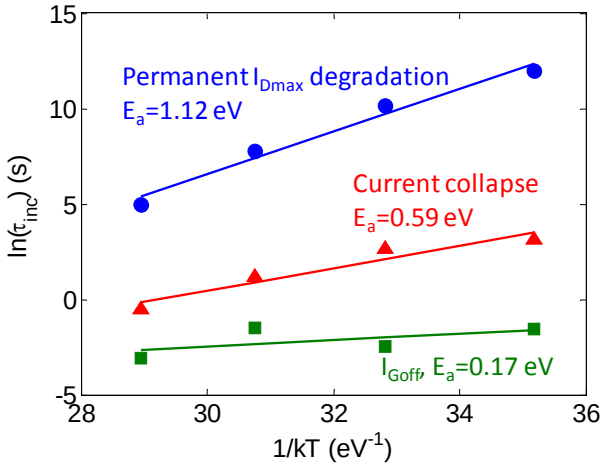


Fig. 7. Arrhenius plot of incubation time for I_{Goff}, permanent I_{Dmax} degradation and current collapse degradation as a function of stress temperature. The incubation time is defined as dashed lines in Fig. 3-Fig. 6.

V_{DS}=0 in GaN HEMTs as observed by planar techniques after the passivation and metals had been removed from stressed devices. In [7], we observed relatively fast formation (less than 10 s) of a continuous groove on the GaN cap running along the edges of the gate. On a longer time scale, we also observed the formation of prominent pits at the source and drain edges of the gate. The average pit cross-sectional area increased as $t^{0.25}$. We found a close correlation between the size and density of the pits and permanent current degradation as a function of stress time. Current collapse degradation also correlated well except for a similar saturating pattern as observed here.

A comparison between the study in [7] with the present work, allows us to postulate hypotheses for the evolution of degradation observed in the present work. The early phase of degradation that is characterized by temperature independent gate leakage current degradation and a corresponding shift in V_T could be associated with the formation of the groove. The groove has been observed to be formed even for stress voltages below V_{crit} [7, 14]. Also, degradation in I_{Goff} has been reported for stress voltage below V_{crit} if the device is stressed for long enough time [8].

The later phase of stress in which both current collapse and permanent drain degradation increase seems associated with the formation and growth of the pits. Interestingly, the time evolution for the increase in current collapse in Fig. 5 evolves as $t^{0.22}$ (slope in Fig. 5) regardless of temperature. This is very close to the observations made in [7] for the time evolution of the growth of the pits.

This temperature-independence degradation rate seems to agree with [7] where pit growth rate exhibited a very weak temperature dependence (E_a=0.11 eV). In addition, it was found that it takes about 10-100 s for the pit formation to be initiated. This appears to correspond to the incubation time for current collapse degradation. Developing a detailed understanding of the physics behind these findings will require structural degradation studies similar to those performed in [14-15].

VI. Conclusion

In summary, we have investigated the time evolution of electrical degradation of GaN HEMTs under high-voltage stress beyond the critical voltage in the OFF state. We found that the gate current starts to degrade first, followed by current collapse and eventually permanent degradation in I_{Dmax}. We also found that while the time evolution of gate current degradation is largely unaffected by temperature, drain current degradation is thermally accelerated. Our findings will be instrumental in developing predictive models for operational lifetime of GaN HEMTs

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