Scalability of Sub-100 nm InAs HEMTs on InP Substrate for Future Logic Applications

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***Abstract*—We have experimentally studied the scaling behavior of sub-100-nm InAs high-electron mobility transistors (HEMTs) on InP substrate from the logic operation point of view. These devices have been designed for scalability and combine a thin InAlAs barrier and a thin channel containing a pure InAs subchannel. InAs HEMTs with gate length down to 40 nm exhibit excellent logic figures of merit, such as $I_{\rm ON}/I_{\rm OFF} = 9 \times 10^4$, drain-induced-barrier lowering $= 80$ mV/V, $S = 70$ mV/dec, and an estimated logic gate delay of 0.6 ps at $V_{DS} = 0.5$ V. In addition, we have obtained excellent high-frequency operation with $L_g = 40$ nm, such as $f_T = 491$ GHz and $f_{\max} = 402$ GHz at $V_{DS} = 0.5$ V. In spite of the narrow bandgap of InAs subchannel, under the studied conditions, our devices are shown not to suffer from excessive band-to-band tunneling. When benchmarked against state-of-the-art Si devices, 40-nm InAs HEMTs exhibit $I_{\rm ON} = 0.6$ A/μm at $I_{\rm Leak} = 200$ nA/μm. This is about two times higher $I_{\rm ON}$ than state-of-the-art high-performance 65-nm nMOSFET with comparable physical gate length and $I_{\rm Leak}$.**

***Index Terms*—Drain-induced barrier lowering (DIBL), gate delay, high-electron mobility transistor (HEMT), InAs, $I_{\rm ON}/I_{\rm OFF}$, logic, scaling, subthreshold swing.**

I. Introduction

III–V compound semiconductors have recently emerged as a promising choice for channel material of future post-Si CMOS logic transistors. This is due to their outstanding electron transport properties, their relative maturity, and demonstrated reliability when compared with other candidates, such as carbon nanotube transistors and semiconductor nanowires [1]–[5]. For future III–V based field-effect transistors (FETs) to enter the CMOS roadmap, they will have to have dimensions compatible with the 22 nm CMOS node or beyond. As such, scalability is of critical importance.

Future III–V FETs are likely to integrate a high-k dielectric in the gate stack and a self-aligned architecture [6]–[9]. There are several challenges to overcome before this can be accomplished [10]–[12]. In the meantime, the scalability of III–V FETs can be studied using high-electron mobility transistors (HEMTs). These are useful devices in their own right for millimeter-wave applications, but they can also constitute an excellent model system to study issues of critical importance of future III–V MOSFETs, such as intrinsic carrier transport, quantum capacitance, band-to-band tunneling (BTBT), impact ionization, and the impact of parasitic resistances onto device performance.

Recent research on InAlAs/InGaAs HEMTs has demonstrated that these devices exhibit excellent logic characteristics down to about 60 nm [13]. This has been accomplished by thinning down the InAlAs barrier $(t_{\rm ins})$ to the 3–4 nm range. Further lateral scaling is going to require scaling of the channel thickness $(t_{\rm ch})$ as well. However, as $t_{\rm ch}$ scales down, carrier transport in the channel deteriorates, mainly as a consequence of the increased carrier scattering mechanisms [14], [15]. In this paper, we have explored a solution to this problem through the introduction of a pure thin layer of InAs in the channel [16], [17]. InAs is a very attractive material with an electron mobility as high as 20 000 cm^2/V $\cdot$ s at room temperature. The introduction of InAs is expected to mitigate the deleterious effects of channel thickness scaling. We show that it is possible to fabricate devices with a channel thickness of 10 nm while keeping excellent carrier transport in the channel. In this way, we demonstrate HEMT scalability down to the 40-nm gate length regime.

This paper represents an augmented and updated version of an earlier conference presentation [18]. It describes the detailed fabrication process of the InAs HEMTs with a 10-nm channel thickness on InP substrate. In addition, we present the logic characteristics of the fabricated InAs HEMTs as a function of gate length (L_g) and barrier thickness $(t_{\rm ins})$, and we compare them to our prior work with a thicker channel $(t_{\rm ch} = 13$ nm) [13]. Finally, we benchmark our fabricated InAs HEMTs against state-of-the-art Si CMOS. A significant finding in this work is that in spite of the narrow bandgap of the InAs subchannel, these devices do not suffer from excessive BTBT.

II. Device Technology

Fig. 1 shows the epitaxial layer structure utilized in this work. This is grown by molecular beam epitaxy (MBE) on a semi-insulating InP substrate. In essence, this is an InAlAs/InGaAs HEMT structure with a composite channel that includes a strained InAs subchannel. Except for the channel structure, the device layer design is similar to our previous work [13]. The layers consist of, from bottom to top, a 500-nm $In_{0.52}Al_{0.48}As$ buffer, a 10-nm composite channel (described in more detail next), a 3-nm $In_{0.52}Al_{0.48}As$ spacer, a Si δ-doping

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n+ Cap	$In_{0.65}Ga_{0.35}As$	10 nm
	$In_{0.53}Ga_{0.47}As$	25 nm
	$In_{0.52}Al_{0.48}As$	15 nm
Stopper	InP	6 nm
Barrier	$In_{0.52}Al_{0.48}As$	8 nm
δ-doping	Si	-
Spacer	$In_{0.52}Al_{0.48}As$	3 nm
Channel	$In_{0.53}Ga_{0.47}As$	2 nm
	InAs	**5 nm**
	$In_{0.53}Ga_{0.47}As$	3 nm
Buffer	$In_{0.52}Al_{0.48}As$	500 nm
3 Inch S. I. InP Substrate		

Fig. 1. MBE-grown epitaxial layer structure of InAs HEMTs used in this work.

$(5 \times 10^{12}/\text{cm}^2)$, an 8-nm $In_{0.52}Al_{0.48}As$ barrier, a 6-nm InP etch-stopper, a 15-nm n^+ doped $In_{0.52}Al_{0.48}As$ subcap, a 25-nm n^+ doped $In_{0.53}Ga_{0.47}As$ subcap, and a 10-nm n^+ doped $In_{0.65}Ga_{0.35}As$ subcap. The channel consists of a trilayer of $In_{0.53}Ga_{0.47}As$, InAs, and $In_{0.53}Ga_{0.47}As$ of thicknesses, from bottom to top, 3, 5, and 2 nm. Altogether, this is about 30% thinner than our previous $In_{0.7}Ga_{0.3}As$ HEMT design [13].

In a Hall epi wafer that has the same structure as the device wafer but otherwise uses a simple 10-nm $In_{0.53}Ga_{0.47}As$ cap with a Si doping density of 1×10^{18} cm^{-3}, the Hall mobility $(\mu_{n,\text{Hall}})$ and 2-D electron gas sheet carrier concentration (n_s) were measured to be around 13 200 $\text{cm}^2/\text{V} \cdot \text{s}$ and $2.9 \times 10^{12}/\text{cm}^2$ at room temperature. The Hall mobility is about 30% higher than in our earlier $In_{0.7}Ga_{0.3}As$ heterostructure [13], [19].

Device fabrication is very similar to our previous work [13], [19]. It began with mesa isolation using H_3PO_4-based wet etchant. This was followed by Ni/Ge/Au (10/45/150 nm) source and drain ohmic contacts with a 2-μm spacing and alloying at 320 °C for 30 s in N_2 ambient. E-beam lithography using a Reica-150 equipment was utilized to define T-shaped gates with various dimensions. We used a trilayer resist stack of ZEP-520A/PMGI/ZEP-520A (from bottom to top, 200/600/100 nm). To study the scaling behavior of this technology, different values of the gate length were defined by adjusting the e-beam dose and changing the layout dimension accordingly to keep the source–gate and gate–drain distances constant.

Gate recessing was performance in three different stages, as in our earlier work [13]. First, an isotropic etching of the InGaAs/InAlAs multilayer cap was performed in the mixture of citric acid and H_2O_2 (20 : 1). This was followed by anisotropic etching of InP layer using low-damaged Ar-based plasma. Finally, time-controlled wet etching of the InAlAs barrier using diluted citric acid solution was performed to further thin down the insulator thickness (t_{ins}). We calibrated the depth of the remaining InAlAs barrier through scanning transmission electron microscope (STEM) inspection and obtained a t_{ins} of about 4 nm, as shown in Fig. 2(a) which corresponds to an $L_g =$ 40 nm device. In addition, we made devices with thicker t_{ins} devices by omitting the third recess step. An insulator thickness of 10 nm was measured by STEM inspection, as shown in Fig. 2(b), which corresponds to an $L_g = 45$ nm device. This is slightly different from the MBE-grown nominal barrier thickness of 11 nm, probably as a result of the finite etching selectivity of InP against InAlAs during Ar-based plasma [20]. Finally, device fabrication was completed by the evaporation and lift-off of Ti/Pt/Au (20/20/300 nm) Schottky gate metal stack.

Devices with various gate lengths were fabricated, from 340 nm down to 40 nm. Fig. 2(c) shows a STEM image of the cross section of a $L_g = 45$ nm T-gate device. Notice that the evaporated gate metal partially overlaps with the InP etch-stopper at both edges of the InAlAs recessed region. As a result, the metallurgical L_g seems to be larger than 45 nm. However, we define L_g as the length of the recessed region in the InAlAs barrier as in the two-step recess process [21]. Fig. 2(c) also shows that the side-recess-spacing length (L_{side}) in these devices was set to be around 200 nm to ensure optimum logic operation. This was done by adjusting the recess etching time of the InGaAs/InAlAs capping layers [22]. The source and drain spacing (L_{SD}) was 2 μm in these devices. Future III–V HFETs will require a scaling of L_{SD} with L_g since a reduction in the device pitch is the main driving force for logic technology.

III. Results

Fig. 3 shows typical output characteristics of InAs HEMTs with (a) $t_{\text{ins}} = 10$ nm and (b) $t_{\text{ins}} = 4$ nm for various gate lengths. As in our previous work on $In_{0.7}Ga_{0.3}As$ HEMTs [13], we find that thinner insulator devices exhibit better current driving capability and a more positive V_T. They also show better scalability. Looking at output conductance (g_o) for both types of 40 nm InAs HEMTs, we see that the devices with $t_{\text{ins}} = 4$ nm show slightly better output conductance than those with $t_{\text{ins}} = 10$ nm, which is a result of the reduction in t_{ins}.

Improved short-channel effects (SCEs) that arise from a thinner insulator are evident in the subthreshold characteristics. Fig. 4 shows subthreshold characteristics of both types of 40 nm devices at $V_{DS} = 50$ mV and 0.5 V, together with gate leakage current (I_G). Here, we can clearly see how the 4-nm barrier device exhibits superior subthreshold swing (S) and drain-induced barrier lowering (DIBL, change in V_T with V_{DS}). We also see that V_T shifts positive as the barrier is thinned down.

A tradeoff with scaling the insulator thickness that is evident in Fig. 4 is an increase of gate leakage current in the forward and reverse gate bias condition. A consequence of this is that the minimum subthreshold current is about an order of magnitude higher for the thin barrier device. It is interesting to note that in both types of devices, the minimum subthreshold current is dominated by Schottky gate leakage, not by band-to-band-tunneling (BTBT). This will be a serious concern when a high mobility channel material is utilized with a significantly smaller bandgap than Si and might ultimately limit the scalability of the device [23], [24]. In our device design, BTBT is not a significant concern in spite of the narrow bandgap of the channel. This might be due to electron quantization in the thin InAs

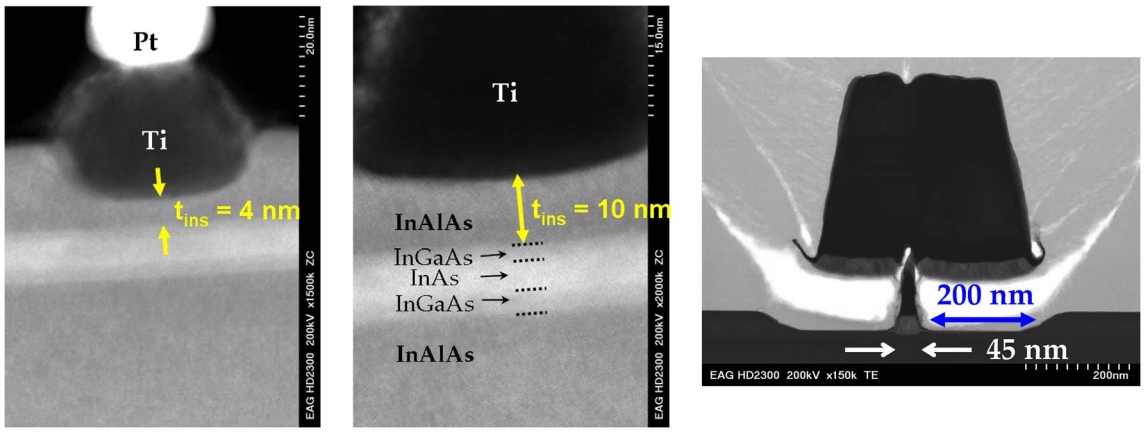

Fig. 2. STEM images of the cross section of the fabricated device. (a) Close up of gate region for an $L_g = 40$ nm and $t_{\rm ins} = 4$ nm device. (b) Close up of gate region for $t_{\rm ins} = 10$ nm device with $L_g = 45$ nm. (c) Gate view of an $L_g = 45$ nm gate length device showing $L_{\rm side} = 200$ nm.

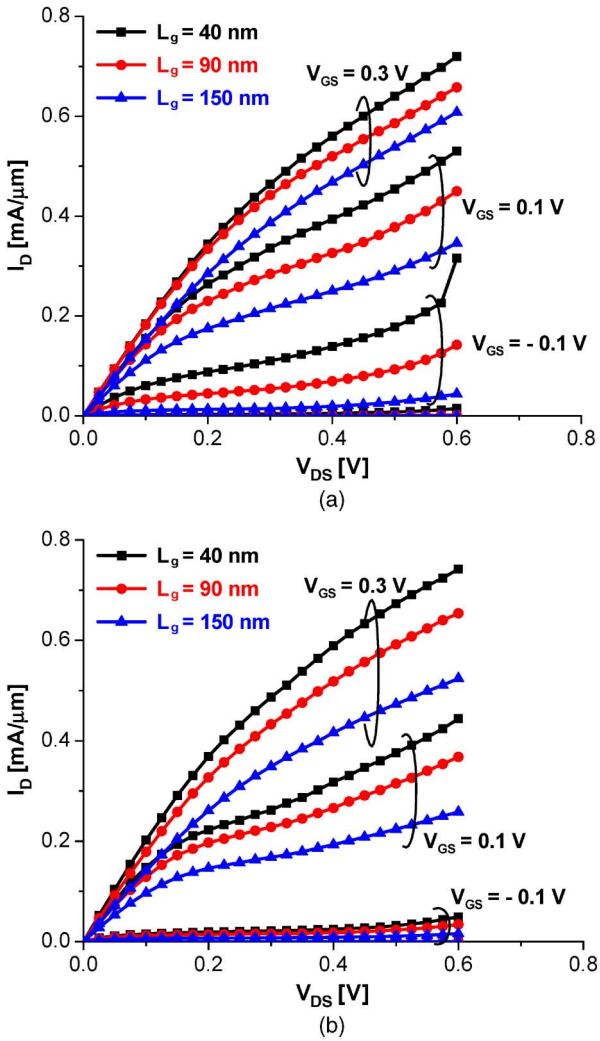

Fig. 3. Output characteristics of InAs HEMTs with (a) $t_{\rm ins} = 10$ nm and (b) $t_{\rm ins} = 4$ nm for various values of L_g.

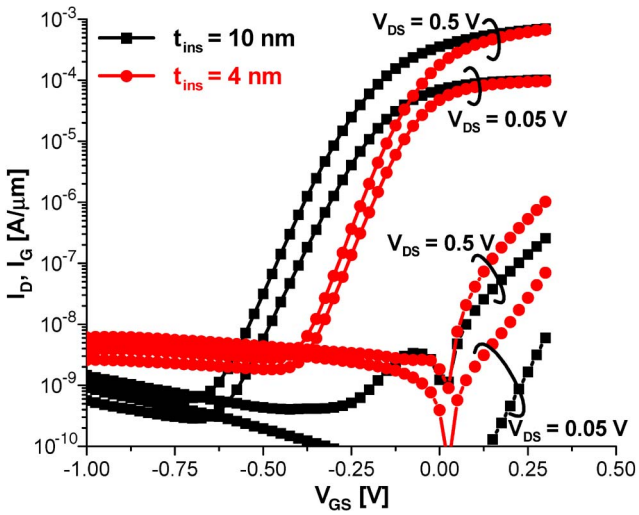

Fig. 4. Subthreshold and gate current characteristics of 40-nm InAs HEMTs with $t_{\rm ins} = 10$ nm (black) and $t_{\rm ins} = 4$ nm (red), at $V_{DS} = 0.05$ V and 0.5 V.

subchannel layer, which is expected to enlarge the effective bandgap (E_g) [25]. However, future device designs with much reduced gate leakage current might show more pronounced BTBT currents.

The improvement in transistor performance with $t_{\rm ins}$ scaling can be seen more clearly in the transconductance (g_m) characteristics. Fig. 5 plots g_m of both types of InAs HEMTs for various values of L_g at $V_{DS} = 0.5$ V. For thicker barrier devices with $t_{\rm ins} = 10$ nm [Fig. 5(a)], as L_g scales down, g_m initially increases, and then, it actually gets worse beyond an L_g of about 60 nm. We can also see a significant negative shift in V_T, as L_g scales down. These are clear indications of severe SCEs. On the contrary, $t_{\rm ins} = 4$ nm devices [Fig. 5(b)] exhibit much less V_T shift as L_g scales down. More importantly, the peak g_m continues to scale gracefully down to $L_g = 40$ nm. In fact, the 40-nm InAs HEMTs with $t_{\rm ins} = 4$ nm display an excellent value of $g_{m,\max} > 2$ mS/μm at $V_{DS} = 0.5$ V.

Fig. 6 summarizes $g_{m,\max}$ as a function of L_g for both types of InAs HEMTs, as well as our previous $In_{0.7}Ga_{0.3}As$ HEMTs with $t_{\rm ins} = 10$ and $t_{\rm ch} = 13$ nm [4]. This figure highlights the combined benefits of thin insulator, thin channel, and higher mobility channel. When compared with $In_{0.7}Ga_{0.3}As$ HEMTs, the benefits of InAs HEMTs are now apparent. For a similar value of the barrier thickness $(t_{\rm ins} = 10$ nm), the InAs HEMTs exhibit much higher values of $g_{m,\max}$ at long

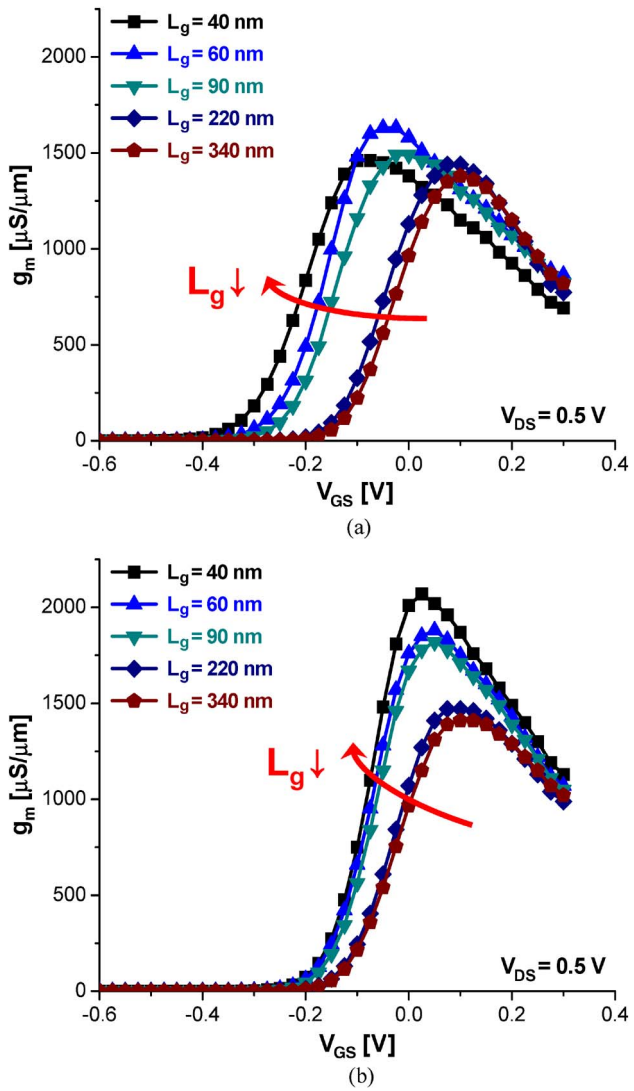

Fig. 5. Transconductance characteristics of 40-nm InAs HEMTs with (a) $t_{\rm ins} = 10$ nm and (b) $t_{\rm ins} = 4$ nm, for various values of L_g, at $V_{DS} = 0.5$ V.

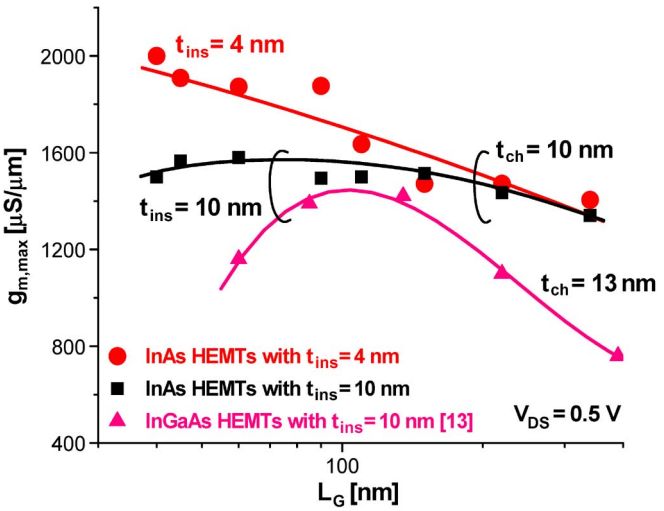

Fig. 6. Maximum transconductance $(g_{m,\max})$ as a function of L_g for InAs HEMTs with $t_{\rm ins} = 10$ nm (black) and $t_{\rm ins} = 4$ nm (red). Our previous results on $In_{0.7}Ga_{0.3}As$ HEMTs with $t_{\rm ins} = 10$ nm and $t_{\rm ch} = 13$ nm are also included [13]. For all data, V_{DS} is 0.5 V.

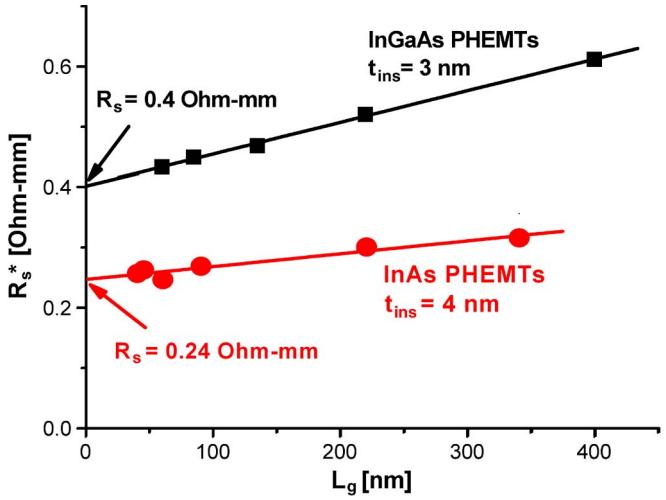

Fig. 7. Measured R_S^* as extracted by the gate current injection technique as a function of L_g for InAs HEMTs with $t_{\rm ins} = 4$ nm and $In_{0.7}Ga_{0.3}As$ HEMTs with $t_{\rm ins} = 3$ nm. The extracted values of R_s for both devices are shown.

L_g than $In_{0.7}Ga_{0.3}As$ HEMTs. This is mainly attributed to the improved transport properties of the InAs subchannel. More significantly, the scaling characteristics of the InAs devices are superior to those of the $In_{0.7}Ga_{0.3}As$ devices. In $In_{0.7}Ga_{0.3}As$ channel HEMTs, g_m peaks at around $L_g = 120$ nm, while in InAs channel HEMTs, g_m peaks at around $L_g = 60$ nm. This is the consequence of the thinner channel. When these improvements (higher g_m and better g_m scalability) are combined with a thinner barrier of 4 nm, InAs HEMTs show very high values of g_m that continues to scale down to the $L_g = 40$ nm regime.

As mentioned in Section II, to avoid performance degradation, it is very important to examine whether the source resistance (R_S) degrades after the three-step recess process. In fact, in an earlier work [13], we found a significant tradeoff with the reduction of $t_{\rm ins}$ in the form of a decrease in g_m and $I_{\rm ON}$. This originated mostly from an increase in R_S and R_D after the three-step recess process. Fig. 7 shows measured R_S^* as a function of L_g for our InAs HEMTs with $t_{\rm ins} = 4$ nm in this work and our previous $In_{0.7}Ga_{0.3}As$ HEMTs with a similar $t_{\rm ins} = 3$ nm, obtained from the gate current injection technique [26]. Since R_S^* is the sum of the actual source resistance (R_S) plus half of the channel resistance $(R_{\rm ch})$, R_S can be extracted by linear extrapolation of the measured R_S^* to $L_g = 0$. We find that in our InAs HEMT, R_S does not degrade, as opposed to in our previous work. This is one more reason why InAs HEMTs with $t_{\rm ins} = 4$ nm outperform significantly our earlier devices. Now, the reason for the excellent value of R_S in InAs HEMTs is likely to arise from a more anisotropic etching profile of the InAlAs barrier after the three-step recess process.

Once we know R_S, we can evaluate the intrinsic transconductance $(g_{\rm mi})$ in an effort to understand the intrinsic performance potential of the technology. Following Chou and Antoniadis' approach [27], we have extended the procedure to extract $g_{\rm mi}$, taking into account the effects of output conductance (g_o), R_S, R_D and gate leakage current (I_G) [13]. Fig. 8 shows $g_{\rm mi}$ as a function of L_g for InAs HEMTs with both $t_{\rm ins} = 4$ nm and 10 nm at $V_{DS} = 0.5$ V, together with $In_{0.7}Ga_{0.3}As$

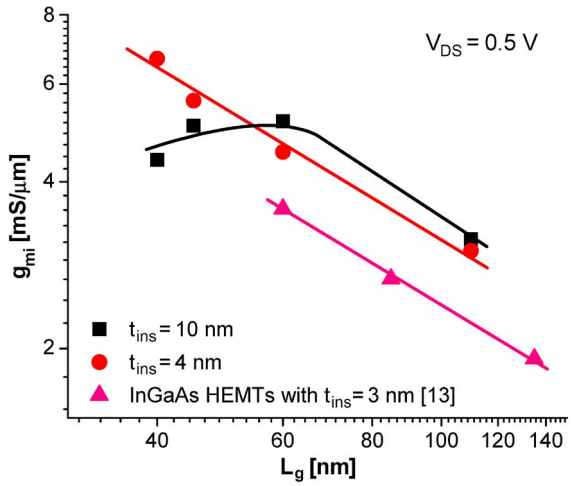

Fig. 8. Extracted intrinsic transconductance ($g_{\rm mi}$) as a function of L_g for InAs HEMTs with $t_{\rm ins} = 4$ nm and 10 nm, and $In_{0.7}Ga_{0.3}As$ HEMTs with $t_{\rm ins} = 3$ nm, at $V_{DS} = 0.5$ V.

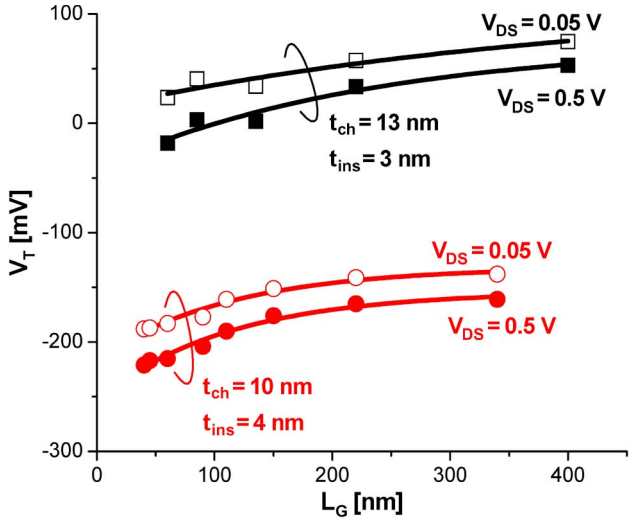

Fig. 9. V_T roll-off behavior of InAs HEMTs with $t_{\rm ins} = 4$ nm and $In_{0.7}Ga_{0.3}As$ HEMTs with $t_{\rm ins} = 3$ nm.

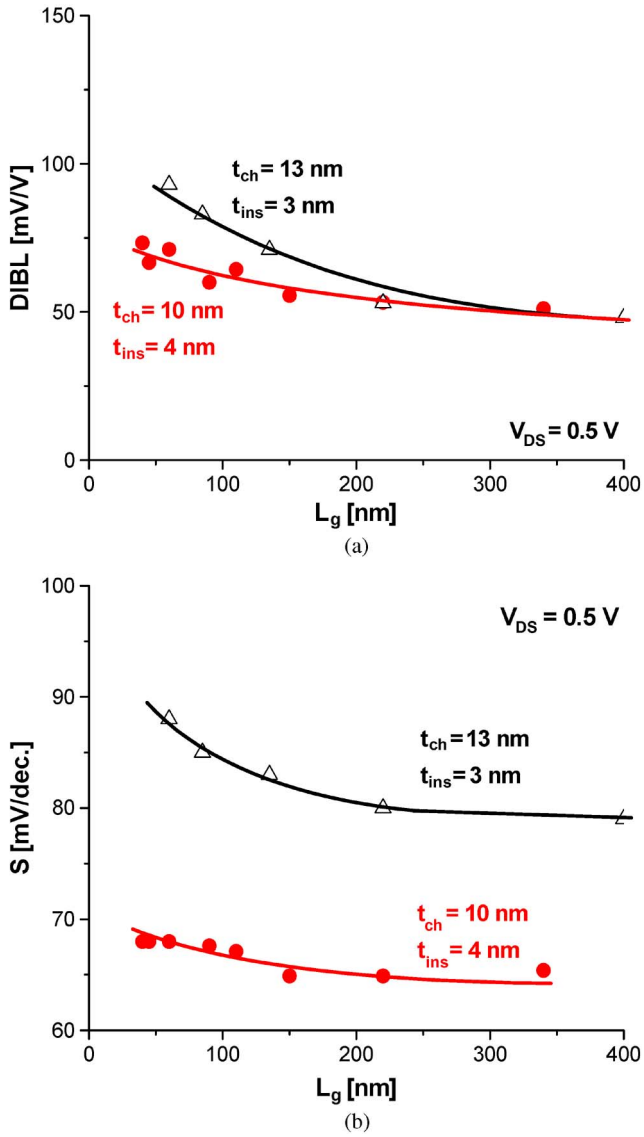

Fig. 10. (a) DIBL and (b) subthreshold swing as a function of L_g, for InAs HEMTs with $t_{\rm ins} = 4$ nm and $t_{\rm ch} = 4$ nm, and $In_{0.7}Ga_{0.3}As$ HEMTs with $t_{\rm ins} = 3$ nm and $t_{\rm ch} = 13$ nm.

HEMTs with $t_{\rm ins} = 3$ nm. For long values of L_g, $g_{\rm mi}$ degrades slightly when thinning down $t_{\rm ins}$. This might be due to an increased probability of carrier scattering with thinned InAlAs barrier surface, which deteriorates carrier transport properties. However, as L_g scales down, the superior scalability of the intrinsic transconductance becomes evident for devices with $t_{\rm ins} = 4$ nm. In comparison with the reference $In_{0.7}Ga_{0.3}As$ devices with $t_{\rm ins} = 3$ nm, InAs HEMTs exhibit far higher values of $g_{\rm mi}$, arising from better carrier transport properties due to the InAs subchannel.

Fig. 9 shows V_T roll-off behavior of InAs HEMTs with $t_{\rm ins} = 4$ nm and $In_{0.7}Ga_{0.3}As$ HEMTs with $t_{\rm ins} = 3$ nm, at $V_{DS} = 0.05$ and 0.5 V, using the V_T definition of $I_D = 1\ \mu{\rm A}/\mu{\rm m}$. Both sets of devices exhibit excellent V_T roll-off behavior down to L_g of sub-100-nm regime due to their thin insulator. Fig. 10 summarizes (a) DIBL and (b) subthreshold swing, as a function of L_g for $t_{\rm ins} = 4$ nm InAs devices, together with those of $t_{\rm ins} = 3$ nm $In_{0.7}Ga_{0.3}As$ devices at $V_{DS} = 0.5$ V [13]. This figure shows how thinning down $t_{\rm ch}$ improves SCEs. In particular, the $t_{\rm ch} = 10$ nm devices with $t_{\rm ins} = 4$ nm show excellent V_T roll-off < 60 mV, DIBL $<$ 80 mV/V, and $S < 70$ mV/dec, down to the $L_g = 40$ nm regime.

Fig. 11 shows $I_{\rm ON}/I_{\rm OFF}$ ratios for the $t_{\rm ch} = 10$ nm devices with $t_{\rm ins} = 4$ nm, together with the $t_{\rm ch} = 13$ nm $In_{0.7}Ga_{0.3}As$ devices with $t_{\rm ins} = 3$ nm, all at $V_{DS} = 0.5$ V. As mentioned earlier, V_T was defined as $I_D = 1\ \mu{\rm A}/\mu{\rm m}$, and then, $I_{\rm ON}$ and $I_{\rm OFF}$ were defined at 2/3 $V_{\rm CC}$ swing above V_T and 1/3 $V_{\rm CC}$ swing below V_T, respectively, as in [1] and [13]. Not only do thin-channel InAs devices exhibit much higher values of $I_{\rm ON}/I_{\rm OFF}$ ratio, but their $I_{\rm ON}/I_{\rm OFF}$ ratios are also maintained as L_g scales down to 40 nm. This stems from the combination of the use of high mobility InAs channel, thinning down the channel and the barrier, and process optimization that prevents R_s degradation. Indeed, 40-nm InAs HEMTs with $t_{\rm ins} = 4$ nm show excellent $I_{\rm ON}/I_{\rm OFF}$ of 9×10^4.

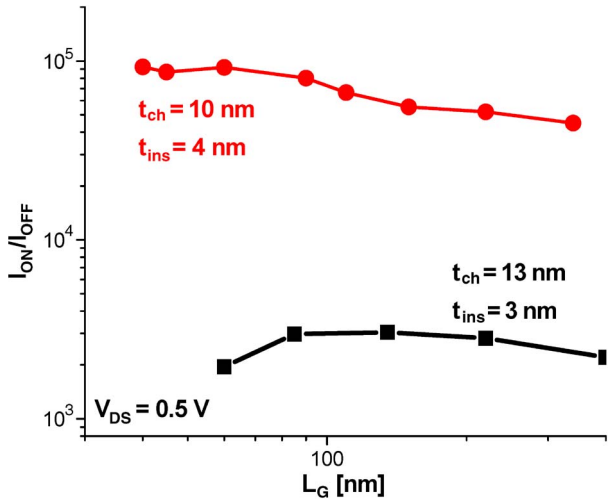

Fig. 11. $I_{\rm ON}/I_{\rm OFF}$ as a function of L_g, for InAs HEMTs with $t_{\rm ins} = 4$ nm and $t_{\rm ch} = 4$ nm, and $In_{0.7}Ga_{0.3}As$ HEMTs with $t_{\rm ins} = 3$ nm and $t_{\rm ch} = 13$ nm.

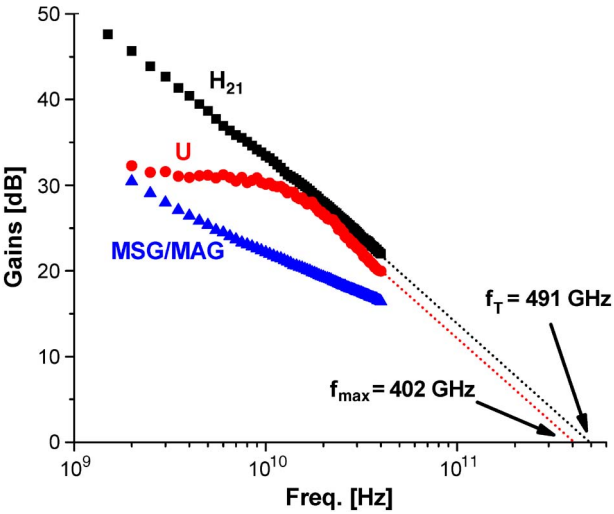

Fig. 12. H_{21}, U, and MSG/MAG of 40-nm InAs HEMTs at $V_{GS} = 0$ V and $V_{DS} = 0.5$ V.

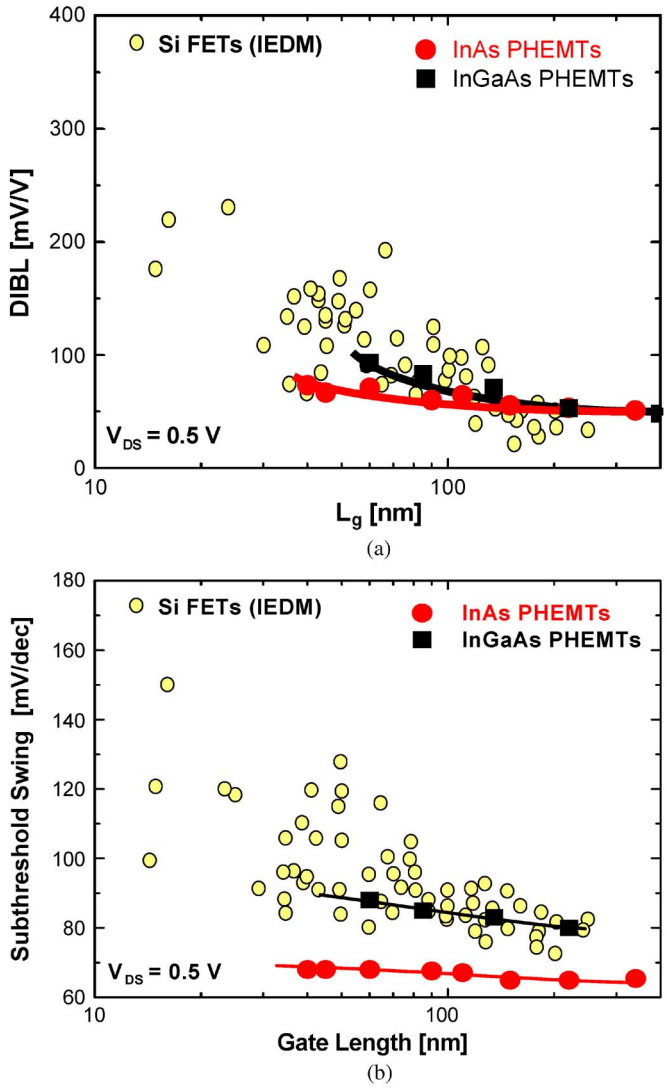

Fig. 13. (a) DIBL and (b) subthreshold swing of InAs HEMTs with $t_{\rm ins} = 4$ nm and $t_{\rm ch} = 4$ nm, and $In_{0.7}Ga_{0.3}As$ HEMTs with $t_{\rm ins} = 3$ nm and $t_{\rm ch} = 13$ nm against L_g, together with that of advanced Si MOSFETs.

Microwave performance of the fabricated InAs HEMTs was characterized from 0.5 to 40 GHz using an HP 8510C network analyzer. We used an on-wafer open/short deembedding method to subtract both pad capacitance and inductance components. Fig. 12 shows the H_{21}, Maximum-Stable-Gain/Maximu-Available-Gain (MSG/MAG), and U of 40 nm InAs HEMTs with $t_{\rm ins} = 4$ nm, at $V_{\rm GS} = 0.2$ V and $V_{DS} = 0.5$ V. Notice that the 40-nm InAs devices exhibit excellent f_T of 491 GHz and $f_{\rm max}$ of 402 GHz, even at $V_{DS} = 0.5$ V. This high f_T arises partly from the excellent transport properties associated with the incorporation of the InAs subchannel.

IV. Benchmark With Si Devices

We have benchmarked our InAs HEMTs against state-of-the-art Si CMOS. Fig. 13(a) and (b), respectively, shows a comparison of DIBL and S. The $t_{\rm ch} = 10$ nm InAs HEMTs with $t_{\rm ins} = 4$ nm exhibit as good a DIBL and even superior subthreshold swing as comparable Si devices.

Speed performance can be evaluated through an estimation of the logic gate delay (CV/I). We have done this following the procedure outlined in [1] and refined in [13]. Fig. 14 shows the CV/I of the $t_{\rm ch} = 10$ nm InAs HEMTs having $t_{\rm ins} = 4$ nm at $V_{DD} = 0.5$ V as well as the $t_{\rm ch} = 13$ nm $In_{0.7}Ga_{0.3}As$ devices having $t_{\rm ins} = 3$ nm [13], as a function of L_g. Here, we also include those of Si CMOS, which are typically obtained at $V_{DD} = 1.1$ to 1.3 V. Our InAs HEMTs exhibit significantly better CV/I than Si-CMOS in spite of the lower voltage of operation. Besides, CV/I scales gracefully down to the $L_g = 40$ nm regime.

The advantage in CV/I that we observed with respect to Si CMOS is not as large as one would expect from the ratio of mobilities in these two materials. Indeed, what is relevant in CV/I is the carrier velocity and the intrinsic capacitance. Recent measurements have shown that the electron velocity in InAs HEMTs is about a factor of two times higher than in Si, even at the lower voltages that we use here [28]. This is consistent with the data that are shown in Fig. 14.

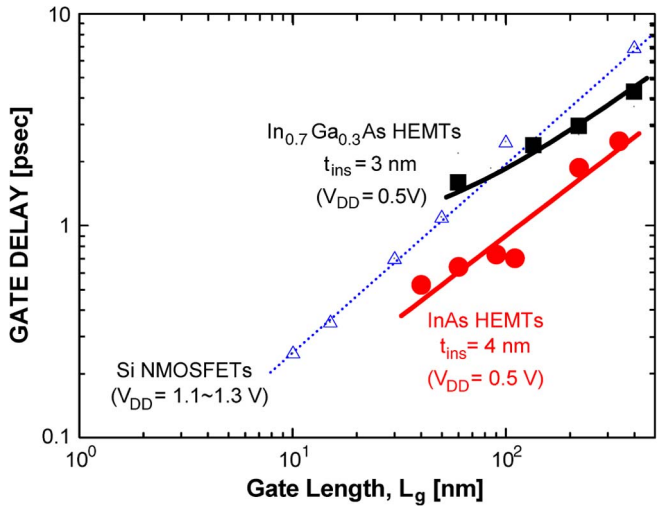

Fig. 14. Gate delay (CV/I) of InAs HEMTs with $t_{\rm ins} = 4$ nm and $t_{\rm ch} = 4$ nm, and $In_{0.7}Ga_{0.3}As$ HEMTs with $t_{\rm ins} = 3$ nm and $t_{\rm ch} = 13$ nm at $V_{DD} = 0.5$ V, together with that of advanced Si MOSFETs at $V_{DD} = 1.1$ V to 1.3 V.

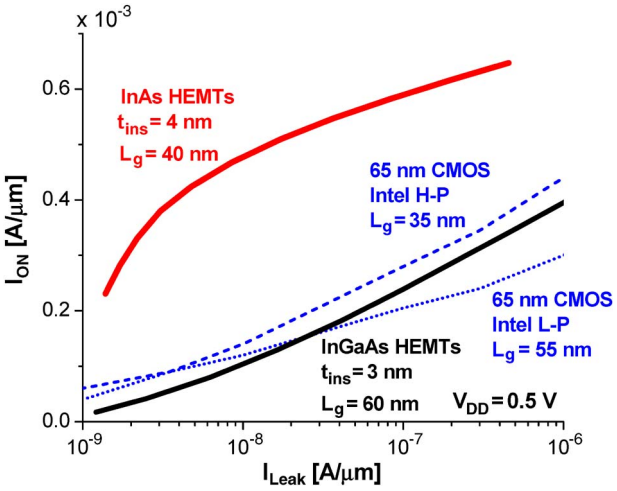

Fig. 15. $I_{\rm ON}$ versus $I_{\rm Leak}$ of 40-nm InAs HEMTs with $t_{\rm ins} = 4$ nm and 60-nm $In_{0.7}Ga_{0.3}As$ HEMTs with $t_{\rm ins} = 3$ nm, together with both high-performance and low-power 65-nm CMOS, at $V_{DD} = 0.5$ V.

Another important device figure of merit for high-performance and low-power applications is $I_{\rm ON}$ versus $I_{\rm OFF}$ characteristics. As mentioned in our previous work [13], a rigorous comparison must include the impact of gate leakage current. We have accounted for this by introducing $I_{\rm Leak}$, which averages each contribution of the device leakage current during the ON and OFF states. Fig. 15 plots $I_{\rm ON}$ as a function of $I_{\rm Leak}$ for a representative 40 nm InAs HEMT with $t_{\rm ins} = 4$ nm, as well as for state-of-the-art 65-nm high-performance [29] and low-power [30] CMOS devices, all at $V_{DD} = 0.5$ V. Included in this graph are data for one of our earlier 60-nm $In_{0.7}Ga_{0.3}As$ HEMTs [13]. It is remarkable that for the same average leakage current of 200 nA/μm, the 40-nm InAs HEMT exhibits a drive current $(I_{\rm ON})$ of around 0.6 A/μm, which is about two times higher than that of high-performance 65-nm CMOS.

V. Conclusion

In summary, in an effort to identify the scaling potential of III–V FETs for future high-speed and low-power logic application, we have developed InAs HEMTs with a thin channel and a thin barrier. We have found that 40-nm InAs HEMTs with $t_{\rm ch} = 10$ nm and $t_{\rm ins} = 4$ nm exhibit excellent logic figures of merit, such as DIBL = 80 mV/V, subthreshold swing of 70 mV/dec, $I_{\rm ON}/I_{\rm OFF} = 9 \times 10^4$, and an estimated logic gate delay (CV/I) = 0.6 ps, all at $V_{DD} = 0.5$ V. These encouraging results stem from the combination of the outstanding transport properties of InAs with the use of a thin insulator and a thin channel. In spite of the short gate length and the narrow bandgap of InAs, we obtained $I_{\rm ON}/I_{\rm OFF}$ ratios close to 10^5 without evidence of BTBT leakage current. We have also found that 40-nm InAs HEMTs exhibit about two times higher $I_{\rm ON} = 0.6$ A/μm than state-of-the-art high-performance 65-nm CMOS at the same $V_{DS} = 0.5$ V. InAs is, indeed, a channel material with great potential for beyond Si CMOS logic applications.

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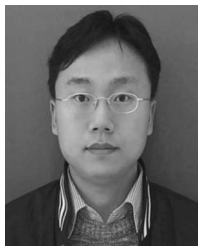

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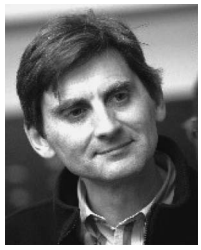

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