Fabrication and Characterization of Through-Substrate Interconnects

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***Abstract*—We developed a through-substrate copper-damascene interconnect technology in silicon with minimal impedance. Via impedance was extracted using S parameter measurements at 50 GHz that were matched to simple circuit models. The extracted impedance shows resistances $\leq 1\ \Omega$, record-low inductance for aspect ratios > 4, and sidewall capacitance that approaches the theoretical value. For an aspect ratio of 10 (10 μm in diameter and 100 μm high), the through-substrate via has an average inductance of 36 pH at 10 GHz, resistance of 0.6 Ω at 1 GHz, and sidewall capacitance of 0.3 pF.**

***Index Terms*—Ground inductance, Si RF technology, substrate crosstalk, substrate via, through-substrate via, through-wafer interconnect, through-wafer via, via inductance.**

I. Introduction

THROUGH-SUBSTRATE interconnects of high-aspect ratio and with low parasitic impedance can find many applications in various semiconductor fields. Specifically, through-wafer interconnects can alleviate interconnect scaling issues in digital circuits, power and ground inductance in silicon radio frequency integrated circuits (RFICs), substrate noise in mixed-signal circuits, and packaging size and cost in microelectromechanical systems (MEMS) and system-in-package (SiP) applications.

Integration and scaling have been the fundamental goals of the semiconductor industry to reduce cost and boost performance. As devices have scaled according to Moore's law, interconnects have lagged. While circuit performance improves as devices scale, interconnect scaling results in longer latency and higher power consumption. Interconnects have quickly become the bottleneck in circuit performance, and managing the need for ever-higher transmission speeds with further scaling is the primary concern for interconnects. Currently, interconnects are laid out on the surface of the chip in an increasing number of metal levels (12 layers at present [1]) and just barely meet performance needs. In addition, continuing integration of circuit functionality onto one chip has been stimulated by the wireless industry for better portability and lower power consumption. This has increased the complexity of not only circuit design but also the demands on interconnects. As metal line widths shrink and line lengths increase, parasitic resistance, capacitance, and inductance degrade circuit performance by increasing delays, loading, and power consumption [2]. Particularly, interconnect inductance contributes to power and ground bounce. Through-substrate vias can help alleviate these problems by reducing line length and minimizing parasitic impedance, especially inductance.

Consumer RF systems have traditionally been fabricated using III–V materials that use through-substrate vias to reduce ground inductance. Silicon has rapidly been supplanting III–Vs because of its lower manufacturing costs and its integration capabilities [3]. Improving the high-frequency performance of silicon by reducing ground inductance with through-substrate vias will project silicon technology into high-end RF and millimeter-wave applications. Furthermore, silicon-based systems allow for integration with digital blocks for system-on-chip (SoC). However, this introduces digital noise into the substrate, which interferes with the operation of RF/analog circuits. This can be mitigated using through-substrate vias wired into a Faraday cage that can suppress crosstalk between blocks [4].

Separately, MEMS packages typically exceed the cost of the device and impose severe design constraints [5]. Introducing low-impedance through-substrate vias as a backside interconnect would reduce packaging size and cost [5]. Through-substrate vias could also provide an interlevel interconnect for MEMS constructed from several bonded wafers.

Through-substrate interconnects also reduce parasitics in packaging, specifically SiP designs [1], by decreasing line length and increasing packing density. This includes multilayer silicon die and chip stacks without parasitic wire bonds and ultimately extends to wafer-level packaging [1], [2], [6], [7]. These examples of SiP can offer the integration of passives, memory, MEMS, RF subsystems, and digital blocks of great interest for wireless applications [1].

To address these applications (Fig. 1), we have developed a through-substrate interconnect technology in silicon using a copper damascene process that allows for ground, power, and signals to be distributed from the backside using high-aspect-ratio low-impedance vias. This paper builds upon previous work on ground vias (single node) [8] but with a completely new process. This new work features backside patterning that allows for backside power, ground, and signal distribution on the same chip. Vias are now completely isolated from the silicon substrate, which was not accomplished using the previous process.

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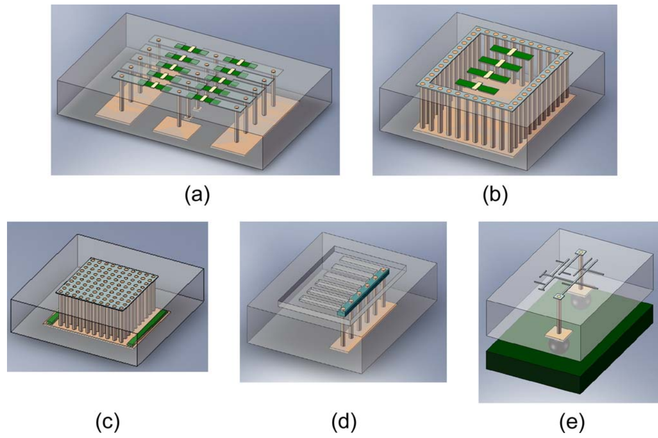

Fig. 1. Various applications of through-substrate interconnects in silicon. (a) Backside interconnect for power, ground, and signals. (b) Faraday cage for substrate noise isolation for SoC. (c) Integrated capacitors. (d) Backside contact for MEMS. (e) Backside package mount for SiP.

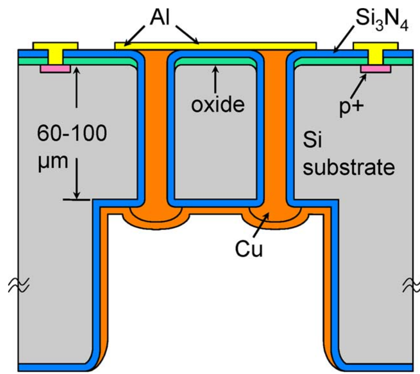

Fig. 2. Cross-sectional illustration of through-substrate vias.

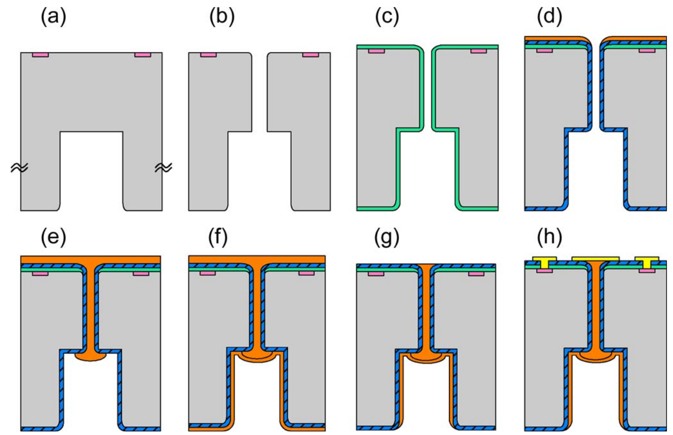

Fig. 3. Through-substrate via process flow. (a) Boron implant on the frontside and backside trenches etched by DRIE. (b) Through-substrate vias etched from frontside by DRIE. (c) Via sidewalls smoothed by growing and stripping oxide. (d) Oxide deposited on frontside, conformal silicon nitride liner deposited, and Ti-Cu seed deposited on frontside. (e) Via filled with Cu by electroplating. (f) Cu sputtered onto backside. (g) Cu removed from front and back of substrate by CMP. (h) Contact holes etched and Al pads deposited, patterned, and etched.

This paper represents an augmented version of a preliminary conference presentation of this work [4].

II. Fabrication

The through-substrate vias were fabricated on n- and p-type wafers (0.01–10 $\Omega \cdot$ cm). Wafers were locally thinned to 60–100 μm in backside trenches to emulate thin substrates without having to deal with them in this demonstration study. The vias in the same backside trench were connected to each other but not to vias in other trenches, so that power, ground, and signals could be routed on the backside of the same chip. Fig. 2 depicts a cross section of a completed through-substrate via.

A. Process Flow

The fabrication of through-substrate vias required the development and thorough characterization of new process steps before integrating into one complete process. The major process steps flow as follows: patterning the substrate backside, etching of the through-substrate via from the front, depositing a conformal dielectric liner, filling the via with electroplated copper, and removing excess copper by chemical–mechanical polishing (CMP). Improvements over previous work [8] and changes in the via process to accommodate backside patterning and new test structures include a deep reactive-ion etch (DRIE) for backside thinning, sidewall smoothing, a conformal silicon nitride liner, efficient copper electroplating, copper CMP, and the introduction of ohmic contacts to the substrate. These new steps are also an improvement over the via processes in [9]–[11].

Fig. 3 describes the through-substrate via process. First, boron is implanted for ohmic contacts using thermal oxide and resist as a mask [Fig. 3(a)]. To thin the wafers down to 60–100 μm, trenches were etched from the backside of the wafer using an anisotropic DRIE [Fig. 3(a)]. DRIE etches nearly vertical sidewalls so that the trenches had a much smaller footprint than when using a KOH etch [12], [13]. The through-substrate vias were also etched from the frontside by DRIE using resist and deposited oxide as a mask [Fig. 3(b)]. This was a through etch, so a handle wafer was needed to prevent etch gases from passing into the helium-cooled chuck. Because DRIE produces rough sidewalls, a thermal oxide was grown and then stripped to leave a smooth sidewall surface for the liner [Fig. 3(c)]. A 2000-Å oxide was then deposited on the frontside as an etchstop for contacts etched later in the process [Fig. 3(d)]. A conformal silicon nitride liner was deposited to protect the silicon substrate from copper diffusion from the copper core of the via [Fig. 3(d)]. Silicon nitride also electrically insulated the substrate from the via so signals could be routed through the substrate. More details are given in the next section.

Proceeding with metallization, a Ti-Cu seed was deposited on the frontside to facilitate copper electroplating that filled the via [Fig. 3(d)]. Due to the isotropic deposition of electroplating, the top of the via closed first and then filled from top to bottom [Fig. 3(e)]. Electroplating was stopped when copper protruded from the via into the backside trench. Next, copper was sputtered on the back and fully coated the inside of the DRIE trenches so that all the vias in one trench are connected to each another [Fig. 3(f)]. This provided a local connection

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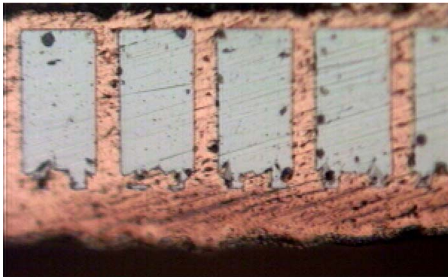

Fig. 4. Picture of vias (before CMP) 13 μm in diameter and 100 μm high ($AR = 8$).

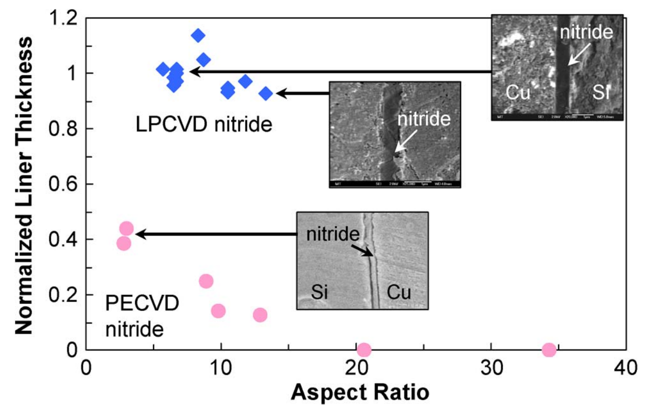

Fig. 5. Silicon nitride sidewall thickness normalized to surface thickness versus actual aspect ratio for PECVD nitride from previous work [8] and LPCVD nitride. The sidewall thickness was taken halfway down the via at the thinnest point of the liner.

for all the vias in the trench. The sputtered backside copper was removed by CMP to isolate each trench from one another while keeping the copper inside the trench intact [Fig. 3(g)]. The frontside copper was also removed using CMP to complete the copper damascene process [Fig. 3(g)]. More details are given below. Contact openings to the substrate were then etched through the silicon nitride and silicon dioxide films on the front surface [Fig. 3(h)]. Finally, aluminum was e-beam deposited, annealed, and patterned to form test structures [Fig. 3(h)]. The measured via diameters varied from 2 to 30 μm. The substrate thicknesses ranged from 60 to 100 μm. Fig. 4 shows a cross section of vias 13 μm in diameter and 100 μm high.

This demonstration project was fabricated to evaluate the electrical characteristics of through-substrate vias and not to propose a specific approach for manufacturing. The high-temperature steps, such as the thermal oxidation for sidewall smoothing and low-pressure chemical vapor deposition (LPCVD) silicon nitride, were chosen from the limited toolset available, and these steps would need alteration if this process was to be used in the back-end. More details of specific process steps are given next.

B. Silicon Nitride Liner

We used silicon nitride as the via liner material because of its barrier properties to copper diffusion and to electrically isolate the via from the silicon substrate [14]–[16]. Silicon nitride was deposited using LPCVD because of its higher conformality over plasma-enhanced chemical vapor deposition (PECVD). Fig. 5 shows measurements of PECVD and LPCVD silicon nitride thickness on the via sidewall divided by the surface thickness and plotted against via aspect ratio. The sidewall thickness measurement was taken halfway down the via at the thinnest point of the liner. The LPCVD nitride thickness is nearly constant all the way down the via, while PECVD nitride is minimal for aspect ratios higher than 15 [8].

C. Copper Electroplating

The low resistivity of copper allows for high current densities in interconnects, and copper has been proven to have increased scalability and better electromigration reliability than Al(Cu) interconnects [17]. Some of the disadvantages of copper are its poor adhesion to dielectrics and the need for barrier and/or adhesion layers [17]. However, copper has the critical advantage of being able to fill high-aspect-ratio holes by electroplating.

We used a commercial copper sulfate solution from Enthone-OMI and a Dynatronix DuPR 10-1-3 current supply with pulse-reverse current, which enhances electrodeposition into high-aspect-ratio structures. The dissolution of copper during the negative pulse provides a better concentration gradient of cupric ions in the via than a dc pulse, so that during the subsequent positive pulse, the deposition is more uniform and the void size is reduced [18]–[20]. After depositing a seed of 250 Å of titanium and 2000 Å of copper on the frontside of the wafer, the wafer was placed into the copper electroplating solution with the seed facing the anode. An average current density of 4.6 mA/cm^2 was applied. This blanket plating step produced an isotropic deposition of copper on the seed until the via closed at the top, as depicted in Fig. 6(a), similar to [8] and [9]. Due to the nonuniformity of the deposition, the wafer was rotated 180° halfway through the deposition. The cause for the nonuniformity is possibly due to a gradient of copper ions in the bath such that the deposition is greater at deeper levels in the bath. A faster stirring speed would enhance mixing but also increases the dissolved oxygen in the bath. Once most vias had closed, which was after about 75 min, the wafer was removed from the bath. The deposition rate was approximately 0.15 μm/min.

In the second step, the wafer was placed facedown into a Teflon jig so that the frontside would not be exposed to the copper solution [Fig. 6(b)]. The jig prevented excess copper from being electroplated onto the frontside so that less copper would have to be removed during CMP in a later stage. In addition, isolating the frontside seed from the solution significantly reduced the surface area to be plated so that a higher current density could be applied. The exposed area was actually too small because only a small amount of copper inside the vias was exposed to the solution. Therefore, two 22-cm^2 dummy pieces electrically connected to the cathode (wafer) were also placed into the solution on either side of the jig. An average pulse-reverse current of 12.5 mA/cm^2 was applied until all the vias were filled. The wafer was rotated 180° halfway through the deposition because of the nonuniformity of the plating bath, and then the vias were overfilled. Because the plated copper of the first plating step must traverse the opening to close the via,

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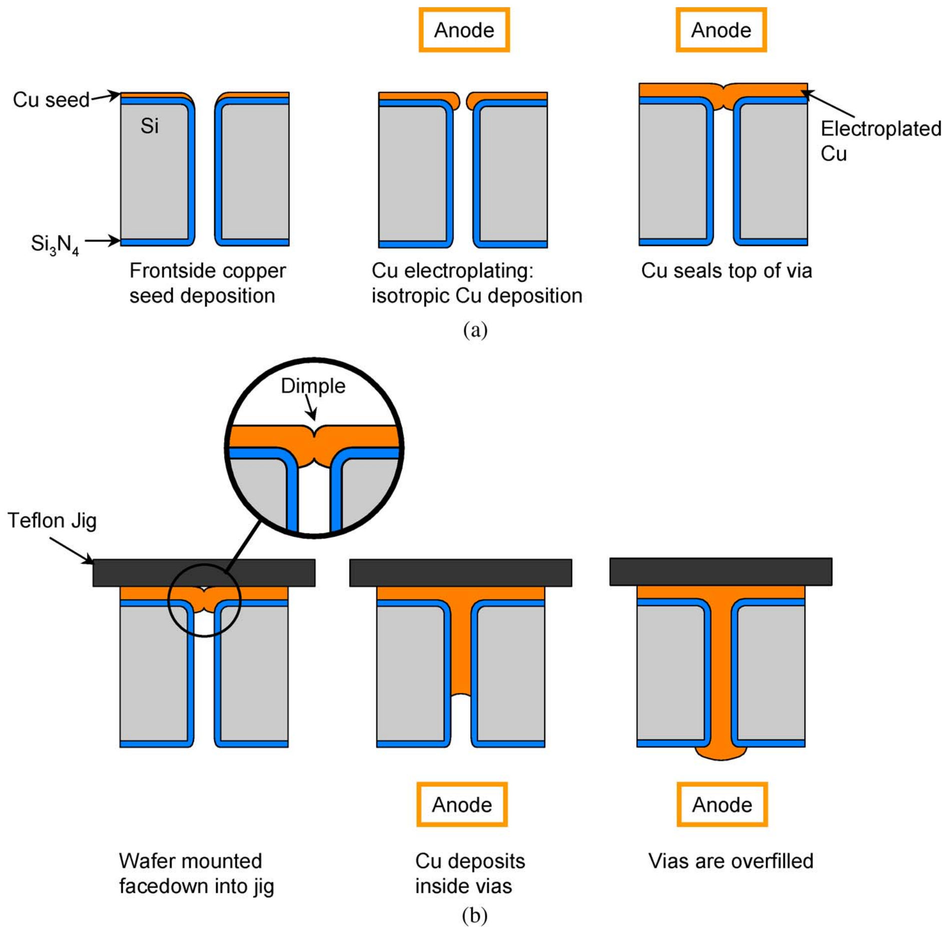

Fig. 6. Copper electroplating steps to reduce deposition time and excess copper buildup on the seed. (a) Blanket plating step. (b) Electroplating with wafer inserted into jig.

larger-diameter vias take longer to close and thus take longer to fill. To ensure that all the vias are filled with copper, the smaller-diameter vias become overfilled into the backside trenches. The deposition rate averaged around 1 μm/min. Using the jig, the amount of excess copper plated onto the seed reduced to 10–20 μm from 40 μm in our earlier process [8].

III. Measurement

We characterized the through-substrate vias by measuring the S parameters from 0.1 to 50 GHz of various coplanar ground–signal–ground RF test structures pictured in Fig. 7. The via impedance was extracted from S_{21} measurements of the two-port test structure in Fig. 7(a). The via under test lies in the center of the signal line and connects to a local ground plane inside the backside DRIE trench. This copper backplane lines the backside DRIE trench, which extends to the edge of the aluminum ground pads. The ground lines are punctuated by many vias to reduce the impedance from the copper backplane to the ground pads. The ground vias are 10 μm in diameter.

The sidewall capacitance of the via to the substrate was measured using one-port test structures like that in Fig. 7(b) on p^+ wafers ($< 0.03\ \Omega \cdot$ cm or less). To minimize the impact of pad capacitance, the test structures consist of arrays of 77 or 431 vias in parallel.

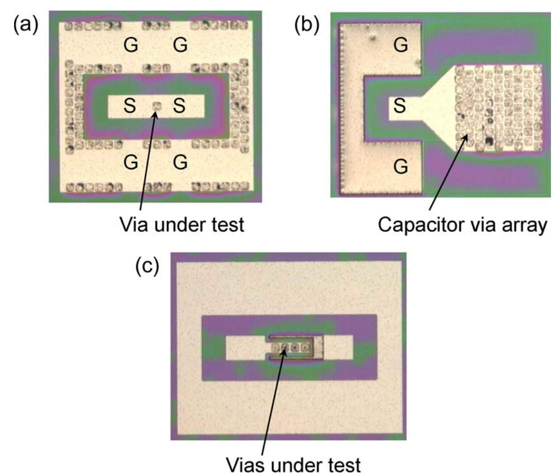

Fig. 7. Pictures of coplanar ground–signal–ground RF test structures. (a) Two-port impedance. (b) One-port capacitance: the signal is connected to the 77-via array, and the ground is the p^+ implant. (c) Leakage test structure.

The integrity of the liner was evaluated by measuring the current leakage across the silicon nitride liner using the test structure in Fig. 7(c). The left pad is connected to the top of the copper vias, which are arranged in arrays of one to four vias in parallel. The right pad is connected to the silicon surrounding the vias through an ohmic contact to the substrate. The via

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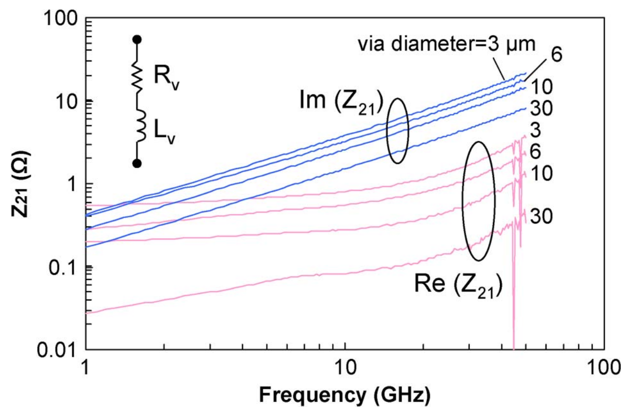

Fig. 8. Z_{21} (converted from S_{21}) versus frequency for vias of diameter 3, 6, 10, and 30 μm. The real part represents resistance and rises at high frequency due to the skin effect. The imaginary part increases with a slope of 1, indicating inductive behavior.

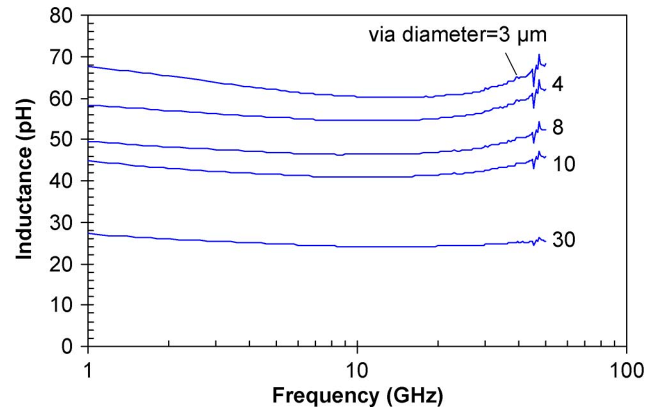

Fig. 9. Inductance L_v versus frequency for vias of diameter 3, 4, 8, 10, and 30 μm.

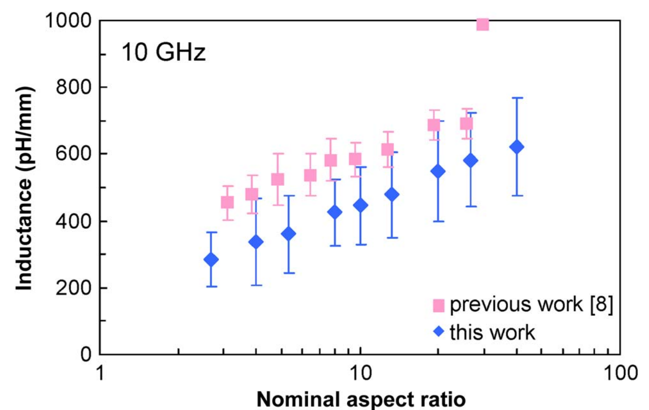

Fig. 10. Via inductance per unit length versus nominal aspect ratio of a via at 10 GHz. The via diameters ranged from 2 to 30 μm. The via height ranged from 60 to 100 μm, so an average of 80 μm was used for aspect ratio. The measured inductance data (blue diamonds) falls below previous work [8] (pink squares) by using a two-port test structure and improved process.

diameter was varied from 2 to 10 μm. The current leakage across the larger via arrays in Fig. 7(b) was also measured.

The through-substrate vias were measured using 125-μm pitch GGB Industries Inc. microwave probes. The probes were connected to an HP8510C network analyzer for S parameter measurements up to 50 GHz. The power was set to 10 dBm and 0-dB attenuation. For the two-port impedance test structure, S_{21} was measured from 100 MHz to 50 GHz. For the one-port capacitance test structure, S_{11} was measured up to 50 GHz. The measured S parameter data were converted to Z parameters for analysis. The leakage current was measured on the same probe station but using dc probes and an HP4155. The wafer chuck was grounded to the HP4155 in all the measurements.

Additional test structures were also fabricated to test the substrate crosstalk isolation properties of several Faraday cage designs [4]. A full report on these findings is forthcoming.

IV. Results and Discussion

From the converted Z parameter data, we extracted the inductance, resistance, and sidewall capacitance of a single via. Simple circuit models and theoretical calculations are used to explain these results.

A. Via Inductance and Resistance

Z_{21} measurements of the impedance test structure in Fig. 7(a) are plotted in Fig. 8 for different via diameters. Looking at the real and imaginary parts of Z_{21}, a through-substrate via can be represented by a simple circuit model of a resistor and an inductor in series. The real part represents the via resistance R_v, and the imaginary part ωL_v linearly rises with frequency and represents the susceptance, which is associated with inductance. From this circuit model, the resistance and inductance of a single via can be extracted. Fig. 9 plots the inductance L_v against frequency.

As shown in Fig. 8, although the real part should remain constant, it rises with frequency due to the skin effect. At high frequencies, the resistance increases as current crowds to the sidewalls of the via. Current travels along the copper via sidewall down to the skin depth. At 1 GHz, the skin depth in copper is 2.1 μm and decreases to 0.3 μm at 50 GHz. This is thin enough to affect the resistance and inductance in even the smallest diameter via.

The inductance at 10 GHz was extracted from data in Fig. 9 and other measurements and is plotted in Fig. 10 (blue diamonds) against nominal aspect ratio. The inductance falls significantly below our previous work [8] (pink squares). We attribute this to the reduced parasitics of the new two-port test structure and a superior process. Previous work fabricated vias using a PECVD nitride that was not completely conformal, and the measurements used a one-port test structure. The new results shown in Fig. 10 represent the lowest inductance reported for high-aspect-ratio (> 4) through-substrate vias [10], [11].

The extracted resistance was taken at 1 GHz to minimize the effects of skin depth and is plotted in Fig. 11 (blue diamonds) against nominal aspect ratio. The resistance is approximately 1 Ω or less and decreases with via diameter. The resistance data from previous work [8] are also plotted in Fig. 11. The new via measurements showed a significant drop in resistance compared with previous work [8] with less scatter. This is likely due to the lower parasitics of the two-port structure. There is a discrepancy between the extracted resistance and the theoretical

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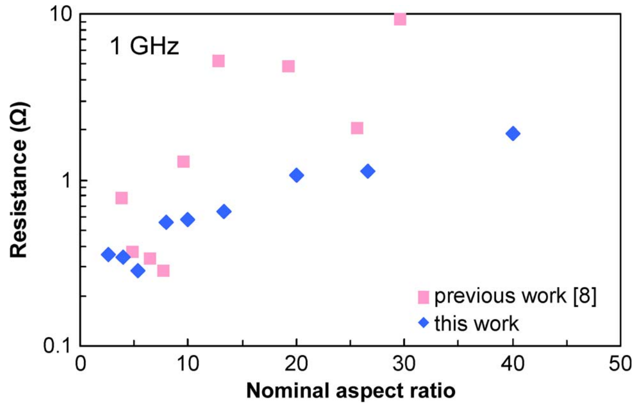

Fig. 11. Via resistance versus nominal aspect ratio of a via at 1 GHz. Via diameters ranged from 2 to 30 μm, and via height was averaged to 80 μm. The measured data (blue diamonds) have lower resistance than previous work [8] (pink squares) by using a two-port test structure.

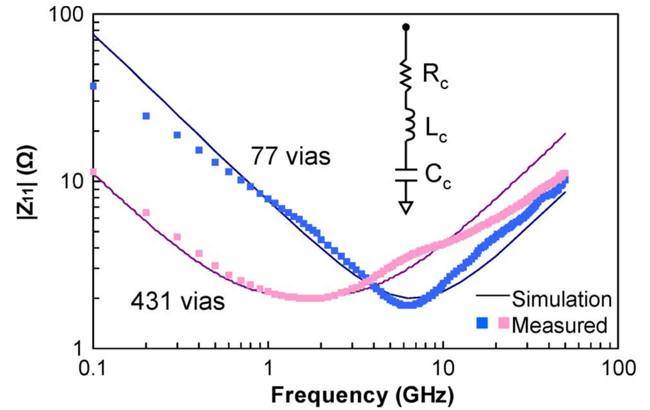

Fig. 12. $|Z_{11}|$ versus frequency for via arrays of 77 and 431 vias measured using the capacitance test structure in Fig. 7(b). The vias are approximately 95 μm tall and nominally 10 μm in diameter. This structure can be represented by a capacitor in series with a resistor and inductor. Simulations of this model are plotted in the solid line for each via array. The via sidewall capacitance was extracted from this model.

resistance, which can be attributed to parasitics of the two-port test structure and contact resistance. De-embedding structures were not fabricated for this test structure.

B. Sidewall Capacitance

The sidewall capacitance of the via to the substrate was measured using the one-port test structure in Fig. 7(b) on p^+ wafers. To minimize the impact of pad capacitance, the test structure consists of arrays of 77 or 431 vias in parallel. The vias are nominally 10 μm in diameter and spaced by 10 μm. Fig. 12 plots $|Z_{11}|$ against frequency for each array size. We find that $|Z_{11}|$ follows a simple model of a capacitor, resistor, and inductor in series, for which

$$Z_{11} = R_c + j\left(\frac{\omega^2 L_c C_c + 1}{\omega C_c}\right) \tag{1}$$

where R_c is the total resistance of the via array, L_c is the total inductance of the via array, and C_c is the total capacitance of the via array test structure. The resonant frequency is

$$\omega_0 = \sqrt{\frac{1}{L_c C_c}} \tag{2}$$

which occurs at the minimum $|Z_{11}|$, as shown in Fig. 12. At frequencies below the resonant frequency, C_c dominates so that

$$|Z_{11}| \simeq \frac{1}{\omega C_c} \tag{3}$$

and so the sidewall capacitance was extracted at these frequencies. To verify this circuit model, we simulated it with Agilent ADS software using the extracted resistor, capacitor, and inductor values. The simulations closely match the measured data, as shown in Fig. 12. The mismatch at high frequencies is due to the skin effect.

The average extracted capacitance and inductance of the via arrays are plotted in Fig. 13. For the 77-via array, the average capacitance was 20 pF, and for the 431-via array, the average capacitance was 132 pF. The single-via data points were obtained from average measurements of the test structure in Fig. 7(a). Taking the slope of the capacitance line, we get a

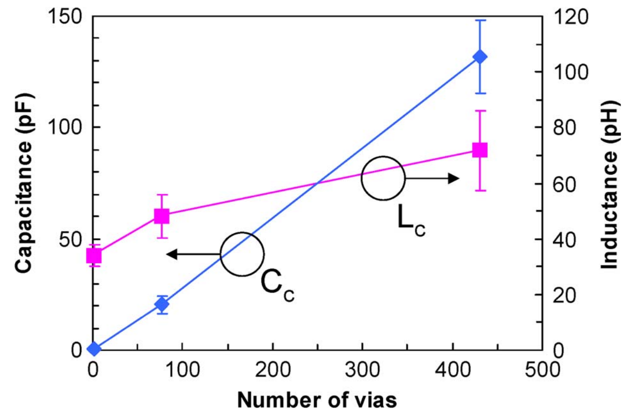

Fig. 13. Extracted capacitance and inductance from measurements of Fig. 7(b). The width of the error bars is one standard deviation. The capacitance is roughly linear with the number of vias. The inductance increases with the number of vias due to mutual inductance.

capacitance of 0.31 pF for an individual via. This approaches the theoretical capacitance of 0.33 pF for a 10-μm-diameter 100-μm-high via with a 7000-Å silicon nitride liner. Nearly perfect scaling of capacitance with the number of vias is shown in Fig. 13. Using vias with a 1 : 1 pitch for high-density integrated capacitors, the expected capacitance per footprint area is about 0.1 $\mu\mathrm{F/cm^2}$, similar to thin-film capacitors. By increasing the aspect ratio to our processing limit of 50, 0.4 $\mu\mathrm{F/cm^2}$ can be reached. By decreasing the silicon nitride thickness from 700 to 100 nm, an even greater capacitance of 2.7 $\mu\mathrm{F/cm^2}$ is attainable. A higher capacitance density will require a dielectric with a higher dielectric constant. This is promising for via applications such as decoupling capacitors and integrated capacitors.

The through-substrate vias in the large via arrays in the capacitance test structure [Fig. 7(b)] are connected in parallel. An interesting finding in this structure is that the total extracted inductance actually increases as more vias are placed in parallel, as shown in Fig. 13. This is due to the mutual inductance of the via array. (The resistance changes little because it is swamped by the parasitic resistance of the one-port test structure.) With more vias in parallel, the self-inductance decreases, but the

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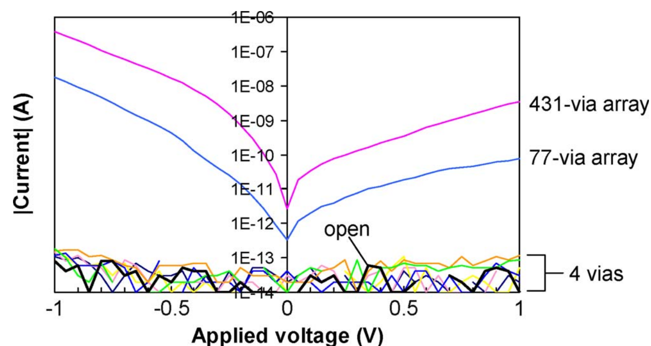

Fig. 14. Current leakage versus applied voltage across four vias in parallel for different via diameters (2–10 μm) and for 77- and 431-via arrays. The via diameter is 10 μm for the via arrays. The leakage for the open test structure is indicated by a thick black line.

mutual inductance increases faster, so that the total inductance goes up. This is an important consideration when using these vias in high-frequency circuits.

C. Liner Integrity

We tested the integrity of the LPCVD silicon nitride liner by measuring the current leakage through the via sidewall using the test structures in Fig. 7(b) and (c) on p^+ wafers. Fig. 14 plots the measured current across the liner of several test structures against an applied voltage of -1 to 1 V. In the four-via structure [Fig. 7(c)], the leakage was measured from the copper via to the silicon substrate for via diameters of 2 to 10 μm. In all cases, the current leakage is in the sub-pA range and lies within the same current range as the open test structure. These currents are below the noise floor of the measurement setup. However, measurements of the larger via arrays in Fig. 7(b) showed that some vias were actually shorted to the substrate. The via arrays that were not shorted had current leakage less than 1 μA for the 431-via array and sub-pA to 100-nA range for the 77-via array. Fig. 14 shows measurements of each size via array that was not shorted.

It is not entirely clear if the shorts were due to defects in the liner in the via sidewall or at the top surface. It is likely that during the nitride etch step, the photoresist was thinner around the edges of the via in the via arrays due to the uneven coating over the vias. The unprotected silicon nitride was etched, revealing the silicon substrate. In addition, the nitride was already thinner at this step due to CMP.

V. Conclusion

We have developed a versatile through-substrate interconnect technology with minimal impedance that allows for backside routing of power, ground, and signals for 3-D and SiP integration, low-ground inductance for RFICs, substrate noise isolation for mixed-signal circuits, and a backside contact for MEMS.

S parameter measurements of the through-substrate vias show that the copper via can be represented by a simple equivalent circuit of a resistor and inductor in series, from which the via resistance and inductance were extracted. The resistance was less than 1 Ω and decreased with via diameter. The via inductance was the lowest ever reported for vias of aspect ratio greater than 4. Using via arrays, the extracted via sidewall capacitance matched the theoretical capacitance calculations of a single via 10-μm diameter and 100 μm high. Fully characterizing the through-substrate vias provides the basis for vias to be incorporated in circuits and other applications.

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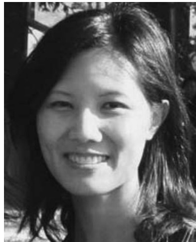

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