Effect of Substrate Contact Shape and Placement on RF Characteristics of 45 nm Low Power CMOS Devices

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***Abstract*—The substrate resistance of 45 nm CMOS devices shows a strong dependence on the distance between the device edge and the substrate contact ring, as well as on the number of sides that the surrounding ring contacts the substrate. We find that the unilateral gain is impacted by the substrate resistance (R_{sx}) through the gate-body capacitance feedback path at low to medium frequencies (<20 GHz). At mm-wave frequencies, the unilateral power gain is affected by R_{sx} through the drain-body capacitance pole, and the unilateral power gain deviates from the ideal -20 dB/dec slope. Within the range of designs that have been studied, the impact of substrate resistance on f_T, maximum available gain, high frequency noise and power characteristics of the devices is minimal.**

***Index Terms*—Maximum oscillation frequency, noise, power gain, RF CMOS, substrate resistance, unilateral gain.**

I. Introduction

CMOS is becoming an increasingly popular choice for radio frequency (RF) circuits and system-on-chip designs. It is well known that parasitic substrate resistance adversely affects the high frequency performance of CMOS devices. A commonly used method for reducing substrate resistance is to place substrate contacts in a ring around the MOSFET. The dependence of substrate resistance on the number of device fingers has been extensively studied [1]–[5]. However, the effect of substrate contact ring shape and proximity has not been fully explored. In addition, previous work is limited to the modeling of substrate resistance; its impact on RF circuit design and power gain has not been well explained.

This work presents a detailed study of the impact of substrate ring shape and placement on the substrate resistance and high frequency figures of merit of 45 nm CMOS devices. Section II presents measured results for substrate resistance, cut-off frequency (f_T) and maximum oscillation frequency (f_{max}) for structures with varying gate finger shape and varying substrate ring shape and position relative to the device. Section III proposes a model to explain the measured dependence of unilateral gain and f_{max} on substrate resistance. Section IV discusses the implications of substrate resistance on power gain, power added efficiency, unilateral gain, and high frequency noise of CMOS devices.

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II. Measurements

Multi-finger NFET and PFET test structures with varying gate finger shape and varying substrate contact ring shape and placement were designed and fabricated using IBM's 45 nm low-power RFCMOS process [5]. All devices have a gate length of 0.04 μm. The total gate width ranges from 10 μm to 180 μm, with unit finger widths ranging from 1 μm to 5 μm. The substrate ring is 0.16 μm wide and is always at a distance of 0.46 μm from the device edge in the direction perpendicular to the gate and 0.53 μm in the direction parallel to the gate, unless otherwise stated. The devices are laid out in a common-source configuration with body node tied to the source. The designs for NFETs and PFETs are identical except for the fact that NFETs are placed directly on the p-type wafer, while the PFETs are placed inside the N well.

S-parameter measurements from 1 GHz to 110 GHz were performed on these test devices at $V_{GS} = 0$ V and $V_{GS} = \pm 0.8$ V and $V_{DS} = \pm 1.1$ V using an Agilent 8510 network analyzer. The measured S-parameters were de-embedded using on-wafer open and short structures that were custom designed for each device. Power measurements at 6 GHz were performed using an ATN electronic load-pull system. High-frequency noise parameter measurements were also performed in the 1 GHz to 26 GHz range using an ATN noise setup with electronic tuners.

The substrate resistance was estimated from the zero gate bias S-parameter data using the following expression [1]:

$$R_{sx} = \frac{real(Y_{22})}{\left(imag(Y_{22} + Y_{12})\right)^2}. \quad (1)$$

This procedure leads to a value of R_{sx} that is constant with frequency at low frequencies (up to around 20 GHz), but starts decreasing at higher frequencies because of the presence of substrate coupling capacitances. Hence, in this work, we use the extracted value at low frequency as the value of R_{sx}.

Fig. 1 shows the extracted substrate resistance for NFETs and PFETs as a function of gate finger width (W_f). The number of fingers (NF) was held constant at 30 for all these device structures. The lower R_{sx} for PFETs is due to the lower sheet resistance of the N-well region compared to the p-substrate. R_{sx} for both NFETs and PFETs decreases with increasing finger width.

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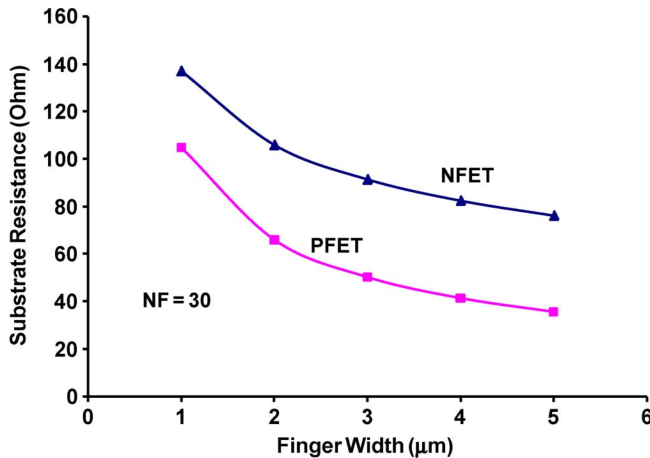

Fig. 1. Substrate resistance for NFETs and PFETs as a function of unit finger width. Number of fingers = NF = 30.

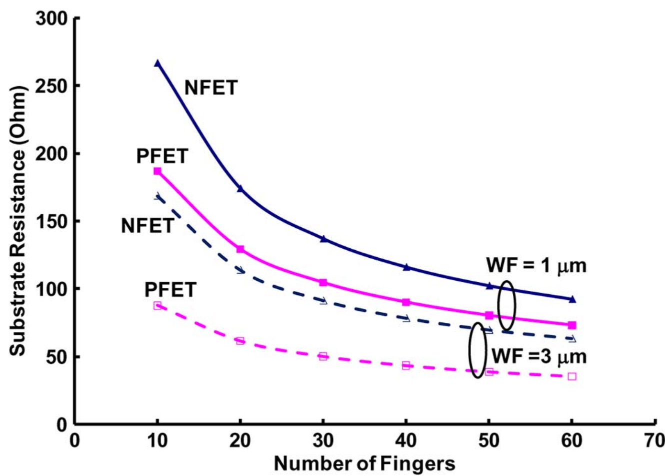

Fig. 2. Substrate resistance for NFETs and PFETs as a function of number of fingers for two values of unit finger width.

However, the decrease is not as steep as the $1/\mathrm{W_f}$ behavior modeled in [2]. The decrease in $\mathrm{R_{sx}}$ for NFETs exhibits a $\mathrm{W_f^{-0.4}}$ behavior, while the $\mathrm{R_{sx}}$ for PFETs shows $\mathrm{W_f^{-0.7}}$ dependence. The reason for this discrepancy is because [2] only considers the substrate coupling of the drain and source junctions to the side contacts $(\mathrm{R_{sxh}})$ and neglects the coupling to the top and bottom substrate contacts $(\mathrm{R_{sxv}})$. The total substrate resistance is the parallel combination of $\mathrm{R_{sxh}}$ and $\mathrm{R_{sxv}}$ [1]. $\mathrm{R_{sxh}}$ shows a $1/\mathrm{W_f}$ behavior, but $\mathrm{R_{sxv}}$ is independent of $\mathrm{W_f}$ [1]. Further $\mathrm{R_{sxv}}$ is much smaller than $\mathrm{R_{sxh}}$ [1] and hence dominates the total $\mathrm{R_{sx}}$. This explains the weak dependence of $\mathrm{R_{sx}}$ on $\mathrm{W_f}$.

The substrate resistance for NFETs and PFETs with finger width of 1 μm and 3 μm and varying number of fingers is shown in Fig. 2. $\mathrm{R_{sx}}$ decreases with increasing number of fingers similar to what was seen in [1], [2].

To explore the effect of sharing a substrate ring between adjacent devices, we designed NFETs and PFETs with varying distance between the device edge and the substrate ring. All the devices in this set have a gate width of 20×3 μm. We vary the distance between the device edge and substrate ring, in a direction parallel to the gate (X) and perpendicular to the gate (Y). The reference device has a dedicated substrate ring with $\mathrm{X} = 0.53$ μm and $\mathrm{Y} = 0.46$ μm and a substrate ring width of 0.16 μm.

Keeping X constant at 0.53 μm and varying Y from 0.46 μm to 7 μm increases $\mathrm{R_{sx}}$ by 16% for NFETs (Fig. 3). Varying X, with Y constant at 0.46 μm, results in a greater increase of $\mathrm{R_{sx}}$ by 23%. The biggest increase in $\mathrm{R_{sx}}$ is seen when both X and Y are increased simultaneously. An increase of 142% is observed for $\mathrm{X} = \mathrm{Y} = 7$ μm, as compared to the reference device. These results can be explained as follows: When only X or Y is increased, the closest contact becomes the de facto contact to the substrate. Also, having the substrate contact perpendicular to the gate (the case of X short) ensures proximity of the contact to more of the drain fingers resulting in lower $\mathrm{R_{sx}}$. Fig. 3 also shows that increasing the substrate contact ring width from 0.16 μm to 0.32 μm decreases $\mathrm{R_{sx}}$ of NFETs by 17%.

Fig. 4 shows the substrate resistance for PFETs as a function of the distance between device edge and the substrate ring. The increase in $\mathrm{R_{sx}}$ for PFETs shows similar trends to that of NFETs, with the maximum change occurring when both X and Y are increased simultaneously. $\mathrm{R_{sx}}$ is again lowest when the closest contact is perpendicular to the gate ($\mathrm{X} = 0.53$ μm case). The slight differences in percentage of change in $\mathrm{R_{sx}}$ for PFETs and NFETs can be explained by the differences in the shape of N-well and P-substrate.

A different set of test structures, with a gate width of 60×3 μm, were designed to explore the shape of the substrate ring. To facilitate wiring or to achieve a more compact design, designers may choose to omit portions of the substrate ring, either from both the diffusion and Metal 1 (M1) ring (RX+M1), or from the M1 ring alone. In one variation, RX+M1 ring is varying: either on all four sides (reference, in Fig. 5), on three sides (RX+M1 U-shape), on two sides (RX+M1 L-shape), or on one side (RX+M1 top) of the device. An increase in $\mathrm{R_{sx}}$ of 64% is observed in NFETs when going from a full substrate ring to a one-sided contact (Fig. 5).

Fig. 5 also shows the substrate resistance for the set of designs that vary the M1 portions of the ring only: either on three sides of the device (M1 U-shape), on one side and perpendicular to the gate (M1 Top) or on one side and parallel to the gate (M1 Left). The diffusion ring is always present in this case. The substrate resistance for this set of devices is lower than when both diffusion and M1 are varied, as one would expect. Also $\mathrm{R_{sx}}$ is higher when the substrate contact is parallel to the gate direction than when it is perpendicular to the gate. This is because most fingers are relatively far away from the contact bar when this is parallel to the gate.

The effect of contact ring shape on substrate resistance of PFETs can be seen in Fig. 6. The dependencies are similar to those seen in NFETs. $\mathrm{R_{sx}}$ is higher when both diffusion and metal are omitted from the ring than when only portions of metal are omitted from the contact ring. PFET $\mathrm{R_{sx}}$ increases by 33% in going from a three-sided contact to a one-sided contact.

Fig. 7 shows the change in the unity current gain cut-off frequency $(\mathrm{f_T})$ and the maximum oscillation frequency $(\mathrm{f_{max}})$ for NFETs and PFETs as a function of the distance between the device edge and the substrate ring. Fig. 8 shows $\mathrm{f_T}$ and $\mathrm{f_{max}}$ for variations in substrate ring shape. No significant difference is observed in $\mathrm{f_T}$ in Fig. 7 and Fig. 8 because the variation in gate

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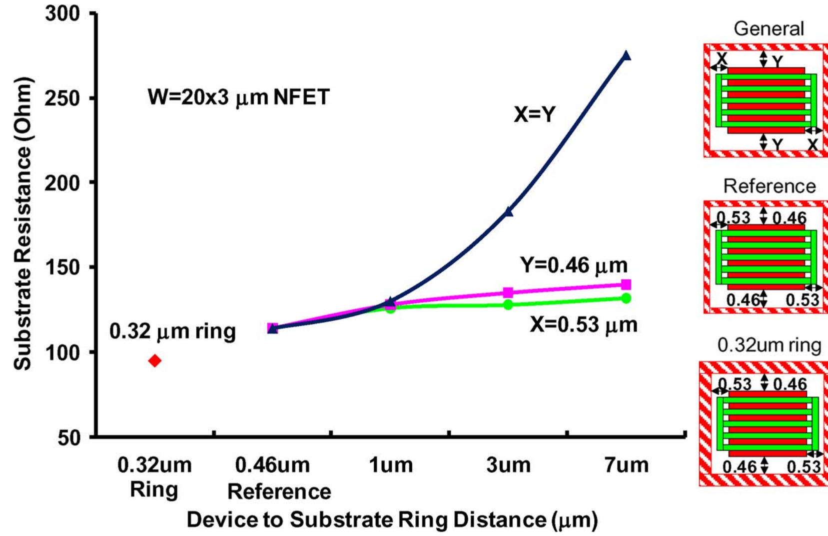

Fig. 3. Substrate resistance for NFETs as a function of distance between device edge and substrate contact ring in the gate width (X) and gate length (Y) directions. Substrate ring width $= 0.16\ \mu$m for all data points except for the one that corresponds to a ring width of $0.32\ \mu$m.

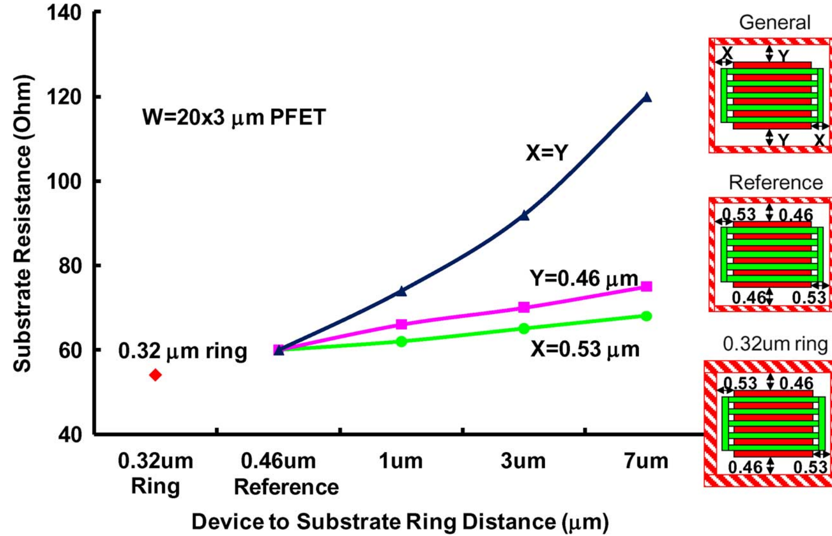

Fig. 4. Substrate resistance for PFETs as a function of distance between device edge and substrate contact ring in the gate width (X) and gate length (Y) directions. Substrate ring width $= 0.16\ \mu$m for all data points except for the one that corresponds to a ring width of $0.32\ \mu$m.

parasitic capacitance, for the structures studied here, is not significant enough to change f_T. The data also shows negligible variation in f_{max} in spite of the change in substrate resistance (maximum increase 142%). The reasons behind these results are explored in the next section.

III. Model

A model for the high frequency figures-of-merit can be derived based on the small signal equivalent circuit shown in Fig. 9. The circuit includes gate resistance (R_g), gate-source (C_{gs}), gate-drain (C_{gd}), gate-body (C_{gb}), source-body (C_{sb}) and drain-body (C_{db}) capacitances, transconductance (g_m), output resistance (r_o), and substrate resistance (R_{sx}). Previous studies [1]–[4] have ignored the presence of C_{gb}, which will be shown to affect the unilateral gain significantly, even with a value as small as 2 fF that arises from fringe capacitance.

The intrinsic parameters are extracted from S-parameter measurements using the following extraction methodology [6], [7]:

$$R_G = real(Z_{11} - Z_{12}) \quad C_{gs} = \frac{imag(Y_{11} + Y_{12})}{\omega}$$
$$g_m = real(Y_{21}) \quad C_{gd} = -\frac{imag(Y_{12})}{\omega}$$
$$r_o = \frac{1}{real(Y_{22})} \quad C_{db} = C_{sb} = \frac{imag(Y_{22} + Y_{12})}{\omega}.$$

R_{sx} is determined from the zero bias s-parameter data using (1). The value of C_{gb} is determined by fitting the equivalent circuit model to the measured s-parameter data in Agilent ADS. For the $20 \times 3\ \mu$m reference NFET, biased at $V_{GS} = 0.8$ V and $V_{DS} = 1.1$ V, the extracted small-signal parameters are: $C_{gs} = 27$ fF, $C_{gd} = 14$ fF, $g_m = 48.4$ mS, $r_o = 192\ \Omega$, $C_{db} = C_{sb} = 37$ fF, $R_{sx} = 76\ \Omega$ and $C_{gb} = 2$ fF.

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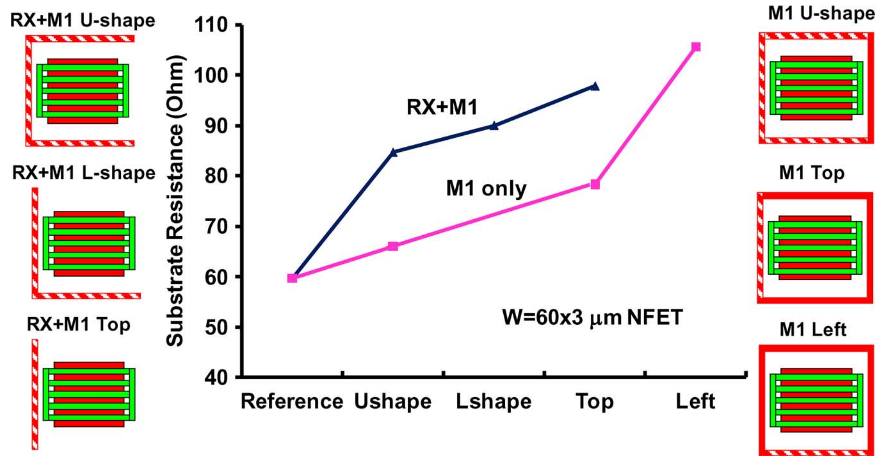

Fig. 5. Substrate resistance for NFETs with different substrate ring shapes. The striped area in the ring contains both diffusion and metal 1 layers, while the solid area contains only diffusion. The reference device has an RX+M1 ring on all sides of the device as seen in Fig. 3.

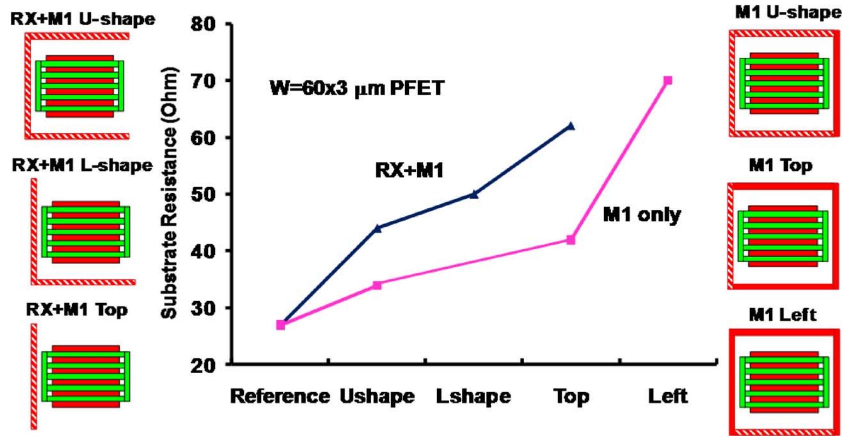

Fig. 6. Substrate resistance for PFETs with different substrate ring shapes. The striped area in the ring contains both diffusion and metal 1 layers, while the solid area contains only diffusion. The reference device has an RX+M1 ring on all sides of the device as seen in Fig. 4.

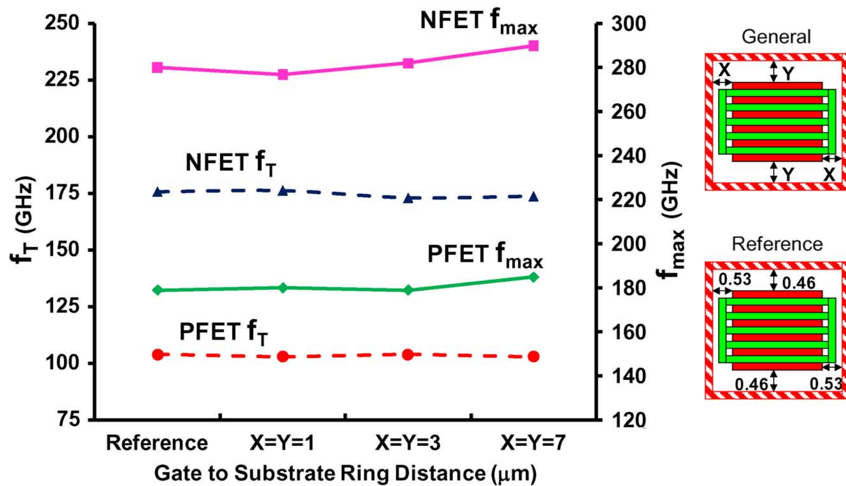

Fig. 7. f_T and f_{max} for NFETs and PFETs (measured at $V_{GS} = 0.8$ V and $V_{DS} = 1.1$ V) as a function of device edge to substrate contact ring distance. $W = 20 \times 3\ \mu$m.

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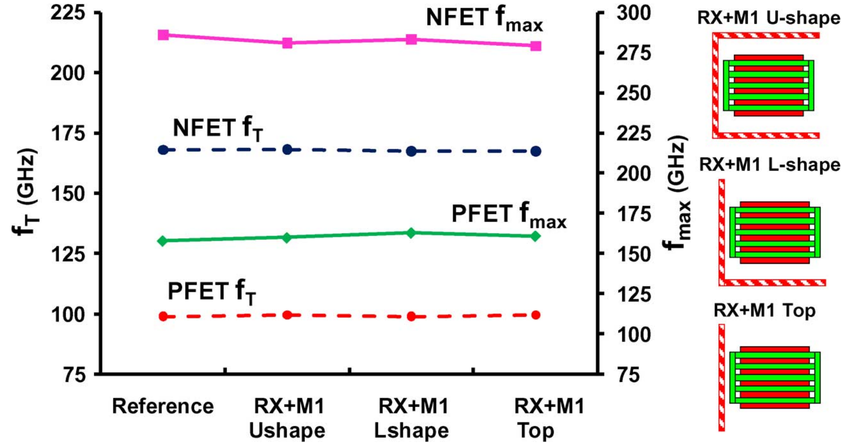

Fig. 8. f_T and f_{max} for NFETs and PFETs with different substrate contact ring shapes. $V_{GS} = 0.8$ V, $V_{DS} = 1.1$ V. $W = 60 \times 3$ μm.

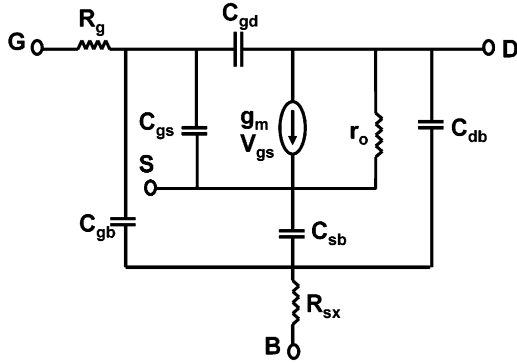

Fig. 9. Small-signal equivalent circuit representing the intrinsic device parameters of CMOS transistor.

The y-parameters for the above equivalent circuit can be derived as follows:

$$Y_{11} \approx \frac{j\omega C_{gg}}{1 + R_g j\omega C_{gg}}, \text{ where } C_{gg} = C_{gs} + C_{gd} + C_{gb} \tag{2}$$

$$Y_{12} \approx \frac{-j\omega C_{gd}}{1 + R_g j\omega C_{gg}} + \frac{\omega^2 C_{db} C_{gb} R_{sx}}{(1 + R_g j\omega C_{gg})) \cdot (1 + R_{sx} j\omega (C_{sb} + C_{db} + C_{gb}))} \tag{3}$$

$$Y_{21} \approx \frac{g_m - j\omega C_{gd}}{1 + R_g j\omega C_{gg}} + \frac{\omega^2 C_{db} C_{gb} R_{sx}}{(1 + R_g j\omega C_{gg})) \cdot (1 + R_{sx} j\omega (C_{sb} + C_{db} + C_{gb}))} \tag{4}$$

$$Y_{22} \approx \frac{1}{r_o} + \frac{j\omega C_{gd} (1 + g_m R_g + j\omega (C_{gs} + C_{gb}) R_g)}{1 + R_g j\omega C_{gg}} + \frac{j\omega C_{db} (1 + j\omega (C_{gb} + C_{sb}) R_{sx})}{1 + j\omega (C_{gb} + C_{sb} + C_{db}) R_{sx}}. \tag{5}$$

The accuracy of our equivalent circuit parameter extraction methodology is illustrated in Fig. 10. The Smith chart shows measured s-parameters and modeled s-parameters (generated in Agilent ADS by simulating the extracted small-signal equivalent circuit) for the 20×3 μm reference NFET. The model shows reasonable agreement with the measured data. The model fit for

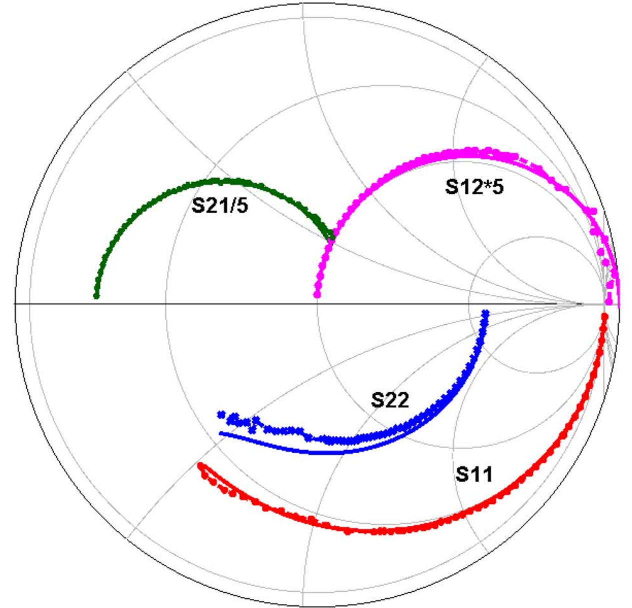

Fig. 10. Measured and modeled S-parameters for 20×3 μm NFET at $V_{GS} = 0.8$ = V, $V_{DS} = 1.1$ V. Measured data are in symbols and the model are the solid lines.

S_{22} at high frequencies could possibly be improved by considering a distributed substrate resistance as in [5], [8].

The above expressions for y-parameters clearly show that Y_{11} is independent of R_{sx} (eq. (2)). For Y_{21}, the first term in (4) dominates, thus making Y_{21} also independent of R_{sx}. The current gain can be written in terms of y-parameters as $h_{21} = Y_{21}/Y_{11}$. Hence, the current gain and the resulting unity gain cut-off frequency (f_T) are also insensitive to R_{sx}. The maximum stable gain, defined as $\text{MSG} = |Y_{21}|/|Y_{12}|$, shows a slight dependence on R_{sx} for $R_{sx} > 20$ Ω. However, the dependence is very weak with MSG decreasing by less than 2% for a 100% increase in R_{sx}.

The unilateral power gain, on the other hand, can depend on the substrate resistance. In terms of y-parameters, U can be expressed as [9]

$$U = \frac{|Y_{12} - Y_{21}|^2}{4\,[\text{Re}(Y_{11})\text{Re}(Y_{22}) - \text{Re}(Y_{12})\text{Re}(Y_{21})]} \tag{6}$$

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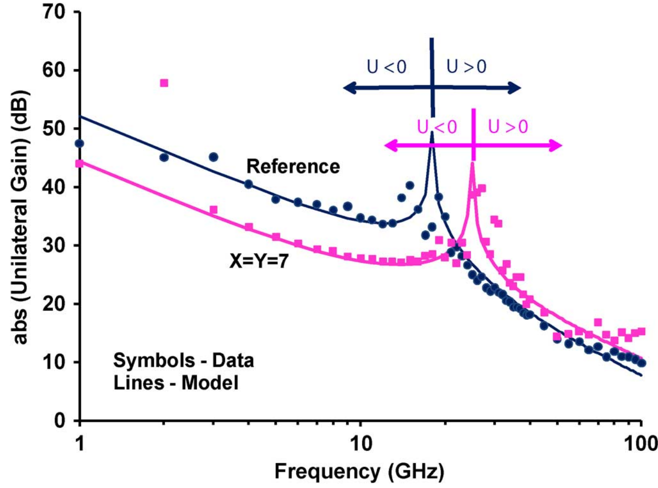

Fig. 11. Effect of increase in R_{sx} on the measured and modeled U of NFETs. $W = 20 \times 3\ \mu m$. $V_{GS} = 0.8$ V, $V_{DS} = 1.1$ V. $R_{sx} = 114\ \Omega$ for reference device and $R_{sx} = 275\ \Omega$ for NFET with $X = Y = 7\ \mu m$.

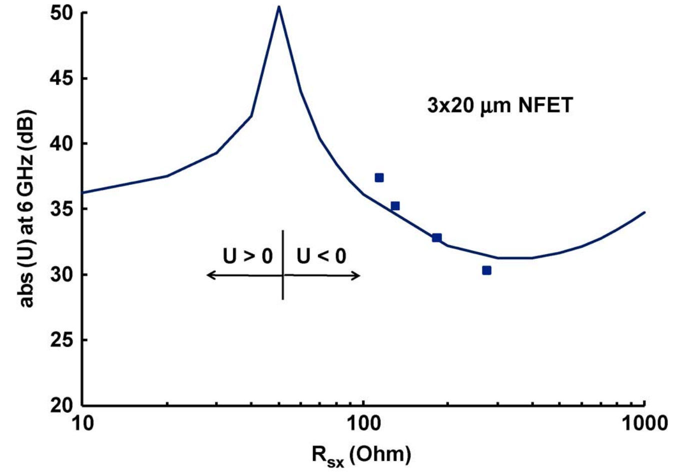

Fig. 12. Effect of increase in substrate resistance of $2 \times 30\ \mu m$ NFET on the modeled unilateral gain at 6 GHz. Measured data shown as symbols.

A simplified expression for U can be obtained by realizing that $C_{gb} \ll C_{gs}$ or C_{gd} for our devices and that $\omega^2 R_g C_{gg}^2 \ll 1$ for the frequencies and parameter values being explored in this work. Retaining only the significant terms, U can be approximated as in equation (7) at the bottom of the page.

The traditional unilateral gain derivation only considers the first 2 terms in the denominator of (7) [9]. We include the new effect of R_{sx} and its interaction with C_{gb} and C_{db} which is captured by the following two terms.

Fig. 11 plots the measured and modeled U (modeled using (7)) for the reference NFET and the device with $X = Y = 7\ \mu m$ which shows the highest increase in R_{sx} in our experiments. Our small-signal model is in reasonable agreement with the data for both devices. The slight discrepancy at very high frequencies (> 60 GHz) could be due to our simplistic model for substrate resistance. Using a more complicated and distributed model for substrate resistance as in [5], [8] could improve the model-data fit at these very high frequencies. Note that U is negative at low to medium frequencies (up to about 20 GHz). In this frequency range, the unilateral gain can be simplified to the form shown in the following:

$$U_{LF-MF} \approx \frac{g_m^2 r_o}{4R_g C_{gg}\omega^2 \left[C_{gg} + g_m r_o C_{gd} - \dfrac{R_{sx} g_m r_o C_{gb} C_{db}}{R_g C_{gg}}\right]}. \tag{8}$$

In the presence of substantial R_{sx} and C_{gb}, the third term in the denominator of (8) dominates leading to negative U. The physical mechanism is that C_{db}, C_{gb}, and R_{sx} create a positive feedback path between gate and drain, resulting in negative unilateral gain.

In order to further understand the role of R_{sx} in the unilateral gain, Fig. 12 plots the modeled unilateral gain at 6 GHz for the $20 \times 3\ \mu m$ reference NFET as a function of R_{sx}. For this exercise, R_{sx} is varied keeping all other small-signal parameters constant, and U is calculated using (7). Increasing R_{sx} from zero will initially cause the denominator of (8) to decrease resulting in an increase in U. As R_{sx} increases further (around 50 Ω for these devices), the third term in the denominator of (8) dominates making U negative. Further increase in R_{sx} results in degradation in the absolute value of U. The measured values for $|U|$ at 6 GHz for various devices are also shown in the figure. The extracted small-signal parameters are not necessarily constant across all these devices, but the changes are not very significant. We observe a 7 dB reduction in $|U|$ at 6 GHz for an R_{sx} increase from 114 Ω to 275 Ω.

The high frequency U and f_{max}, on the other hand, are independent of C_{gb}, but are influenced by the pole formed by C_{db} and R_{sx} (third term in the denominator of (7)). For the value of C_{db} in this study (37 fF), low values of R_{sx} (5 to 50 Ω) shift the pole $C_{db}R_{sx}$ to the left on the frequency axis thus resulting in a lower f_{max}. This is shown for $R_{sx} = 20\ \Omega$ in Fig. 13, which graphs the modeled $|U|$ as a function of frequency. The secondary pole also causes the U versus frequency to deviate from the -20 dB/dec slope at the high frequencies where f_{max} is extracted. Increasing R_{sx} shifts the pole to the right leading to a slightly higher f_{max}. This can also be seen in Fig. 13 for the case when $R_{sx} = 200\ \Omega$ (dotted line). In this case the U versus frequency follows the -20 dB/dec slope only at very high frequencies. At low frequencies (<20 GHz), U is negative. Fig. 13

$$U = \frac{g_m^2 r_o}{4R_g C_{gg}\omega^2 \left(C_{gg} + g_m r_o C_{gd} + \dfrac{r_o C_{gg}\omega^2 C_{db}^2 R_{sx}}{1+\omega^2 C_{db}^2 R_{sx}^2} - \dfrac{R_{sx} g_m r_o C_{gb} C_{db}}{R_g C_{gg}\left(1+\omega^2 (C_{gb}+C_{db}+C_{sb})^2 R_{sx}^2\right)}\right)} \tag{7}$$

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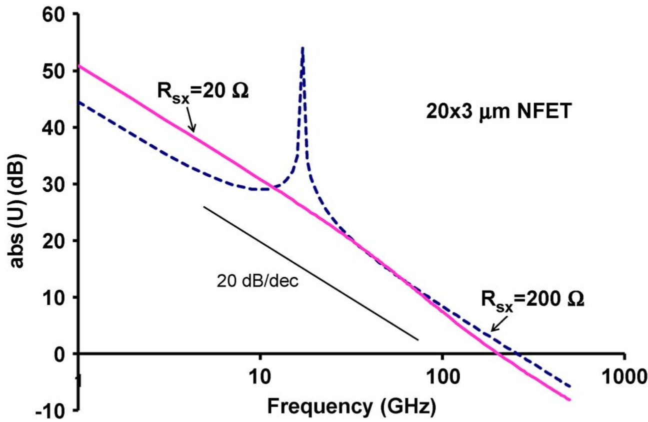

Fig. 13. Impact of substrate resistance on modeled unilateral gain and f_{max}. U vs. f deviates from the ideal -20 dB/dec slope.

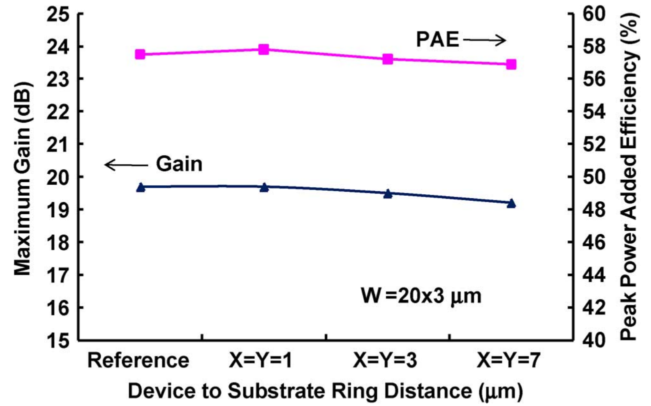

Fig. 15. Maximum power gain and peak power added efficiency of NFETs at 6 GHz as a function of device edge to substrate ring distance. Device biased at $V_{GS} = 0.8$ V and $V_{DS} = 1.1$ V.

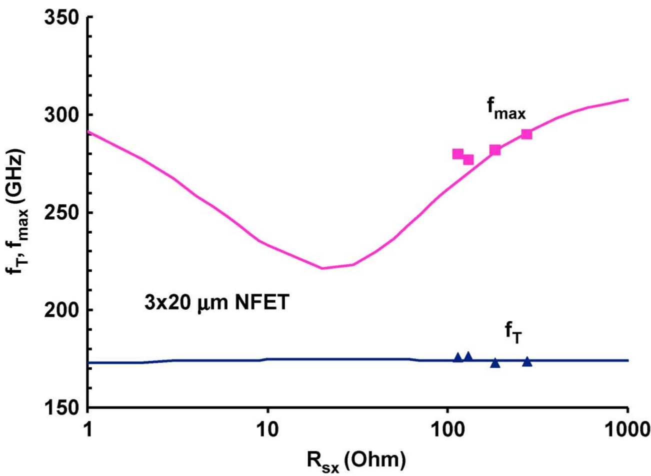

Fig. 14. Effect of increase in substrate resistance of NFET on the modeled f_T and f_{max}. Measured data shown as symbols.

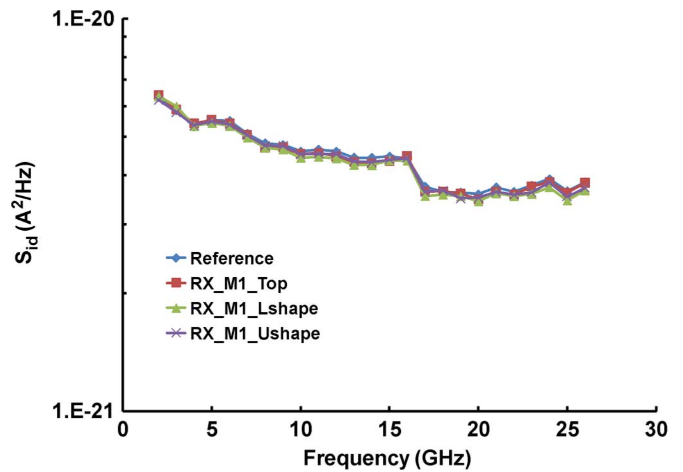

Fig. 16. Drain noise spectral density as a function of frequency for NFETs with different substrate contact ring shapes. $W = 60 \times 3\ \mu m$. $V_{GS} = 0.8$ V, $V_{DS} = 1.1$ V.

also illustrates the need for high frequency S-parameter measurements when extrapolating f_{max} of modern CMOS devices. Extrapolation from 50 GHz would result in erroneous and inflated values for f_{max}.

The dependence of f_{max} on substrate resistance is shown in Fig. 14 for a wide range of R_{sx}. Again, all other small-signal parameters are assumed to be constant and f_{max} is extracted from the U calculated using (7). f_{max} initially decreases with increasing R_{sx}. For $R_{sx} > 20\ \Omega$, f_{max} increases with R_{sx}. This is consistent with the discussion in the previous paragraph. The measured f_{max} data is also shown as symbols in the figure. The change in measured f_{max} is minimal because of the relatively small range in R_{sx} (114 Ω to 275 Ω). Fig. 14 also shows f_T as a function of R_{sx}. As was mentioned earlier, Y_{12} and Y_{21} are insensitive to R_{sx}. Thus, the current gain and f_T are constant with R_{sx}. This is consistent with the measured f_T data that is also shown in the figure.

IV. Circuit Design Implications

Power measurements were performed at 6 GHz by tuning the source and load impedances for maximum power gain. Fig. 15 shows the maximum power gain and the peak power added efficiency (PAE) as a function of distance between substrate contact ring and device edge. The increase in R_{sx} by 140% in going from the reference device to the $X = Y = 7\ \mu m$ device has negligible effect on the power gain and the peak PAE. This is because the maximum power gain is known to be correlated to the maximum stable gain (MSG) and PAE is strongly correlated to f_{max} [10]. Since MSG and f_{max} are relatively insensitive to the change in substrate resistance, it makes sense that the power characteristics are also insensitive to substrate resistance.

The drain noise spectral density as a function of frequency is shown in Fig. 16 for a $60 \times 3\ \mu m$ NFET with different substrate ring shapes. There is no discernible difference in the high frequency noise data with increasing substrate resistance (from 60Ω to 98Ω in this data set). This amount of variation in the substrate resistance is not significant enough to modulate the noise figure as the noise at the measured bias is dominated by other noise sources such as channel noise and gate induced noise.

The impact of substrate resistance on unilateral gain is an important consideration for designers. One popular design practice is to use feedback to cancel various loss paths in the device, thus

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achieving the highest gain in the circuit [11]. When $R_{sx}C_{gb}$ is significant, the unilateral gain becomes negative at the design frequency (<20 GHz), making the circuit unstable. A compensation network that cancels out the internal substrate resistance effect would then be required to stabilize the circuit. Hence, an accurate model for the substrate resistance and its impact on unilateral gain is essential for successful designs. A more comprehensive 5-resistor network substrate model is presented in [5].

The findings from this work can be used in making informed design trade-off decisions. For example, it has been shown that minimizing R_{sx} and parasitic C_{gb} capacitance is key to stabilizing U. One effective way to reduce R_{sx} is using a dedicated substrate contact ring for each device. A wider contact ring has been shown to reduce R_{sx} further, but may increase C_{gb}. C_{gb} can be reduced by optimizing the gate poly and metal wiring.

V. Conclusion

The impact of gate finger shape and substrate contact ring shape and position on the substrate resistance, f_T, and f_{max} of 45 nm CMOS devices is presented. The decrease in measured substrate resistance as a function of number of gate fingers follows previously published models. However, the effect of finger width on R_{sx} is much smaller than in the published models. An increase of 140% in the substrate resistance is observed when the distance between the device edge and the substrate ring is increased from 0.46 μm to 7 μm on all sides of the device. R_{sx} increases by 64% in going from a ring contact to a one sided contact. f_T, high frequency noise, power gain and power added efficiency are relatively insensitive to the moderate changes in substrate resistance in the range that has been studied in this work. A small signal model is created to accurately predict the impact of R_{sx} on Y-parameters and unilateral gain. The low to medium frequency unilateral gain has a strong dependence on C_{gb} and R_{sx}, while the high frequency U and f_{max} are modulated by C_{db} and R_{sx}.

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References

[1] N. Srirattana *et al.*, "A new analytical scalable substrate network model for RF MOSFETs," in *IEEE MTT-S Symp. Dig.*, Jun. 2004, pp. 699–702.

[2] I. M. Kang *et al.*, "Scalable model of substrate resistance components in RF MOSFETs with bar-type body contact considered layout dimensions," *IEEE Electron Device Lett.*, vol. 30, no. 4, pp. 404–406, Apr. 2009.

[3] R. Suravarapu and K. Mayaram, "A layout dependent and bias independent scalable substrate model for CMOS RF transistors," in *Proc. IEEE Radio and Wireless Conf.*, Aug. 2002, pp. 217–220.

[4] H. Hjelmgren and A. Litwin, "Small-signal substrate resistance effect in RF CMOS identified through device simulations," *IEEE Trans. Electron Devices*, vol. 48, no. 2, pp. 397–399, Feb. 2001.

[5] J. Wang *et al.*, "RF modeling of 45 nm low-power CMOS technology," in *2009 Workshop on Compact Modeling (WCM)*.

[6] D. Lovelace *et al.*, "Extracting small-signal model parameters of silicon MOSFET transistors," in *Int. Microwave Symp. Dig.*, 1994, pp. 865–868.

[7] Y. Cheng *et al.*, "MOSFET modeling for RF IC design," *IEEE Trans. Electron Devices*, vol. 52, no. 7, pp. 1286–1303, Jul. 2005.

[8] C. Doan *et al.*, "Millimeter-wave CMOS design," *IEEE J. Solid-State Circuits*, vol. 40, no. 1, pp. 144–155, Jan. 2005.

[9] B. Razavi *et al.*, "Impact of distributed gate resistance on the performance of MOS devices," *IEEE Trans. Circuits Syst.*, vol. 41, no. 11, pp. 750–754, Nov. 1994.

[10] J. Scholvin *et al.*, "Fundamental power and frequency limits of deeply scaled CMOS for RF power applications," in *IEEE IEDM Tech. Dig.*, Dec. 2006, pp. 217–220.

[11] G. D. Vendelin *et al.*, "Applying f_{max}, f_t and f_{mag} for microwave transistor designs at microwave and millimeter-wave frequencies," *IEEE Microwave Mag.*, Feb. 2007.

[12] U. Gogineni *et al.*, "Effect of substrate contact shape and placement on RF characteristics of 45 nm low power CMOS devices," in *Proc. IEEE Radio Frequency Integrated Circuits (RFIC) Symp.*, 2009, pp. 163–166.

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Basanth Jagannathan , photograph and biography not available at the time of publication.

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