60 nm Self-Aligned-Gate InGaAs HEMTs
with Record High-Frequency Characteristics

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Abstract

We have developed a new self-aligned gate technology for InGaAs High Electron Mobility Transistors with non-alloyed Mo-based ohmic contacts and a very low parasitic capacitance gate design. The new process delivers a contact resistance of 7 Ohm-μm and a source resistance of 147 Ohm-μm. The non-alloyed Mo-based ohmic contacts show excellent thermal stability up to 600 °C. Using this technology, we have demonstrated a 60 nm gate length self-aligned InGaAs HEMT with g_m = 2.1 mS/μm at V_{DS} = 0.5 V, and f_T = 580 GHz and f_{max} = 675 GHz at V_{DS} = 0.6 V. These are all record or near record values for this gate length.

Introduction

Reducing source and drain parasitic resistance is essential to boosting the frequency response of III-V High Electron Mobility Transistors (HEMTs) [1-2]. A key to accomplishing this is to shrink the source-gate contact separation, L_{GS}. State-of-the-art III-V HEMTs typically feature L_{GS} values in the range of 0.5 to 1 μm which result in source resistance (R_s) in InGaAs HEMTs of around 200 ohm-μm. The lowest source resistance in InGaAs HEMTs has been reported by Matsuzaki [3] as R_s = 100 Ohm-μm in non-self-aligned devices with a gate-source separation, L_{GS} = 100 nm. To improve beyond this, a self-aligned gate design is essential.

Several self-alignment schemes for InGaAs HEMTs have been demonstrated in the literature [4-5]. In one approach, after T-shape gate formation, ohmic metal is deposited using the gate as a mask. This results in L_{GS} of about half the gate head size [4]. In a separate approach demonstrated by our group, W was used as non-alloyed ohmic contacts with the gate nested inside an opening in a self aligned way. Through this technology 90 nm gate length InGaAs HEMTs were demonstrated with L_{GS} = 60 nm [5]. This technology featured a simple lift-off gate with high parasitic capacitance. As a result, the frequency response of the fabricated transistors was unremarkable.

In this work, we demonstrate a new self-aligned gate technology with non-alloyed Mo-based ohmic contacts and a very low parasitic capacitance gate design. The new process delivers very low values of contact resistance and source resistance and record high-frequency characteristics. The proposed device architecture allows for the incorporation of a high-K gate dielectric in the gate stack to achieve MOS type devices.

Process Technology

Fig. 1 shows a simplified process sequence on a HEMT heterostructure. Device fabrication starts with blank 20 nm Mo e-beam evaporation after removal of the native oxide in an HCl based solution. This Mo layer serves as source and drain non-alloyed ohmic contact. The process follows with mesa isolation, Ti/Mo ohmic pad, SiO_2 sacrificial layer deposition and Ti/Au contact pad formation.
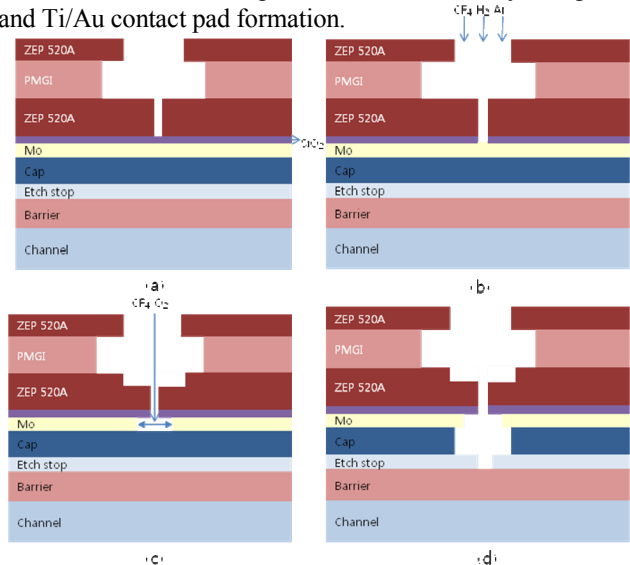

Fig. 1 Process flow for SAG structure: a) double exposure and double development e-beam process, b) $CF_4/H_2/Ar$ based plasma etching to create opening in SiO_2, c) CF_4/O_2 plasma to isotropically etch Mo, and d) two-step gate recess process using Citric acid and Ar plasma to expose barrier.

The first step in T-shape gate formation is a double-exposure double-development gate resist process (Fig. 1a). This is followed by etching of an opening in the SiO_2 by anisotropic $CF_4/H_2/Ar$ based plasma (Fig. 1b). We then carry out isotropic etching of the Mo layer by CF_4/O_2 plasma (Fig. 1c) to place the edge of the Mo contacts at a controlled distance away from the edges of the gate (set by the edge of the SiO_2 sacrificial layer). Following this, we perform a two-step gate recess process which consists of cap removal by a citric acid based solution followed by Ar based plasma for the InP etch stop (Fig. 1d). This results in a slight undercut of the Mo contact layer. We then evaporate and lift off a Pt/Ti/Pt/Au gate stack followed by a thermal step to drive the Pt into the InAlAs barrier and achieve an effective barrier thickness of t_{ins} = 5 nm.

Devices with L_g in the range of 50 to 150 nm were fabricated. **Fig. 2** shows a schematic cross section of the final device. **Fig. 3** shows STEM images of a fabricated L_g = 60 nm device. The gate to source contact separation (L_{GS}) and side-recess-length (L_{side}) were 100 nm and 200 nm, respectively.
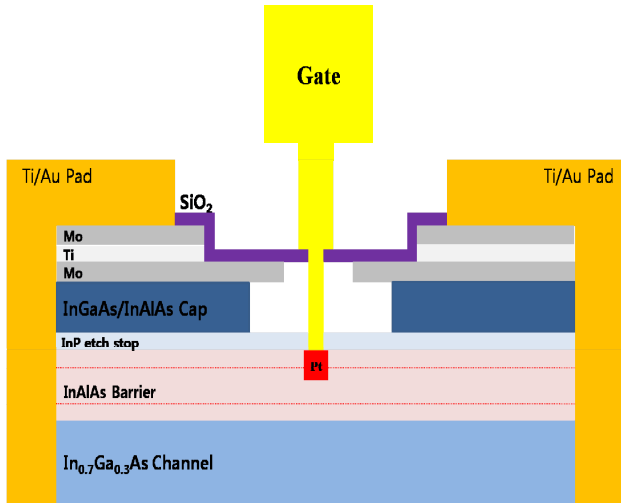
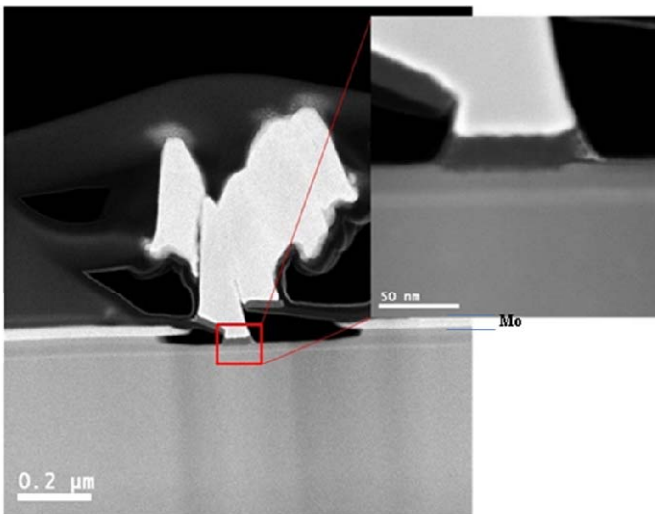**Fig. 2** Final cross section of Mo-based SAG HEMT.

Fig. 3 Cross-section STEM images of Mo-based SAG HEMT with L_g = 60 nm with 100 nm gate-source contact separation and L_{side}=200 nm. The barrier thickness, t_{ins}, is estimated to be 5 nm.

For our first device demonstration, we used a metamorphic InAlAs/InGaAs heterostructure grown on a GaAs substrate with dual Si-doping layers which are located in the upper InAlAs barrier to enhance electron tunneling at the contacts. The channel is made out of $In_{0.7}Ga_{0.3}As$ and is 10 nm thick.

DC and Microwave Characteristics

Fig. 4 shows resistance measurements in TLM structures. We compare our approach using Mo blanket deposition and dry etching with a scheme based on standard Mo evaporation plus lift-off. Also, as reference, we add earlier self-aligned W-based ohmic results [5]. The new Mo-based approach yields an R_c of 7 Ohm-μm. This is nearly an order of magnitude improvement over previous self-aligned ohmic-contact technology [5] and a record value among non-alloyed ohmic contacts to InGaAs FETs. Also, blanket Mo deposition yields

better results than a Mo lift-off process due to the absence of residual photoresist at the metal-semiconductor interface. Our Mo contact technology is also thermally stable up to 600C.

Fig. 5 shows output characteristics of a typical Mo-based SAG HEMT with L_g = 50 nm. The device exhibits excellent saturating characteristics with low R_{ON} and a high current of 0.68 mA/μm at V_{DS} = 0.5 and V_{GS}-V_T = 0.33 V (2/3 of V_{DS}).

Fig. 6 shows typical current and transconductance characteristics vs. V_{GS} at V_{DS} = 0.5 V. This device exhibits over 2.2 mS/μm of maximum transconductance, a record value for L_g = 50 nm HEMTs at V_{DS} = 0.5 V. This result arises from the reduced source resistance of the SAG structure.

Fig. 7 shows subthreshold characteristics for V_{DS} = 50 mV and 0.5 V. The subthreshold swing S = 120 mV/dec and DIBL = 160 mV/V that we obtain are not as good as earlier demonstrations from our group. This is the consequence of slightly higher gate leakage current. An optimized heterostructure and Pt sinking process should correct this.
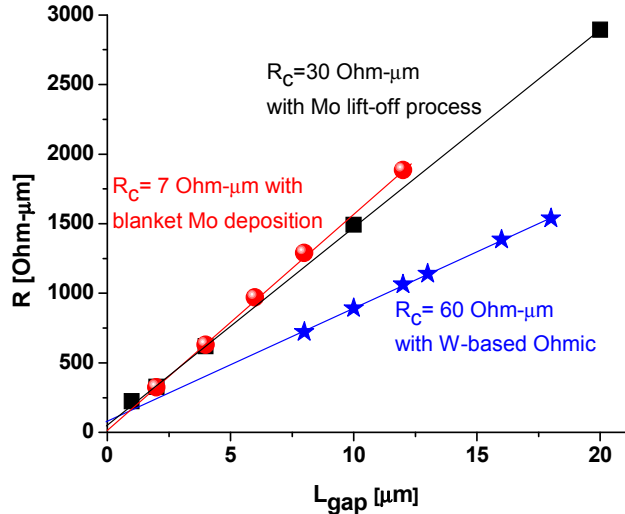

Fig. 4 TLM measurements for three different contact schemes. The gap length in each contact was measured by SEM.
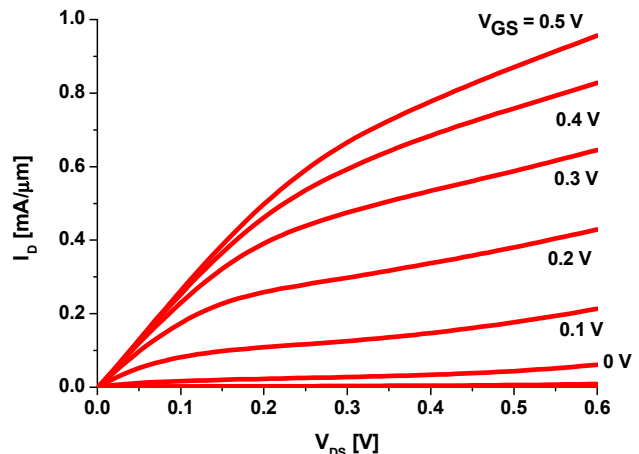

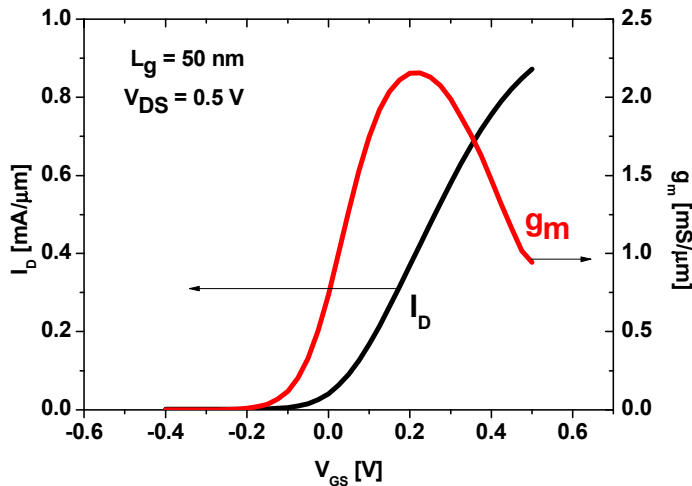**Fig. 5** Output characteristics of Mo-based SAG HEMT with L_g = 50 nm.

Fig. 6 Transfer and transconductance characteristics of 50 nm SAG HEMT.

In order to understand the source resistance characteristics of SAG HEMT fabricated by this process, we have directly measured the effective source resistance, R_s^*, by means of the gate current injection technique [6], as shown in **Fig. 8**. The source resistance R_s can be extracted by linear extrapolation of R_S^* to zero L_g [7]. The extracted R_s is 147 Ohm-μm. This value is around 30% lower than our previous report on self-aligned W-based devices [5].

Fig. 9 shows the maximum transconductance (g_m) as a function of L_g for our devices and state-of-the-art non-self-aligned InAs PHEMTs [8] as well as earlier W-based SAG HEMTs [5] at $V_{DS} = 0.5$ V. All these devices have about the same $t_{ins} = 5$ nm. Our fabricated Mo-based SAG devices show improved transconductance and excellent scalability down to $L_g = 50$ nm. In particularly, the $L_g = 100$ nm device exhibits a g_m of nearly 2 mS/μm at $V_{DS} = 0.5$ V.
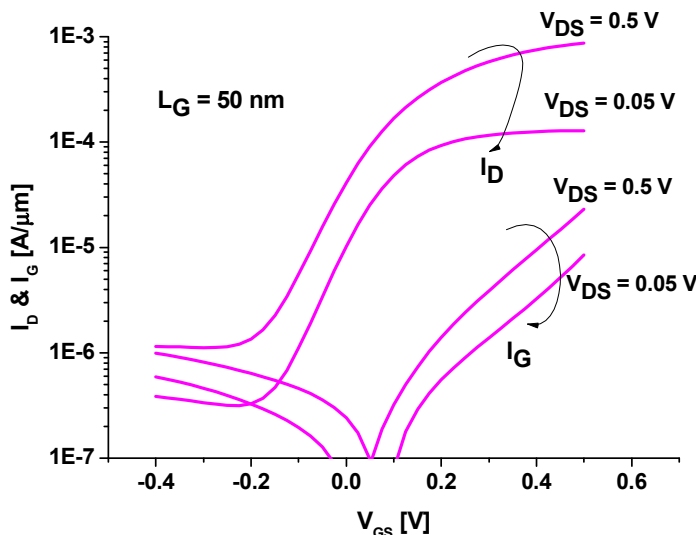

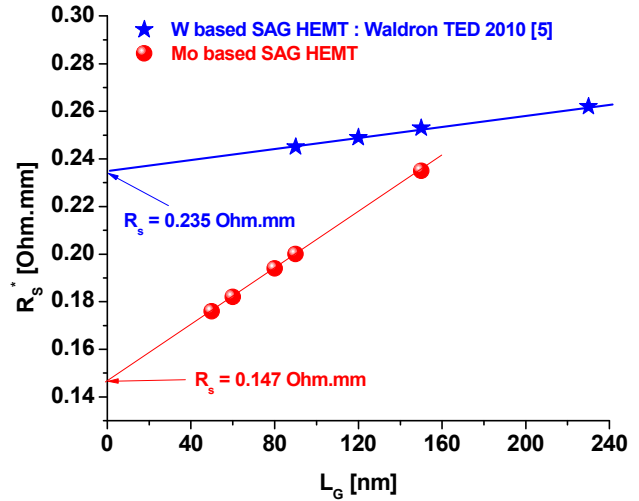**Fig. 7** Subthreshold and I_G characteristics of 50 nm Mo-based SAG HEMT.

Fig. 8 Effective source resistance R_s^* as a function of L_g obtained from the gate current injection technique. The present devices are compared with those from an earlier self-aligned technique [5]. The actual source resistance is the extrapolation of R_s^* to $L_g = 0$.

Microwave performance was characterized from 0.5 to 40 GHz. On-wafer open and short patterns were used to subtract pad capacitances and inductances from the measured device S-parameters. **Fig. 10** plots H_{21}, Unilateral gain (U_g), MSG and K-factor for a $L_g = 60$ nm device at the peak g_m bias condition at $V_{DS} = 0.6$ V ($L_g = 60$ nm is the smallest microwave device available).
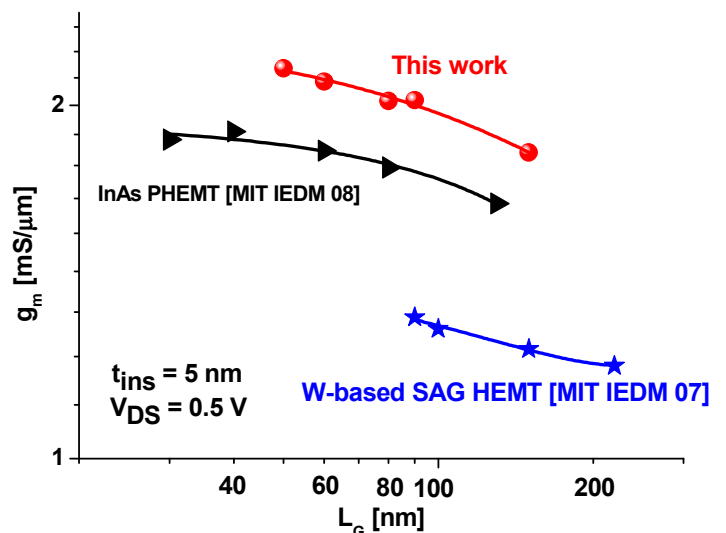

Fig. 9 Maximum transconductance (g_m) as a function of gate length for Mo-based SAG HEMTs and state-of-the-art non-self-aligned InAs PHEMTs [8] as well as W-based SAG HEMTs [5]. All devices have t_{ins}=5 nm.
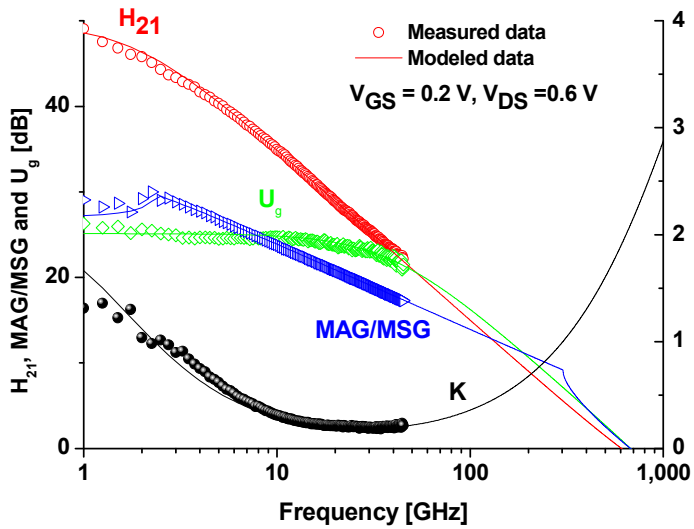
Fig. 10 Measured and modeled microwave characteristics of L_g=60 nm Mo-based SAG HEMT at V_{DS} = 0.6 V.

Excellent values of f_T = 580 GHz and f_{max} = 675 GHz have been obtained. The measured characteristics are well described by a simple lumped model constructed in ADS that predicts f_T = 600 GHz and f_{max} = 675 GHz. In addition, we measured this device at the same bias point in a separate system up to 67 GHz. We found f_T = 590 GHz and f_{max} = 680 GHz giving credibility to our measurements

Fig. 11 shows f_T as a function of L_g for sub-100 nm InGaAs and InAs HEMTs. The obtained f_T value in our devices is the highest ever reported in a HEMT above L_g = 50 nm and bodes well for the future scalability of this device design. **Fig. 12** shows f_{avg} = $(f_T \times f_{max})^{0.5}$ as a function of L_g for our SAG HEMTs as well as reports from the literature. It is clear that our new SAG technology attains record well-balanced high frequency characteristics.
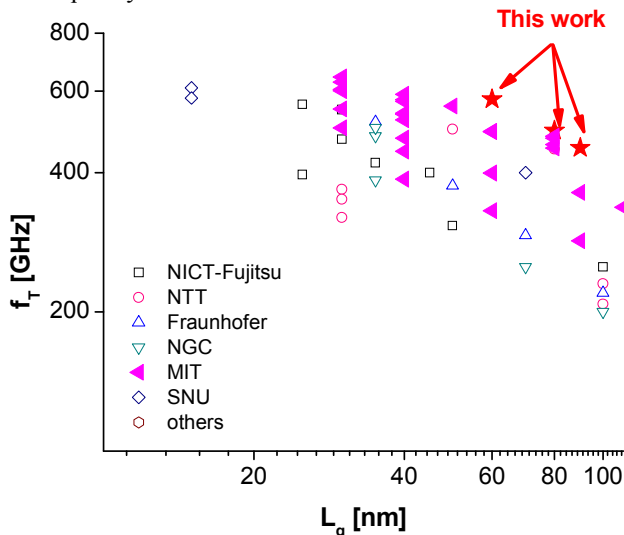

Fig. 11 f_T as a function of L_g for reported InGaAs and InAs HEMTs in the literature, including Mo-based SAG HEMTs in this work.
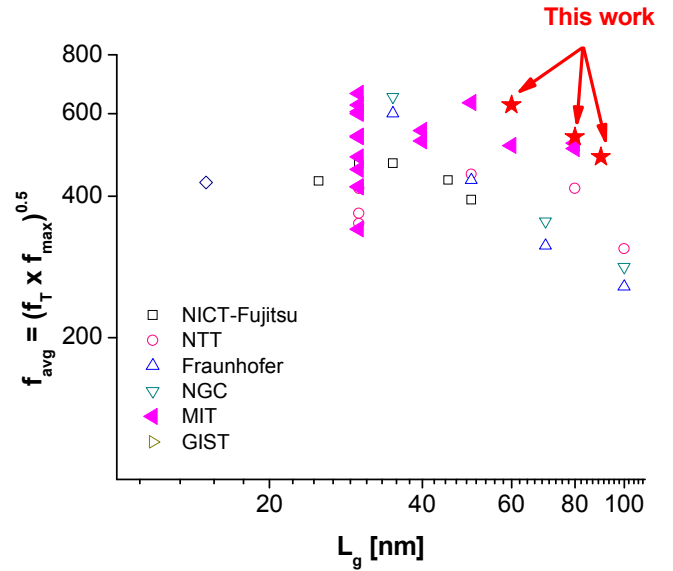

Fig. 12 f_{avg} = $(f_T \times f_{max})^{0.5}$ as a function of L_g for reported InGaAs and InAs HEMTs in the literature, including Mo-based SAG HEMTs from this work.

Conclusions

We have demonstrated a new Mo-based SAG HEMT technology that delivers outstanding source resistance and high frequency characteristics. In particular, L_g = 60 nm devices exhibit g_m = 2.1 mS/µm at V_{DS} = 0.5 V, f_T = 580 GHz and f_{max} = 675 GHz at V_{DS} = 0.6 V. Mo-based SAG HEMTs shows extremely low contact resistance of 7 ohm-µm and a source resistance of 147 ohm-µm. This is the first demonstration of a self-aligned gate InGaAs HEMT technology with state-of-the-art frequency response. This result strongly suggests a path towards obtaining Field-Effect Transistors with f_T and f_{max} both surpassing 1 THz.

References

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