50-nm E-mode $In_{0.7}Ga_{0.3}As$ PHEMTs on 100-mm InP substrate with f_{max} > 1 THz

Dae-Hyun Kim, *Jesús A. del Alamo, Peter Chen, Wonill Ha, Miguel Urteaga and Berinder Brar

Teledyne Scientific Company (TSC), Thousand Oaks, CA 91360, USA, E-mail: dkim@teledyne.com

*Massachusetts Institute of Technology (MIT), Cambridge, MA 02139, U.S.A

Abstract

We have demonstrated 50-nm enhancement-mode (E-mode) $In_{0.7}Ga_{0.3}As$ PHEMTs with f_{max} in excess of 1 THz. The devices feature a Pt gate sinking process to effectively thin down the $In_{0.52}Al_{0.48}As$ barrier layer, together with a two-step recess process. The fabricated device with L_g = 50-nm exhibits V_T = 0.1 V, $g_{m,max}$ = 1.75 mS/µm, f_T = 465 GHz and f_{max} = 1.06 THz at a moderate value of V_{DS} = 0.75 V. In addition, we have physically modeled the abnormal peaky behavior in Mason's unilateral gain (U_g) at high values of V_{DS}. A revised small signal model that includes a shunting $R_{gd\text{-}NDR}$ with negative value successfully describes the behavior of the device from 1 to 67 GHz.

Introduction

The last few years have witnessed an explosion of interest in devices suitable for ultra high frequency applications, such as in the Tera-Hz regime. To accomplish this, a device technology must rely on boosting high frequency operation by reducing gate length (L_g) to sub-50 nm, improving carrier transport in the channel, improving electrostatic integrity and minimizing resistance and capacitance parasitics [1-2].

An additional feature that is highly desirable in future THz circuits is a positive V_T. Achieving E-mode PHEMTs is rather difficult as it demands tight control of t_{ins}, especially as L_g approaches to sub-50 nm regime. In this work, we use Pt gate sinking to shift V_T and to thin down the barrier [3]. Pt gate sinking in devices with high InAs compositions in the channel have been demonstrated before [4-5]. What is important in this work is a well balanced device design that pays close attention to short-channel effects and that leads to exceptional high frequency characteristics. In this work, we demonstrate for the first time enhancement-mode $In_{0.7}Ga_{0.3}As$ PHEMTs with f_{max} in excess of 1 THz at a moderate value of V_{DS} = 0.75 V.

Process Technology

Fig. 1 shows a cross section of the device structure. The device architecture brings together unique features designed to minimize parasitics and mitigate short-channel effects, as in [5]. The epitaxial layer structure is similar to [6]. It features a 10-nm thick $In_{0.7}Ga_{0.3}As$ channel. After a two-step recess process that exposes an InAlAs barrier, a Pt/Ti/Pt/Au (3/30/10/350 nm) gate was created. Subsequently, the devices were annealed at 250 °C for 2 minutes to drive the Pt into the InAlAs barrier. In this way, a gate-to-channel distance (t_{ins}) of about 4-nm was achieved with side-recess spacing (L_{side}) of 150-nm. A range of gate length (L_g) in this work was from 200-nm to 50-nm.

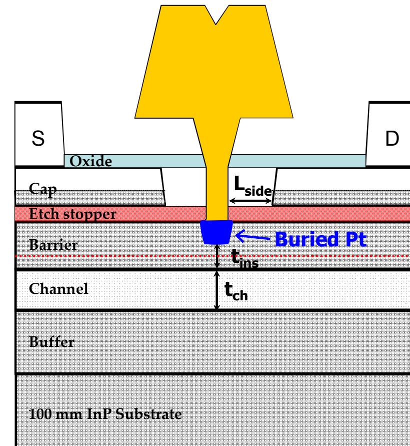


Fig. 1 Schematic of $In_{0.7}Ga_{0.3}As$ PHEMT on a 100-nm InP substrate. It features t_{ch} = 10 nm and t_{ins} = ~ 4 nm. The devices were fabricated with Pt gate sinking. The smallest L_g was 50-nm, and L_{side} was 150-nm.

DC & Microwave Characteristics

Fig. 2 shows typical DC output characteristics of $In_{0.7}Ga_{0.3}As$ PHEMTs with various values of L_g. Well-behaved drain current saturation is observed with excellent pinch-off characteristics up to V_{DS} = 0.9 V for all gate lengths. Typical ON-resistance (R_{ON}) is about 0.4 Ω-mm for L_g = 50 nm devices. As in the author's previous work on $In_{0.7}Ga_{0.3}As$ PHEMTs [5], the devices in this work also show improved current driving capability as L_g scales down to 50 nm.

Fig. 3 plots the transconductance (g_m) characteristics of the same devices at V_{DS} = 0.5 V. The devices exhibit a continuously increasing g_m, as L_g scales down to 50-nm. Particularly, the device with L_g = 50 nm shows $g_{m,max}$ = 1.7 S/mm. These outstanding characteristics arise from improved charge control behavior through the combination of the two-step recess plus buried Pt gate sinking technology.

Fig. 4 plots the sub-threshold and transfer characteristics of all the 50-nm $In_{0.7}Ga_{0.3}As$ PHEMTs on a 100-mm wafer. The devices offer a true e-mode operation (V_T = 0.1 V, defined with a criteria of I_D = 1 mA/mm) with excellent V_T uniformity (ΔV_T = 28 mV) across the wafer. Besides, the devices show very sharp subthreshold characteristics, as assessed by a subthreshold-swing = 80 mV/dec and DIBL = 80 mV/V, which are close to those of advanced InGaAs PHEMTs [6]. Besides, these devices do not show excessive gate leakage current. The typical gate turn-ON voltage ($V_{g,ON}$) was greater than 0.5 V with a criteria of I_g = 1 mA/mm, which is highly attractive for e-mode operation.

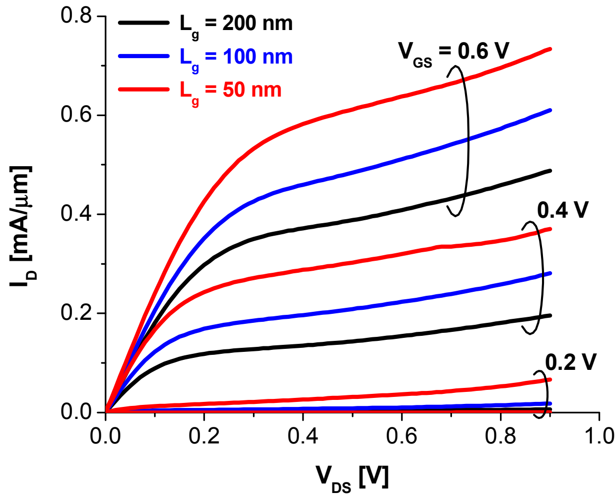


Fig. 2 Output characteristics of $In_{0.7}Ga_{0.3}As$ PHEMTs with various gate lengths (L_g = 200, 100 and 50 nm).

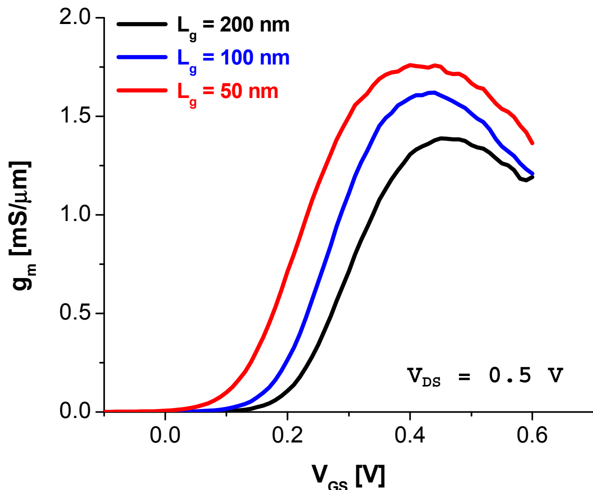


Fig. 3 Transconductance (g_m) characteristics for $In_{0.7}Ga_{0.3}As$ PHEMTs with various gate lengths at V_{DS} = 0.5 V.

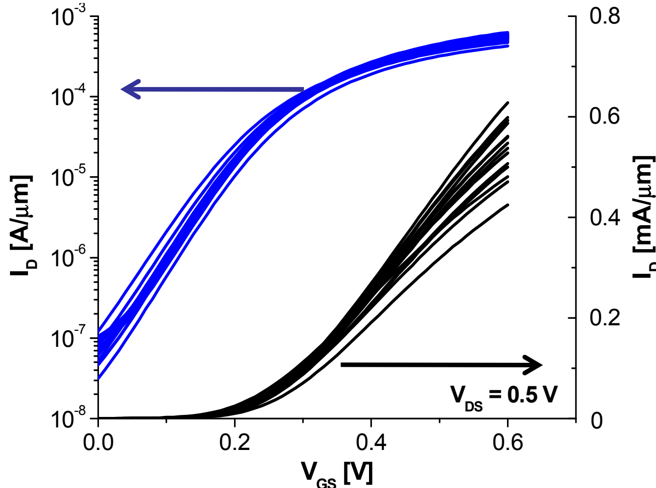
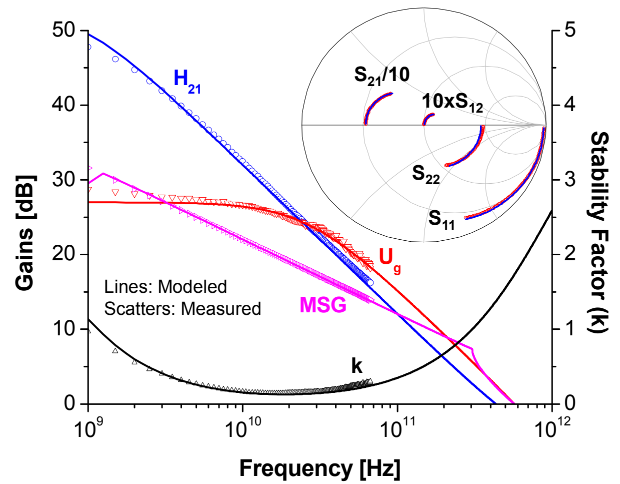
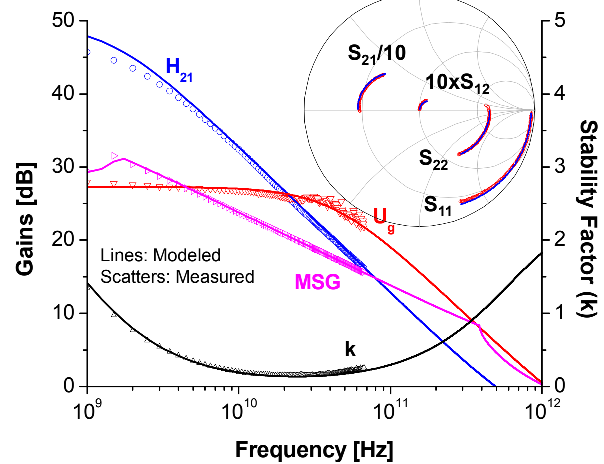


Fig. 4 Subthreshold and transfer characteristics of 50-nm $In_{0.7}Ga_{0.3}As$ PHEMTs on a 100-mm InP substrate at V_{DS} = 0.5 V.

Microwave performance was characterized using an Agilent precision-network-analyzer (PNA) with a standard Line-Reflection-Reflection-Match (LRRM) calibration from 1 GHz to 67 GHz. On-wafer open and short structures were used to de-embed pad capacitances and inductances. **Fig. 5** plots measured (symbols) and small-signal modeled (lines) short-circuit current gain (H_{21}), maximum stable gain (MSG), Mason's unilateral gain (U_g) and stability factor (k) for the 50-nm device at (a) V_{GS} = 0.5 V and V_{DS} = 0.5 V, and (b) V_{GS} = 0.5 V and V_{DS} = 0.75 V. The transistor f_T was determined by extrapolating $|H_{21}|$ with a slope of -20 dB/decade using a least-squares fit. The 50-nm PHEMT in this work exhibits a high value of f_T = 465 GHz at V_{DS} = 0.75 V, and over 400 GHz at V_{DS} = 0.5 V. More significantly, the device displays an extremely high value of maximum oscillation frequency (f_{max}). At V_{DS} = 0.75 V, f_{max} of 1.06 THz is obtained from extrapolation using the measured U_g.



(a) V_{GS} = 0.5 V and V_{DS} = 0.5 V



(b) V_{GS} = 0.5 V and V_{DS} = 0.75 V

Fig. 5 RF gains (H_{21}, U_g and MSG), stability factor (k), and S-parameters (inset) for 50-nm $In_{0.7}Ga_{0.3}As$ PHEMTs with W_g = 2 x 20 μm vs. frequency, together with predictions from the small-signal model. Inset of both figures is the comparison of measured and modeled S-parameters.

To accurately extract the value of f_{max}, we carried out small-signal modeling at different bias conditions, as recently proposed [7]. The estimated f_{max} is sensitive to the values of small-signal parameters, such as R_g, R_s and R_d. To make the small-signal modeling process robust, we carefully extracted all the parasitic resistances [7], used them to derive all the intrinsic parameters, and finally verified the accuracy of the small-signal model at different bias conditions across multiple devices. As shown in **Fig. 5**, our models predict all the S-parameters, RF gains and k consistently at both bias conditions. From the model, the 50-nm device yields f_{max} = 1.08 THz at V_{DS} = 0.75 V, which is very similar to the value from the measured U_g. This is the highest f_{max} ever reported in any FET on any material system with E-mode operation.

Increasing V_{DS} beyond 0.75 V is likely to yield even better f_{max}. However, it is very difficult to extract it from either the experimental measurement of U_g, or from the small-signal model. This is because U_g is apt to show sharp peaky behavior at intermediate frequencies as V_{DS} increases. **Fig. 6** shows measured and modeled RF gains and k at V_{DS} = 0.9 V. Indeed, U_g exhibits an anomalously increasing behavior with frequency, and the modeled U_g fails to describe it. For a given device, we have verified that this behavior is reproducible across different measurement systems. Such behavior has also been observed in high frequency devices by another group [1].

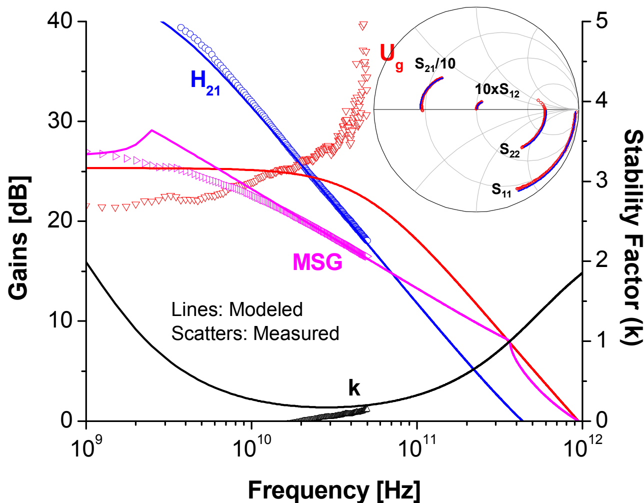


Fig. 6 RF gains (H_{21}, U_g and MSG), k-factor, and S-parameters (inset) for 50-nm $In_{0.7}Ga_{0.3}As$ PHEMTs vs. frequency at V_{GS} = 0.5 V and V_{DS} = 0.9 V, together with model predictions.

Advanced Small-Signal Model

In trying to understand the abnormal behavior in U_g, we found that U_g is actually negative before the peak occurs. From the definition of Mason's unilateral gain, U_g takes the sign of its denominator. The expression of U_g is:

$$U_g = \frac{|Y_{21} - Y_{12}|^2}{Re(Y_{11}) \bullet Re(Y_{22}) - Re(Y_{12}) \bullet Re(Y_{21})} \quad (1)$$

Fig. 7 shows the denominator of the experimental U_g for the 50-nm device at V_{DS} = 0.5 V and 0.9 V. Clearly, a negative value of U_g arises from its denominator and this occurs at high values of V_{DS}. Furthermore, the frequency at zero-crossing in Den(U_g) is responsible for the abnormal peaky behavior in U_g. Now, the question arises: what is the origin of this? We found that a '*Negative-Differential-Resistance*' (NDR) effect between gate and drain at high values of V_{DS} is responsible for the negative U_g.

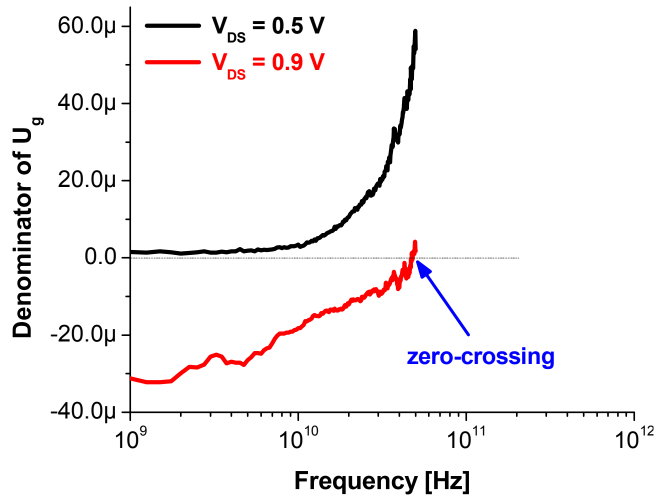


Fig. 7 Denominator of U_g for 50-nm device as a function of frequency at V_{DS} = 0.5 V and 0.9 V.

A possible mechanism for this is shown in **Fig. 8**. As V_{DS} increases, high-field effects at the drain-side of the gate, such as hot electron production, become more prevalent. These hot electrons are capable of causing NDR effects between the gate and drain [8]. **Fig. 9** shows the measured I_G as a function of V_{DS} for 50-nm devices with different values of V_{GS}. As V_{DS} increases, I_G initially decreases (due to the reduction and eventual change of sign of the gate-drain gate leakage current), and then increases at V_{DS} = 0.5 V for V_{GS} > 0.4 V due to real-space transfer of hot electrons from the channel into the gate [7]. This is a region of negative differential resistance in I_G.

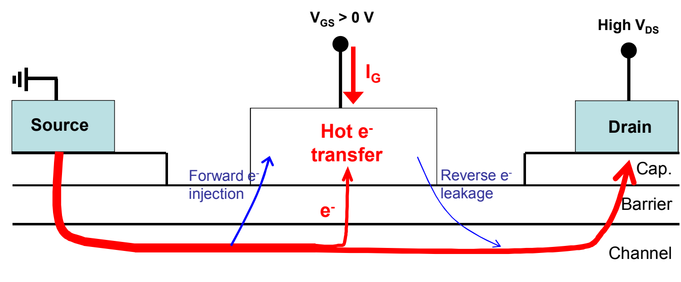


Fig. 8 Physical origin of NDR effect between gate and drain. As V_{DS} increases, there is real-space transfer of hot electrons from the chanbnel to the gate.

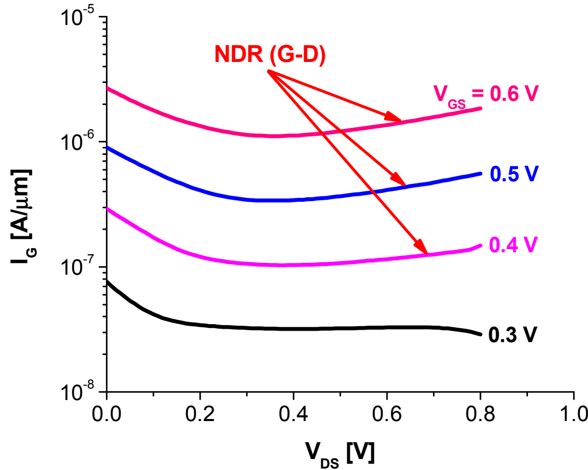


Fig. 9 I_G vs. V_{DS} for 50-nm device at various values of V_{GS}.

From the RF point of view, this phenomenon can be modeled by adding a shunt negative resistance ($R_{gd\text{-}NDR}$) between gate and drain, as shown in **Fig. 10**. From this model, the denominator of U_g is approximated as $g_0/R_{gs} + g_m/R_{gd,total}$. If R_{gd_total} has a negative sign and its absolute value is smaller than g_mR_{gs}/g_0, then the denominator of U_g becomes negative. We have used this revised small-signal model to estimate f_{max}. The value of R_{gd_total} can be obtained from $Re(Y_{12}) = -R_{gd_total}$ in the equivalent circuit model. **Fig. 11** plots measured and modeled RF gains and k at V_{DS} = 0.9 V with the addition of $R_{gd\text{-}NDR}$. Our model predicts the experimental gain characteristics and the k-factor very nicely, including the sharp peak in U_g. Using the model, we extrapolated a value of f_{max} = 920 GHz at V_{DS} = 0.9 V, which is a bit lower than that at V_{DS} = 0.75 V. This is likely due to the drop in f_T that results from the increase in the drain delay as V_{DS} increases.

To see how our devices stand out in comparison to other reports, **Fig. 12** plots f_{max} as a function of f_T for our 50-nm device with V_{DS} = 0.75 V, as well as other reports including III-V HBTs and III-V HEMTs. Clearly, the device in this work exhibits a record value of f_{max} for e-mode operation.

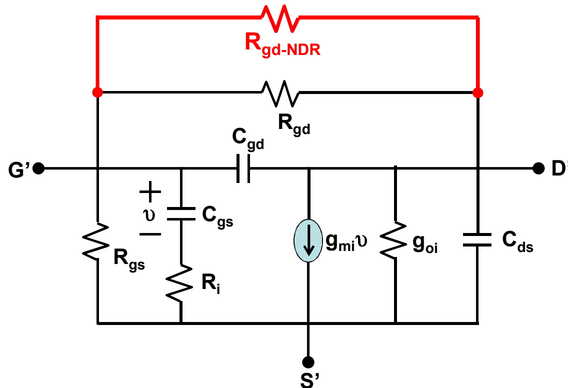


Fig. 10 Modified small-signal equivalent circuit of the intrinsic device with the shunt addition of R_{gd_NDR} between intrinsic gate and drain. $R_{gd_total}^{-1}$ is the sum of $R_{gd_NDR}^{-1}$ and R_{gd}^{-1}, and $Re(Y_{12})$ is - R_{gd_total}.

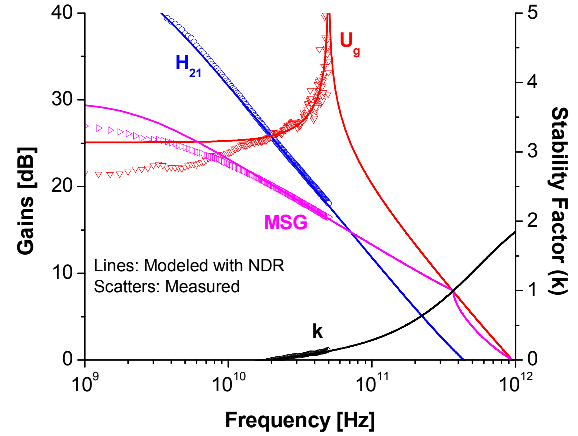


Fig. 11 Data and modified model predictions for RF gains and k-factor at V_{GS} = 0.5 V and V_{DS} = 0.9 V. Our model predicts the abnormal behavior in U_g nicely, as well as the k-factor.

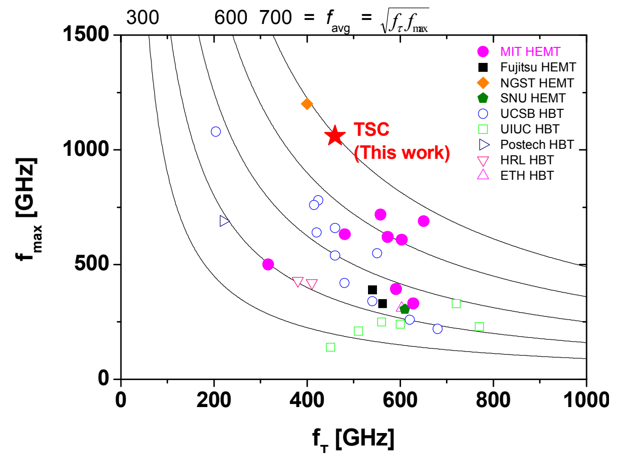


Fig. 12 f_{max} as a function of f_T for 50 nm $In_{0.7}Ga_{0.3}As$ PHEMTs in this work, as well as other reports on III-V HEMTs and HBTs. For all the data f_T and f_{max} are measured at the same bias condition.

Conclusions

In summary, we have demonstrated for the first time 50-nm E-mode InGaAs PHEMTs on a 100-mm InP substrate with f_{max} > 1 THz. We have physically modeled the abnormal peaky behavior in U_g at high values of V_{DS}, and successfully revised the small signal model by adding $R_{gd\text{-}NDR}$ with negative value. Without doing this, any attempt on f_{max} extrapolation at high values of V_{DS} could result in an over-estimation on its value.

References

[1] R. Lai *et al.*, *IEDM*, p. 609, 2007.
[2] D.-H. Kim *et al.*, *IEEE EDL*, p. 830, 2008.
[3] Mahajan *et al.*, *IEEE EDL*, p. 284, 1997.
[4] T.-W. Kim *et al.*, *IEEE TED*, p. 1577, 2008.
[5] D.-H. Kim *et al.*., *IEDM*, p. 719 , 2008.
[6] D.-H. Kim *et al.*, *IEEE TED*, p. 2606 , 2007.
[7] D.-H. Kim *et al.*, *DRC*, late news paper, 2010.
[8] S.J. Kim *et al.*, *JJAP*, p. 6152 , 2000.

Acknowledgements

This work was sponsored in part by DARPA under a SPAWAR System Center, San Diego Contract Number N660001-06-C-2025. The authors thank Nidhi and U. Mishra for the help in doing S-parameter measurements, and A. Lui with IQE for the growth of the epi wafer.