RF Power Degradation of GaN High Electron Mobility Transistors

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Abstract

We have developed a versatile methodology to systematically investigate the RF reliability of GaN High-Electron Mobility Transistors. Our technique utilizes RF and DC figures of merit to diagnose the degradation of RF stressed devices in real time. We have found that there is good correlation between selected RF and DC figures of merit. However, compared with DC stress, RF stress at the same bias point is found to be more severe and to introduce new degradation modes. At high power level, RF stress induces a prominent trapping-related increase in the source resistance most likely as a result of the creation of new traps. This is in contrast with drain degradation that often occurs under similar DC conditions. Our findings cast a doubt over the ability of DC life test in evaluating reliability under RF power conditions.

Introduction

GaN high electron mobility transistors (HEMTs) have shown extraordinary RF power performance. Although there have been extensive studies on DC reliability [1-2], much less attention has been given to the RF reliability of this technology [3-5]. Today, detailed understanding of RF degradation mechanisms is still lacking. To fill this void, we have developed a methodology to systematically investigate RF reliability and to compare it with DC reliability. A key goal is to evaluate the ability of DC life tests to correctly assess RF reliability. A second goal is to investigate possible new degradation mechanisms under RF stress.

We have found that there is good correlation between the degradation of selected DC and RF figures of merit. However, RF stress degrades the device much more severely than DC stress at the same bias point. Also, the degradation increases with increasing RF power level. The signature of degradation is also different. Unlike DC stress, RF stress induces a prominent increase in source resistance suggesting that a new mechanism is in action. We show that this degradation arises from the high power condition that the device attains during large signal RF swing. Our research suggests that DC life tests are likely to underestimate RF reliability.

Stress Test Methodology

Our set up consists of a four-channel Accel-RF life-test system AARTS RF10000-4/S equipped with a switching matrix that allows us to temporarily stop RF stressing and characterize the device through an external semiconductor parameter analyzer [2] (**Fig. 1**). The entire system is controlled through the Accel-RF system computer.

A flow chart of a typical RF stress test is shown in **Fig. 2**. It consists of two nested loops. In the inner loop we perform RF/DC stress under a variety of conditions with the device at a base plate temperature T_{stress}. This loop also includes short device characterization where a few DC and RF parameters are measured every 5-30 minutes with the device at T_{base}=50°C. The outer loop is executed after key events (e.g. after each step in step-stress and before and after the stress experiment). In the outer loop, we first perform a carrier detrapping step by heating the device at 100°C for 30 min. Following this, we carry out a current collapse measurement [6], full I-V measurements, and full RF power sweeps with the device at room temperature.

DC figures of merit include I_{Dmax} (V_{GS}=2, V_{DS}=5 V), R_S, R_D (separately measured by the gate current injection technique [7]), and V_T. RF performance is evaluated through the saturated output power P_{out} (P_{in}=23 dBm, about 3 dB compression) and small-signal gain G_{lin} (P_{in}=10 dBm) at

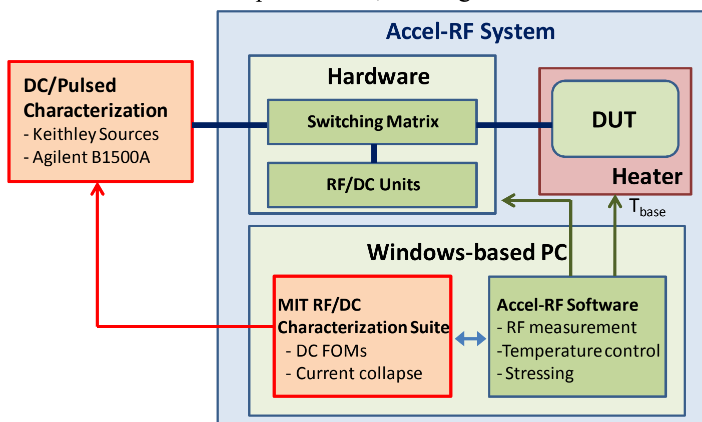

Fig. 1. System configuration of RF stress test setup.

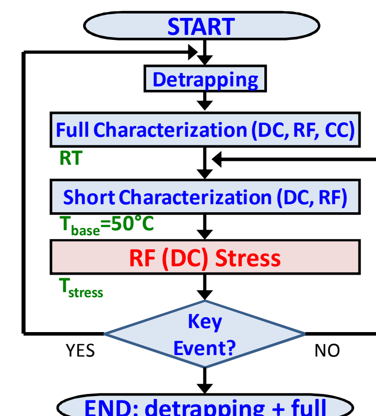

Fig. 2. Typical RF stress test procedure.

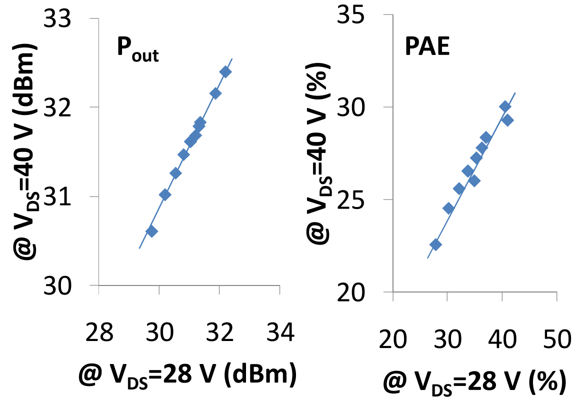

Fig. 3. Correlation between RF figures of merit measured at 28 V and at 40 V at room temperature during a typical RF stress test. For both conditions, I_{DQ}=100 mA/mm and P_{in}=23 dBm. The different data points represent measurements on the same device at different stages of RF stress.

V_{DS}=28 V and I_{DQ}=100 mA/mm. We have confirmed that RF performance at 28 V correlates well with that at 40 V, the designed operating voltage for the tested MMICs (**Fig. 3**). This is important because RF device characterization at 28 V is more benign than at 40 V. Our characterization strategy was verified to be benign after repeated runs.

Experimental Results

We have studied experimental single-stage internally-matched MMICs with 4x100 µm GaN HEMTs. This device technology is characterized by a critical voltage (V_{crit}) for OFF-state DC step-stress that is higher than 80 V at 150°C.

A. DC vs. RF and P_{in} step stress

Our first experiment was designed to compare DC and RF stress reliability at a typical RF operating point and to examine the role of RF power level. We first stressed a device in DC for 5 hours at V_{DS}=40 V and I_{DQ}=100 mA/mm. After this, RF stress was applied at increasing P_{in} from 20 to 26 dBm for 5 hours in each stage. During stress, the channel temperature T_j was maintained at ~170°C by appropriately adjusting the base plate temperature taking into account the power balance in the MMIC and its thermal resistance.

Figs. 4-6 show respectively the evolution of DC, RF and current collapse figures of merit during this experiment. In the DC stress phase, there is little degradation except for a small increase in current collapse. Adding RF induces a prominent increase in R_S, current collapse, permanent I_{Dmax} degradation [8], and a sharp decrease in P_{out} and G_{lin}. There was no change in I_G, which is attributed to the high V_{crit} of these devices. The prominent increase in R_S, much larger than R_D, at high P_{in} is markedly different from high-voltage DC stress induced degradation [1-2, 9-10]. An increased R_S negatively affects g_m, I_{Dmax}, P_{out} and G_{lin}. Although the total degradation in R_S was more than 150% as evaluated during the inner loop characterization (**Fig. 4**), its permanent degradation was only 8% as judged from measurements in the outer loop after electron detrapping (**Fig. 6**) (16% and 4%,

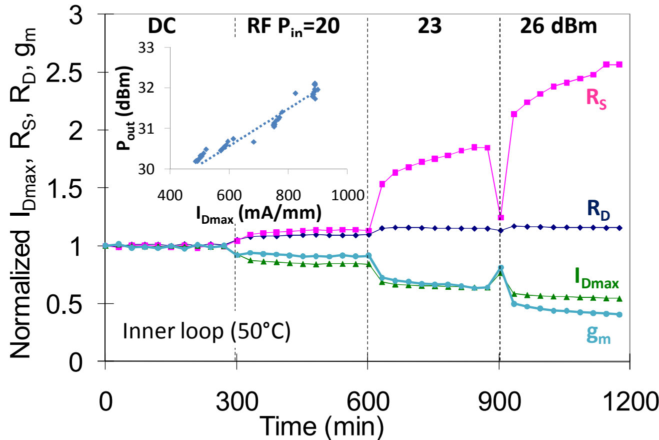

Fig. 4. Change in I_{Dmax}, R_S, R_D and g_m in a DC/RF step-P_{in} stress test. Device characterization from the inner loop at 50°C is shown. All FOMs are normalized to their unstressed values. The spikes in I_{Dmax} and R_S result from a detrapping step performed before the full characterization (Fig. 2). Inset shows correlation between P_{out} and I_{Dmax}.

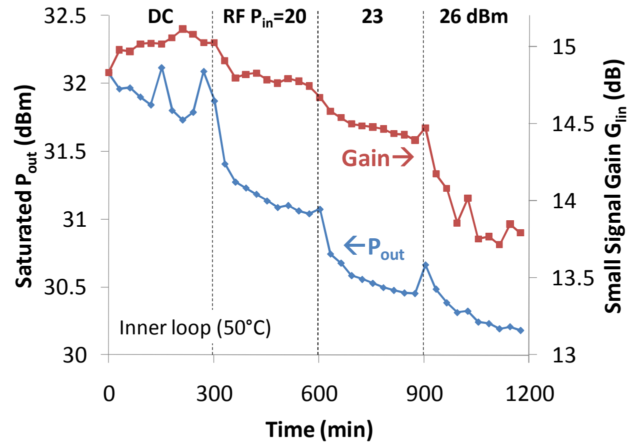

Fig. 5. Change in saturated P_{out} and small-signal gain G_{lin} measured at 28 V (inner loop in Fig. 2, T_{base}=50°C) in the experiment of Fig. 4.

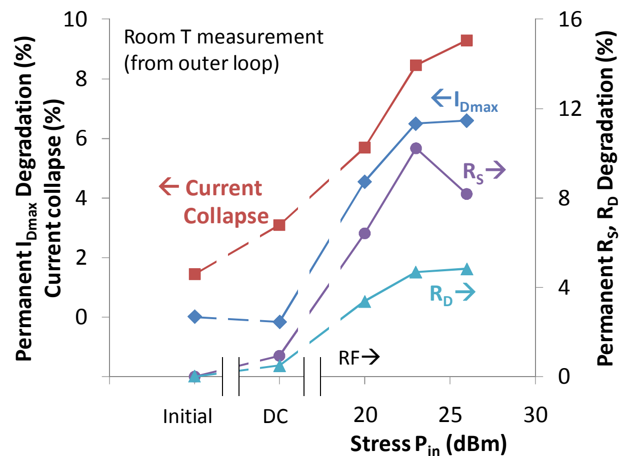

Fig. 6. Permanent I_{Dmax}, R_S, R_D degradation and current collapse vs. stress P_{in} (including pre-stress and DC-stress) in the experiment of Fig. 4. All these measurements are performed at room temperature in the outer loop (Fig. 2).

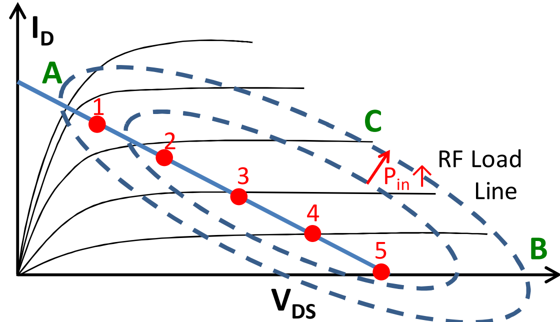

Fig. 7. Schematic of output characteristic and RF load line. Five bias points used in the experiment of Fig. 8 are marked on the idealized low-frequency load line (points 1-5). Three possible regimes responsible for RF degradation are marked: ON-state (A), OFF-state (B), and high power state (C).

respectively for R_D). This shows that most of the increase in R_S results from trapping. The relatively slow time constant of P_{out} and R_S degradation that are visible in **Figs. 5** and **4** suggests that RF stress is responsible for creating new traps. This is also consistent with the data in **Fig. 6**. A large R_S increase was unambiguously observed at high P_{in} RF stress in 15 MMICs tested under a variety of conditions.

This and many other experiments revealed a good correlation between degradation in DC and RF figures of merit (**Fig. 4** inset). A drop of I_{Dmax} of 21% corresponds to a drop in P_{out} of 1 dB [4]. We also found a tight correlation between G_{lin} and g_m (or R_S) (not shown).

In order to evaluate whether the R_S increase may result from high negative or positive instantaneous V_{GS} during RF swing, we performed V_{DS}=0 stress tests in DC. We found that up to V_{GS}=-30 V, R_S and R_D only increased by 5%. For V_{GS}>0, there was little change in R_S and R_D up to +3 V. This rules out this possibility. In addition, we find no evidence of structural degradation right next to the gate edge using the technique in [11]. This all suggests that we are in front of a new degradation mechanism that is unique to RF stress.

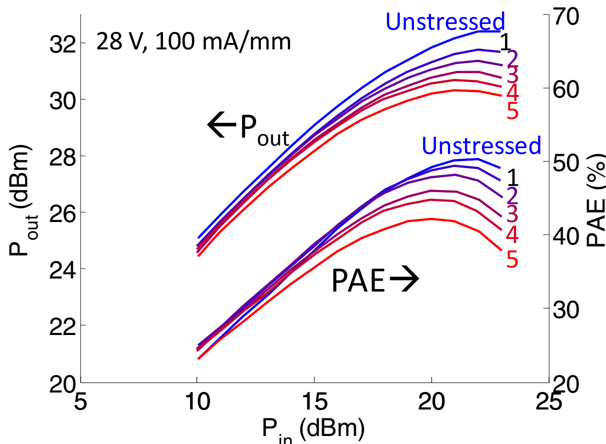

Fig. 8. Change in P_{out} and PAE characteristics at V_{DS}=28 V and 100 mA/mm (outer loop) in a step-V_{DS}-I_{DQ} RF stress test. The stress V_{DS} was stepped from 10 to 50 V in 10 V steps (5 hr/step) with P_{in}=23 dBm. I_{DQ} was reduced accordingly so as to remain on the designed load line of the MMIC. The stress points are marked in Fig. 7. T_j during stress was held constant at 175°C.

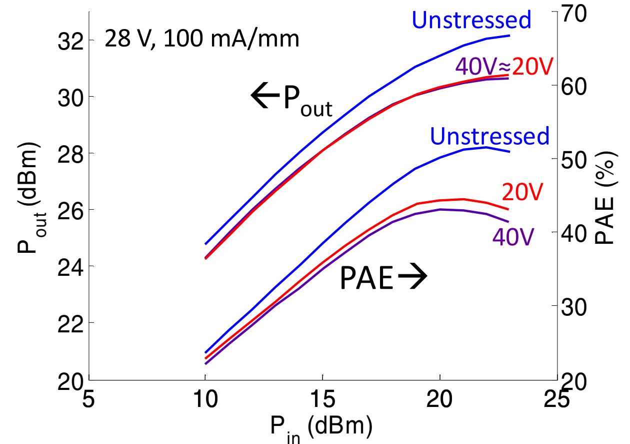

Fig. 9. Change in P_{out} and PAE characteristics at V_{DS}=28 V and 100 mA/mm (outer loop) in a step-V_{DS}-I_{DQ} RF stress test. The stress V_{DS} was stepped in a reverse order from 40 to 20 V (5 hr/step). These stress points correspond to points 4 and 2 in Fig. 7, respectively. T_j during stress was constant at 170°C.

B. Step-stress along the load line

At high frequency and high power level, the load line of a transistor power amplifier broadens up from a straight line into an ellipse. This brings the transistor into new regions of operation, as sketched in **Fig. 7**, and opens new possibilities for degradation under RF operation. In particular, there is the high-current ON regime (region A in **Fig. 7**), high-voltage OFF regime (B), and high-power regime (C).

In order to determine if one of these regions is responsible for the observed degradation, we performed a step-V_{DS}/I_{DQ} experiment with the device biased at different points along the load line (**Fig. 7**, V_{DS} =10 to 50 V in 10 V step, 5 h/step). P_{in} and T_j were 23 dBm and 175°C, respectively. **Fig. 8** shows RF power sweeps carried out in the outer loop at 28 V, 100 mA/mm. The data reveal that more degradation occurs after higher V_{DS} stress. There was >60% increase in R_S at high V_{DS} and 5.3% of permanent increase (20% and 5.3% for R_D). If done in the reverse order (high to low stress V_{DS}, **Fig. 9**), there was no additional degradation during the last step (lower V_{DS}/higher I_{DQ}). This suggests that the ON regime is not responsible for large-signal RF degradation in spite of very high compression with high positive I_G and high I_D.

C. OFF-state vs. high-power stress

In order to discriminate between the roles of stress regimes B and C in **Fig. 7**, we have performed an OFF-state step-stress experiment in DC (representing B) followed by RF stress (includes both B and C). First, V_{DS} was stepped from 30 to 80 V in 10 V step with V_{GS}=-5 V at T_j=T_{base}=120°C. Then, RF stress was applied at 40 V, 100 mA/mm and P_{in}=23 dBm (T_j=160°C). In order to rule out high temperature effects, 80 V DC OFF-state stress was performed at T_j=T_{base}=160°C immediately before the RF stress.

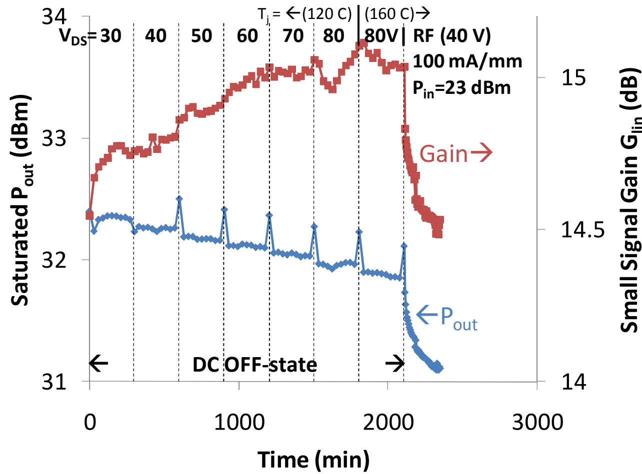

Fig. 10. Change in P_{out} and G_{lin} at V_{DS}=28 V and 100 mA/mm during DC OFF-state step-stress test. Stress condition was V_{GS}=-5 V and V_{DS}=30 to 80 V in 10 V step at 120°C. Another 80 V step was performed at 160°C before stressing the device in RF with V_{DS}=40 V and P_{in}=23 dBm (T_j=160°C).

Fig. 10 shows the evolution of P_{out} and G_{lin} at 28 V and 100 mA/mm as measured in the inner loop at T_{base}=50°C. DC stress produced minor degradation, even at 80 V and T_j=160°C. This is testament to the high V_{crit} of this technology and shows that region B is relatively benign in spite of very high E-field. Upon turning on the RF drive, despite the much lower V_{DS}=40 V, the device degrades sharply. **Fig. 11** shows the evolution of DC figures of merit in this experiment as measured in the outer loop. Degradation is only observed after the RF input is turned on and is characterized by a prominent increase in R_S. This experiment suggests that region C is responsible for degradation since it is only reached under the RF input.

D. High-power pulsed stress

In an effort to confirm that the high power region with high I_D and high V_{DS} (C) is the main cause of the sharp R_S increase, we tried to emulate this stress condition without RF input. This is not possible under DC stress because the very high power dissipation leads to high channel temperature and device destruction. Instead, we stressed HEMT devices under pulsed conditions (500 µs pulse width, 0.05% duty cycle). 100 pulses with different V_{DS} and I_D are applied for stress. As shown in **Fig. 12**, for stress voltage beyond 50 V under high current condition, R_S sharply increases. This is consistent with the RF results. Although the detailed degradation mechanism is not clear, it is consistent with a trap formation due to hot-carrier origin [1] since it requires both high I_D and V_{DS} at the same time. We speculate that hot holes produced by impact ionization create traps as they are swept towards the source side. Confirming this requires further studies.

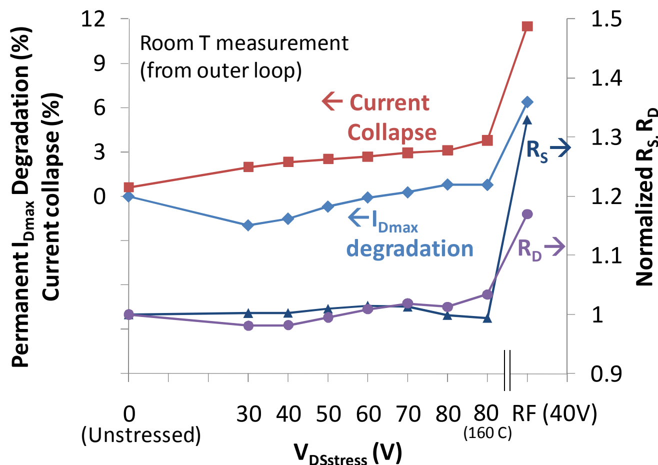

Fig. 11. Change in permanent I_{Dmax} degradation, current collapse (outer loop), R_D, and R_S (inner loop) in the experiment of Fig. 10.

Conclusions

In summary, we have developed a methodology to study the RF reliability of GaN HEMTs. We found a dominant degradation mechanism that produces a large degradation in $R_S$and I_{Dmax}, both mostly due to trapping, and a loss of P_{out}. This mechanism is associated with the high-power region of the device and is therefore presumed to be related to trap formation due to hot carrier effects. Our research reveals the difficulty of using DC life tests for estimating large signal RF reliability.

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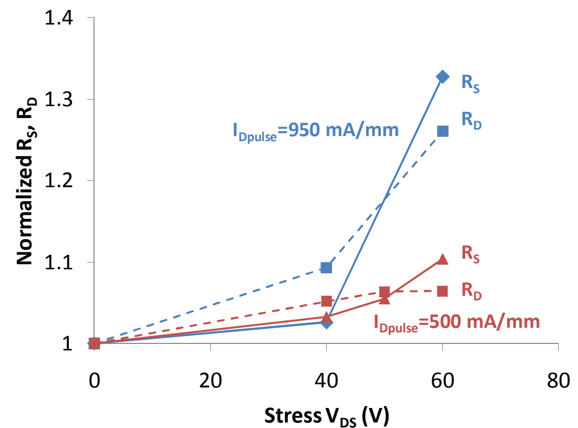

Fig. 12. Change in R_S and R_D in pulsed stress tests at room temperature. Pulse width was 500 µs and duty cycle was 0.05%.