III-V CMOS:

A sub-10 nm Electronics Technology?

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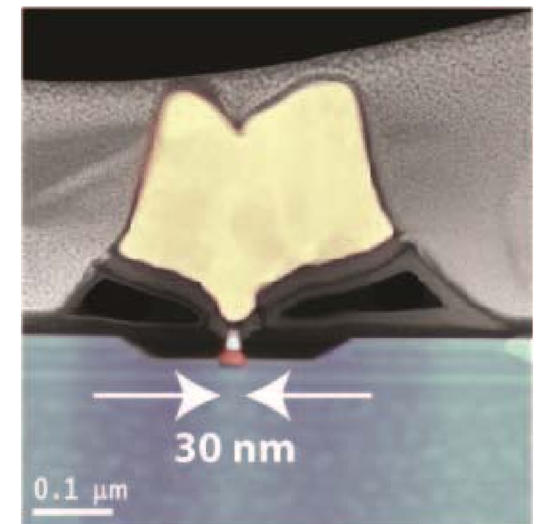
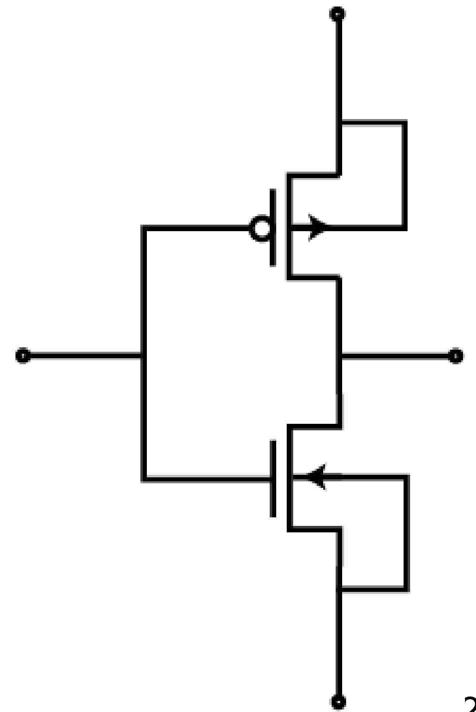
MTL, NSL, SEBL



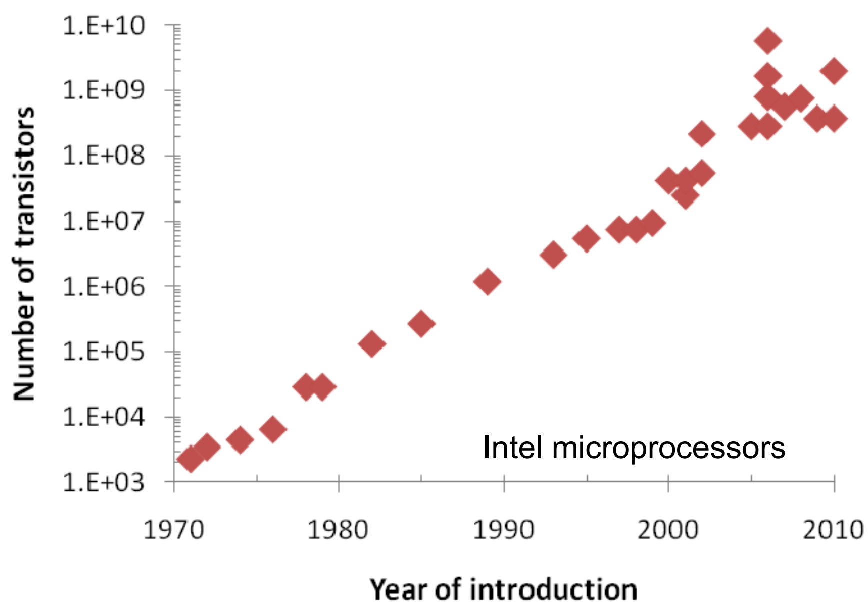
Outline

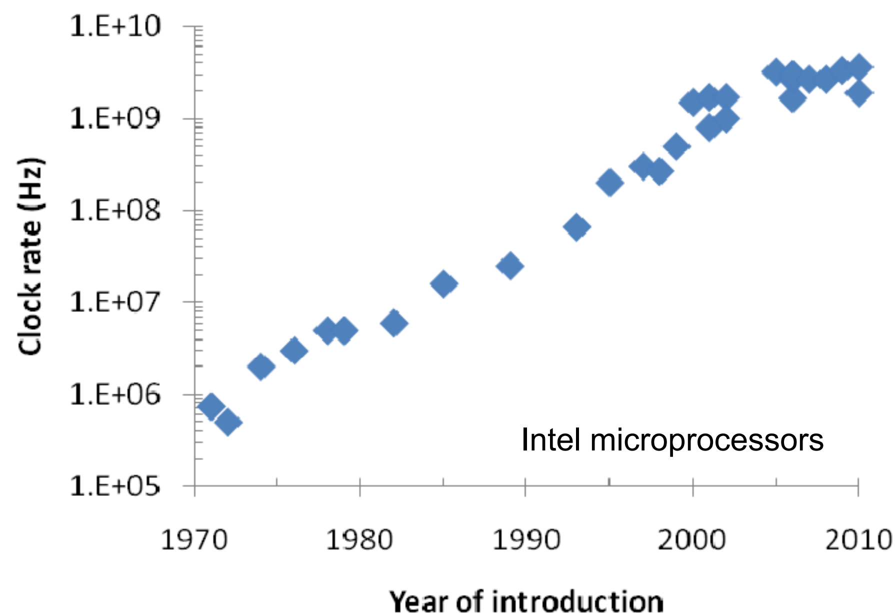
- Why III-Vs for CMOS?
- Lessons from III-V HEMTs
- The challenges for III-V CMOS
- The prospects of 10 nm III-V CMOS
- Conclusions



The Si CMOS Revolution: *Smaller is Better!*

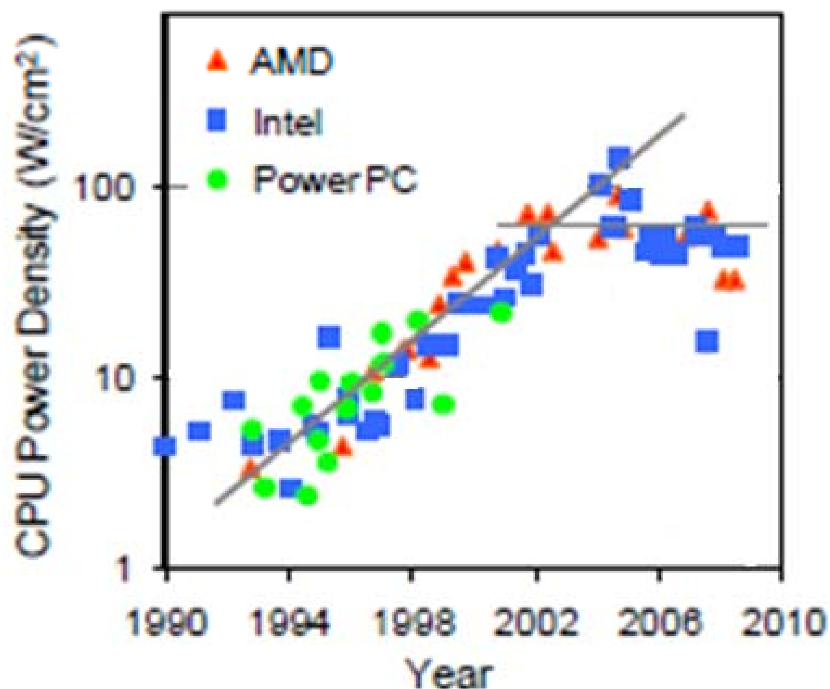
- Virtuous cycle of CMOS scaling
  → exponential improvements in:
  - *Transistor density ("Moore's law")*
  - *Performance*
  - *Power efficiency*



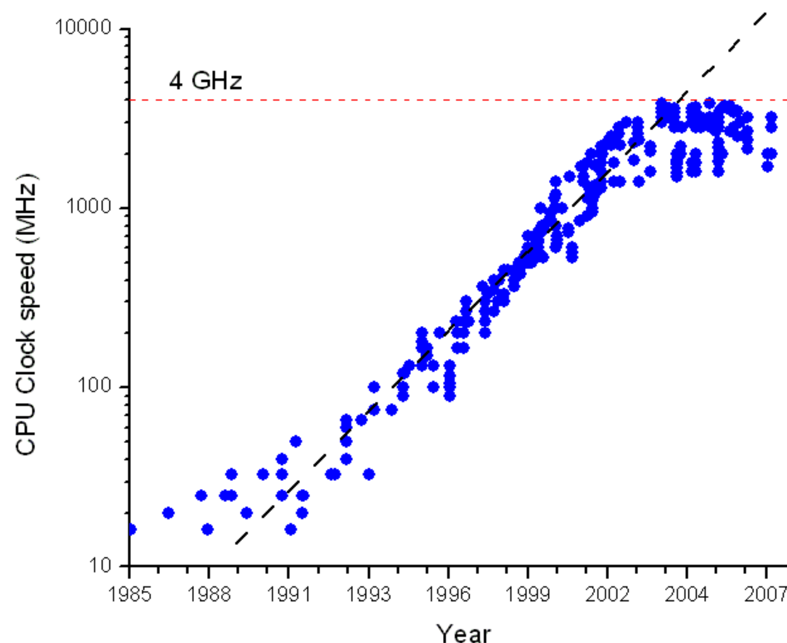


Recent trend in CMOS scaling

- Si CMOS has entered era of *"power-constrained scaling":*
  - CPU power density saturated at ~100 W/cm^2
  - CPU clock speed saturated at ~ 4 GHz



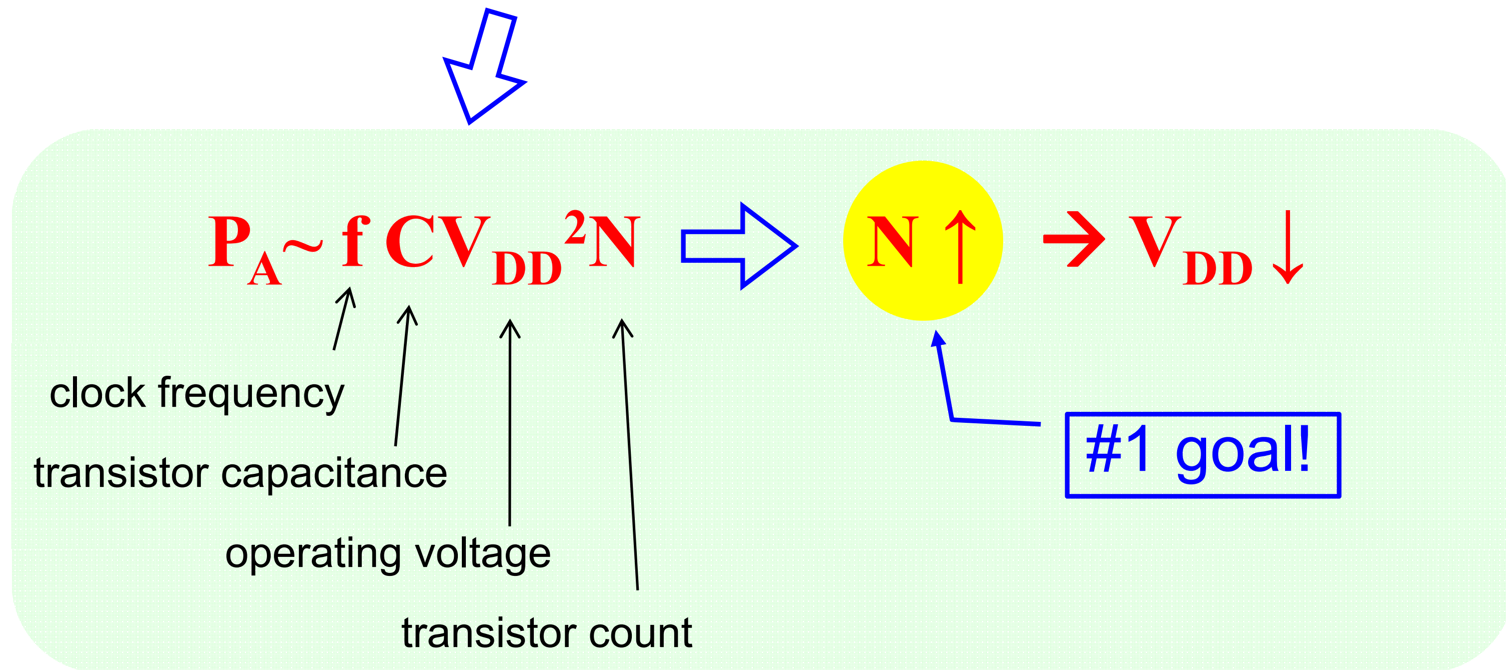
Pop, Nano Res 2010



http://www.chem.utoronto.ca/~nlipkowi/pictures/clockspeeds.gif

Consequences of Power Constrained Scaling

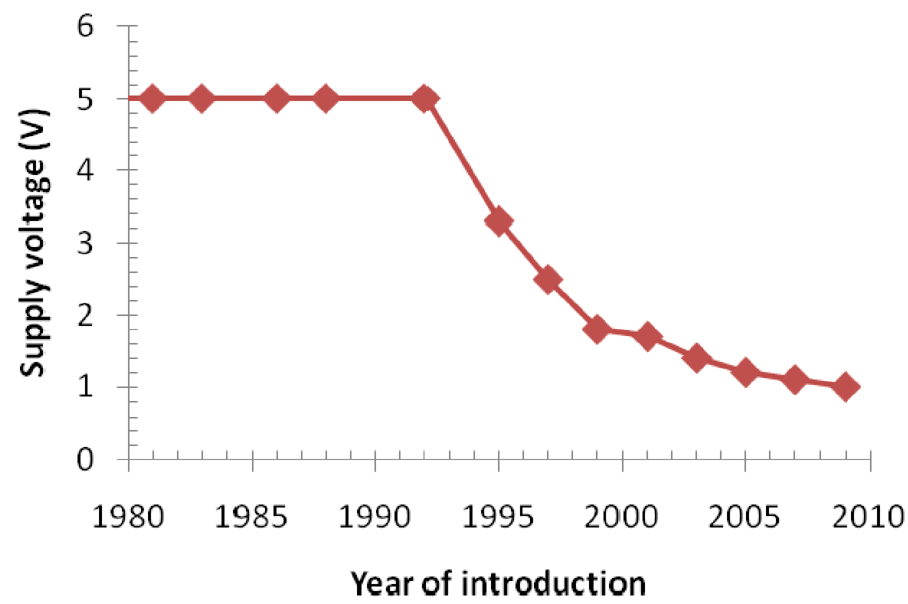
Power = active power + passive power



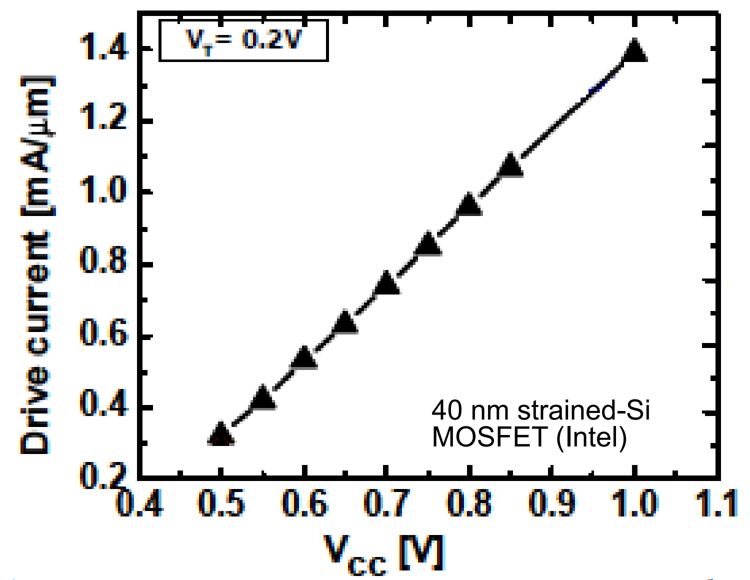
→ Transistor scaling requires reduction in supply voltage

CMOS power supply scaling

Recently, V_{DD} scaling very weakly:



Because Si performance degrades as $V_{DD}\downarrow$:

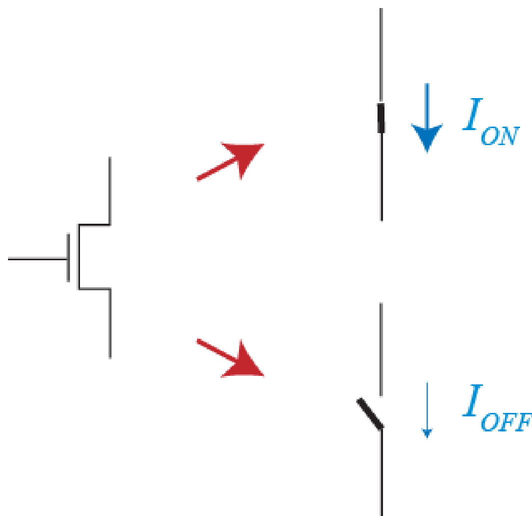


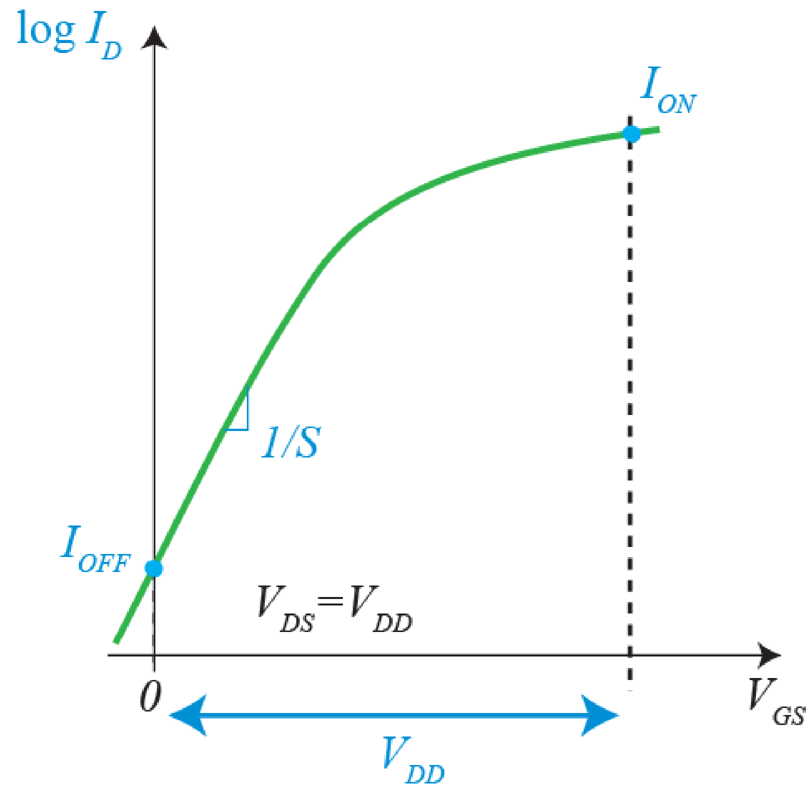
Dewey, IEDM 2009

→ Need scaling approach that allows V_{DD} reduction while enhancing performance

How III-Vs allow further V_{DD} reduction?

- Goals of scaling:
  - Reduce transistor footprint
  - extract maximum I_{ON} for given I_{OFF}





How III-Vs allow further V_{DD} reduction?

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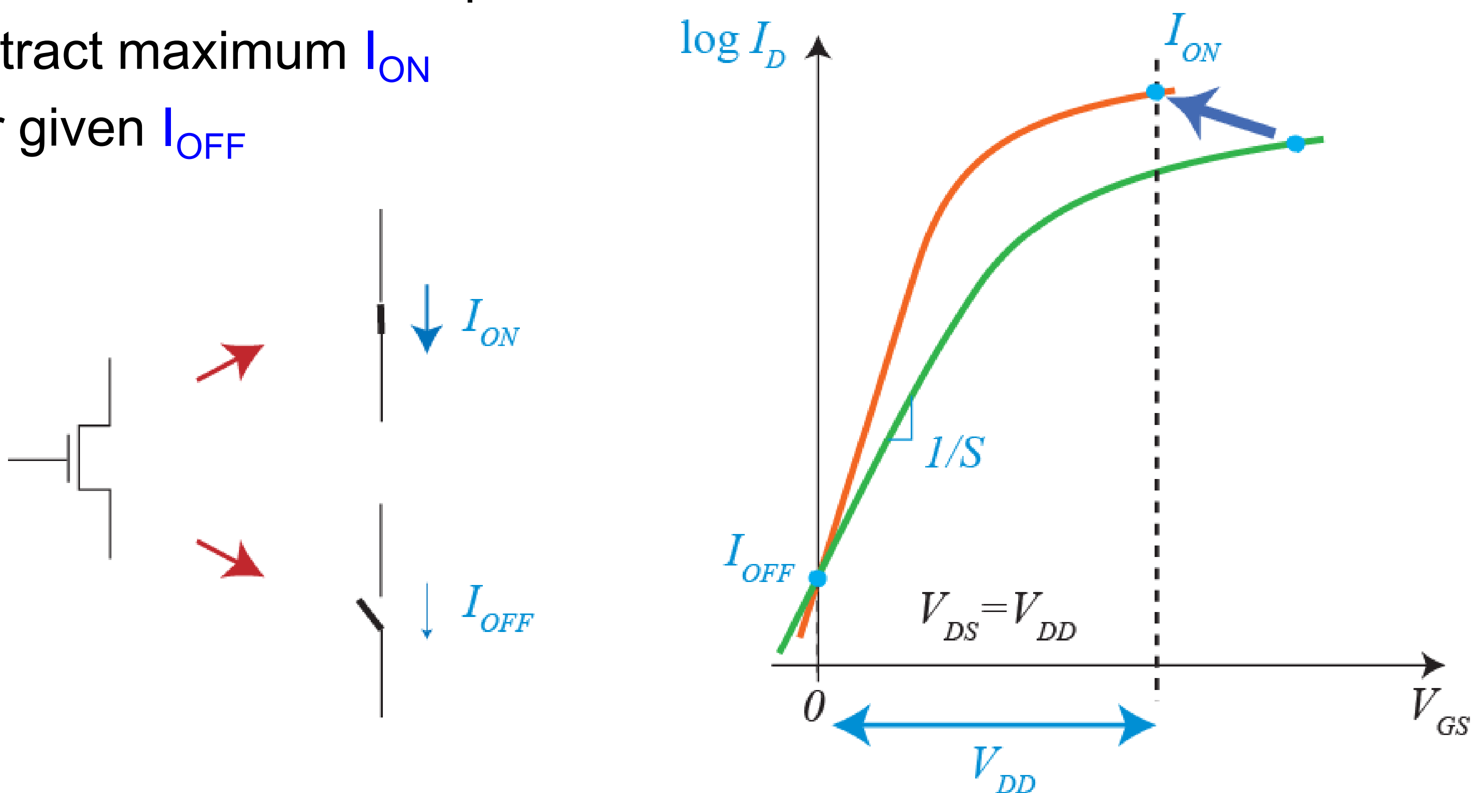
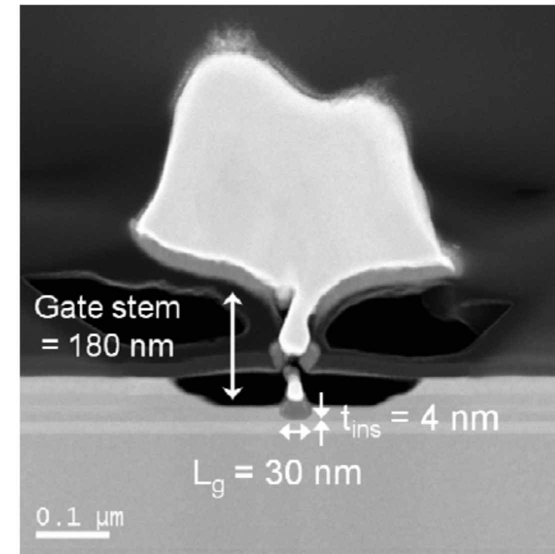
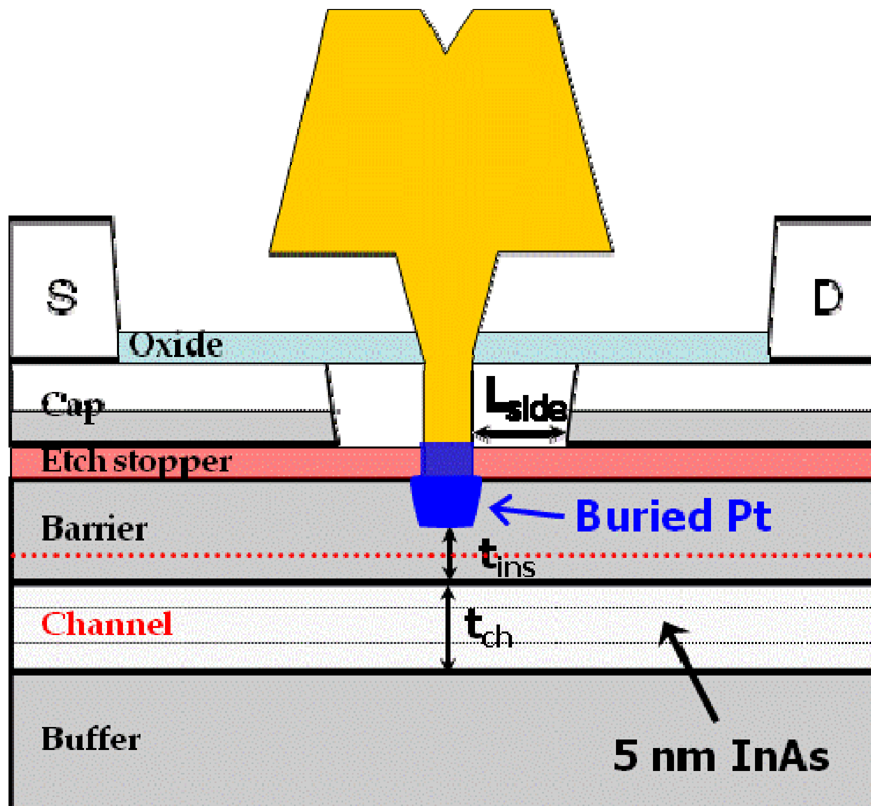


- III-Vs:
  - higher electron velocity than Si → I_{ON} ↑
  - very tight carrier confinement → S ↓ → sharp turn on

III-V High Electron Mobility Transistors

- State-of-the-art: InAs-channel HEMT





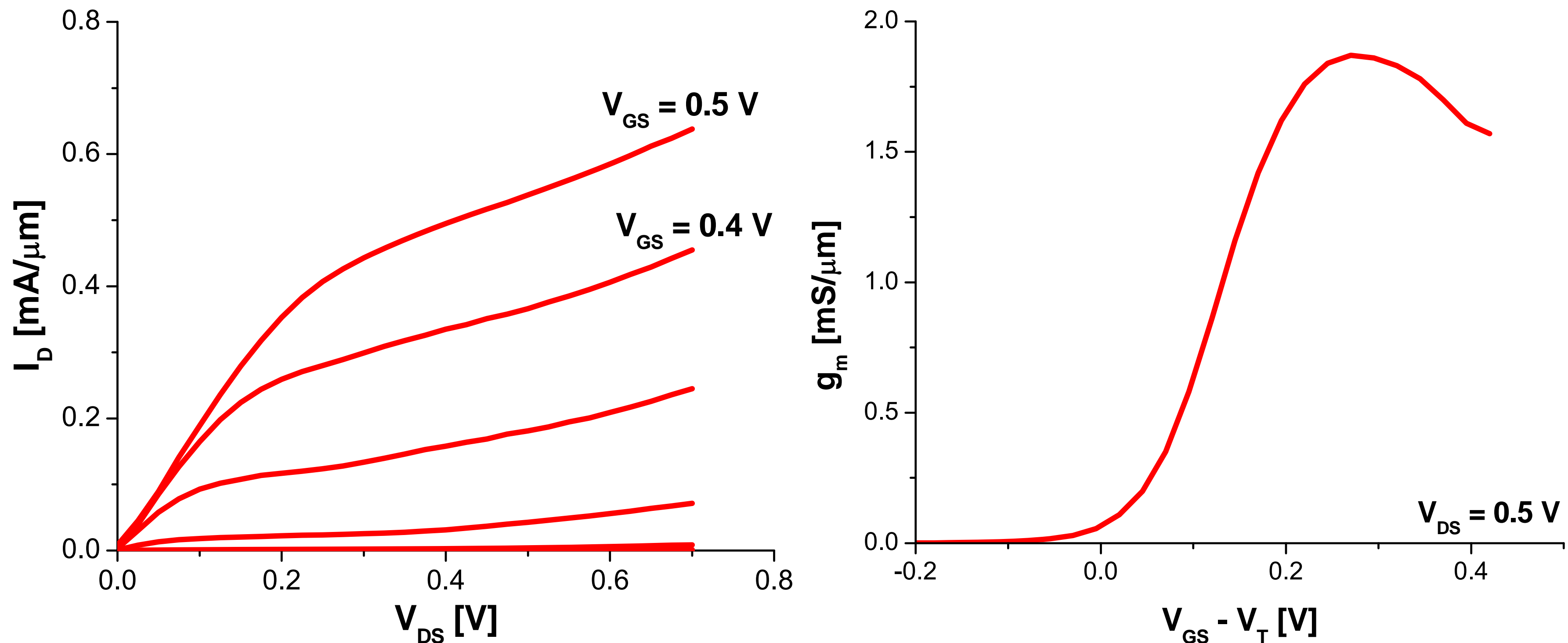
- QW channel (t_{ch} = 10 nm) :
  - InAs core (t_{InAs} = 5 nm)
  - InGaAs cladding
- $\mu_{n,Hall}$ = 13,200 cm^2/V-sec
- InAlAs barrier (t_{ins} = 4 nm)
- Pt/Ti/Mo/Au Schottky gate
- L_g=30 nm

Kim, IEDM 2008

III-V HEMTs

- L_g=30 nm InAs-channel HEMT

Kim, IEDM 2008

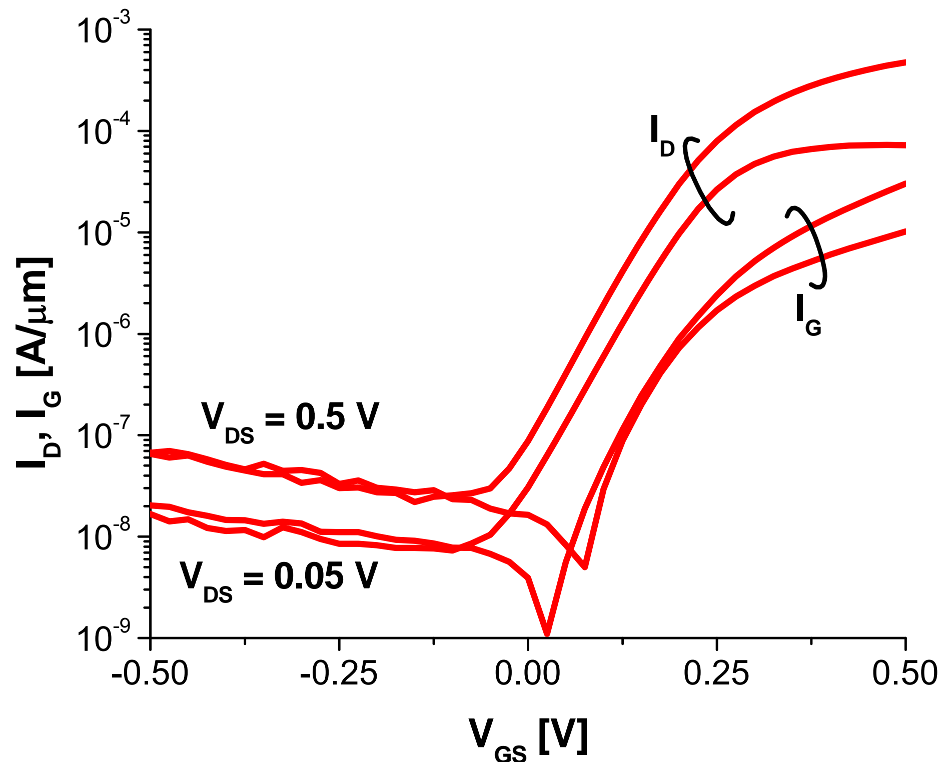


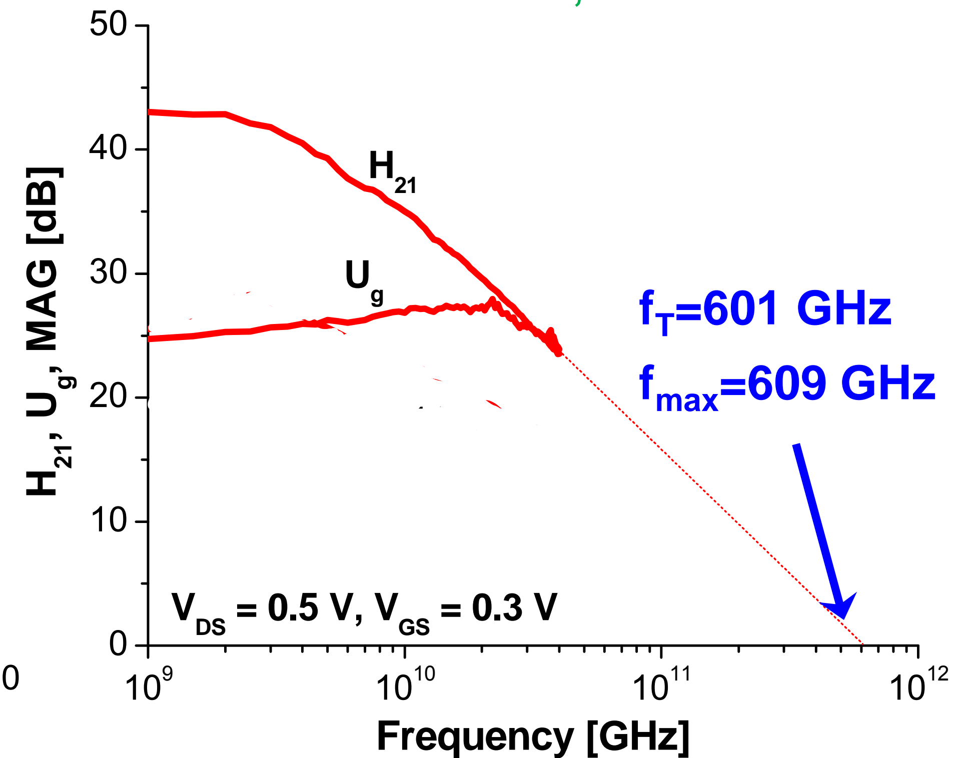
- Large current drive: I_{ON}=0.4 mA/μm at V_{DD}=0.5 V
- Enhancement-mode FET: V_T = 0.08 V
- High transconductance: g_{mpk}= 1.8 mS/um at V_{DD}=0.5 V

III-V HEMTs

- L_g=30 nm InAs-channel HEMT

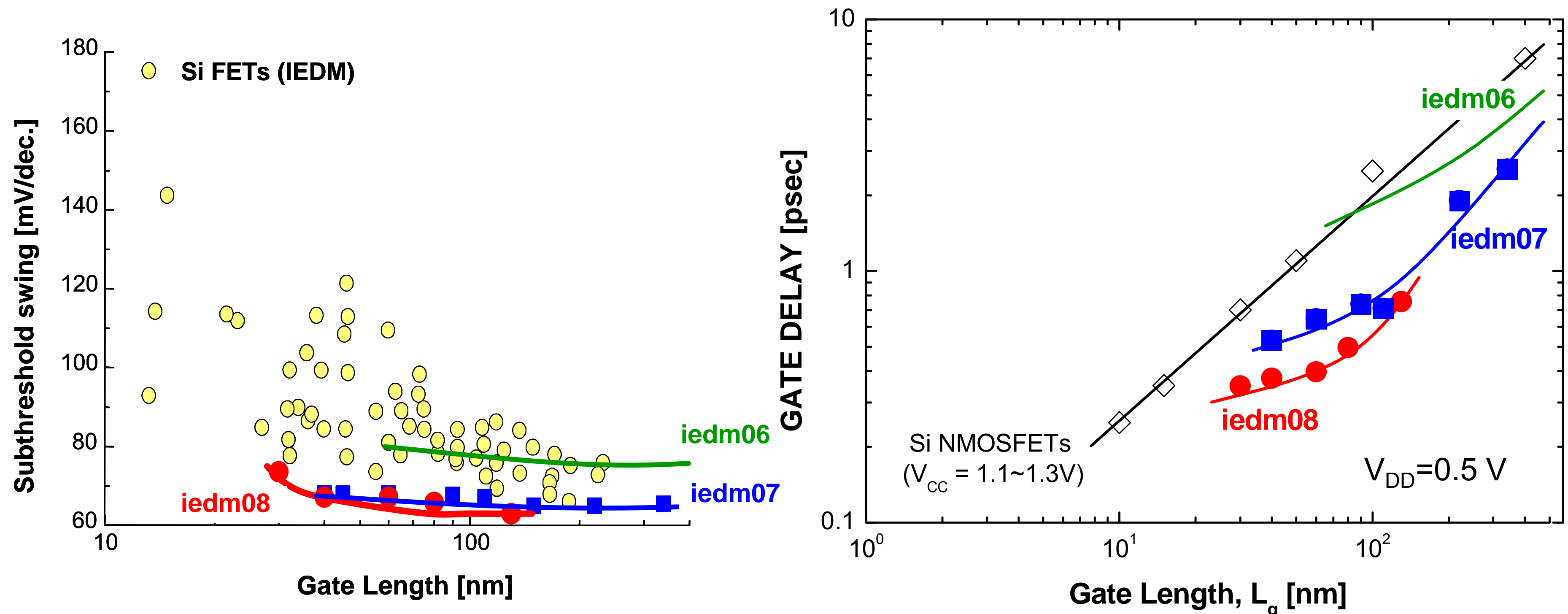
Kim, IEDM 2008





- S = 73 mV/dec, I_{on}/I_{off}=~10^4
- First transistor with both f_T and f_{max} > 600 GHz

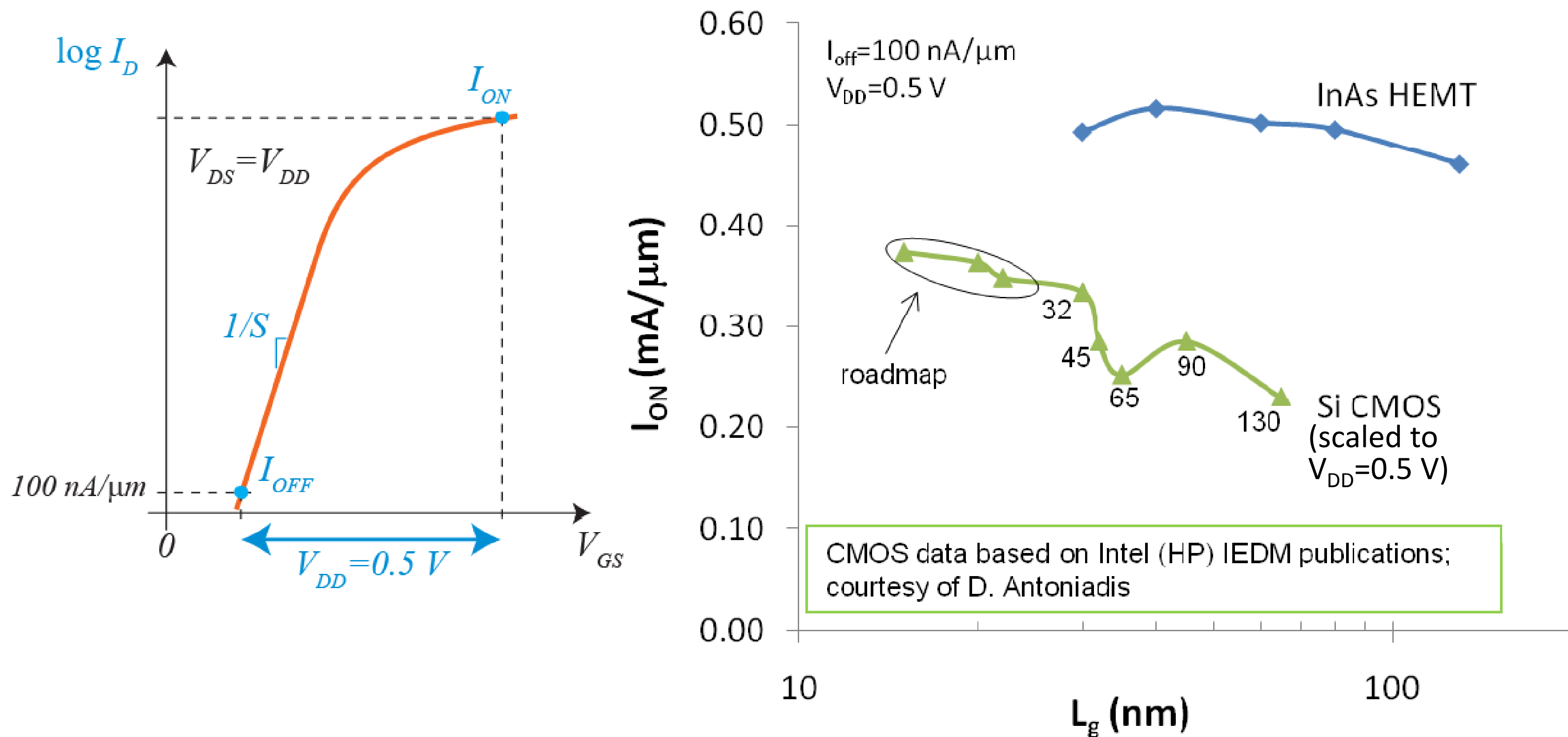
Scaling of III-V HEMTs: Benchmarking with Si



- Superior short-channel effects as compared to Si MOSFETs
- Lower gate delay than Si MOSFETs at lower V_{DD}

Scaling of III-V HEMTs: Benchmarking with Si

- FOM that integrates short-channel effects and drive current: I_{ON} @ I_{OFF}=100 nA/μm, V_{DD}=0.5 V

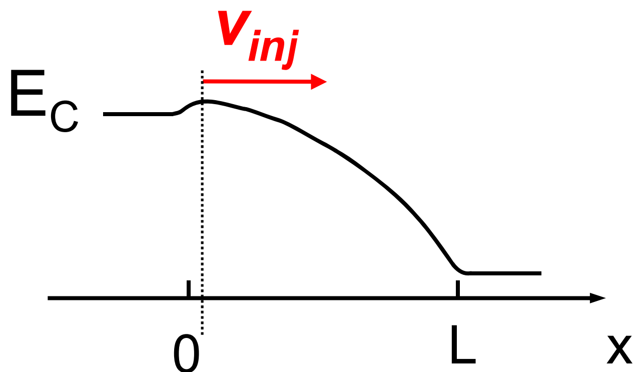


III-V HEMTs: higher I_{ON} for same I_{OFF} than Si

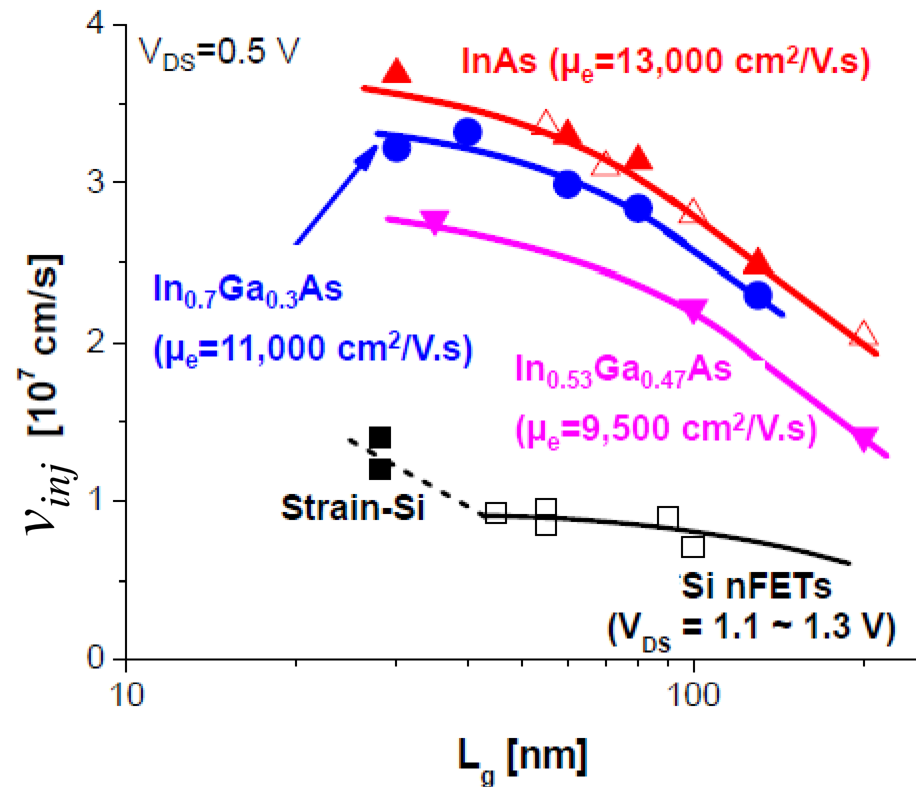
Lessons from III-V HEMTs

1. Very high electron injection velocity at the virtual source

Kim, IEDM 2009



v_{inj} ≡ electron injection velocity at virtual source

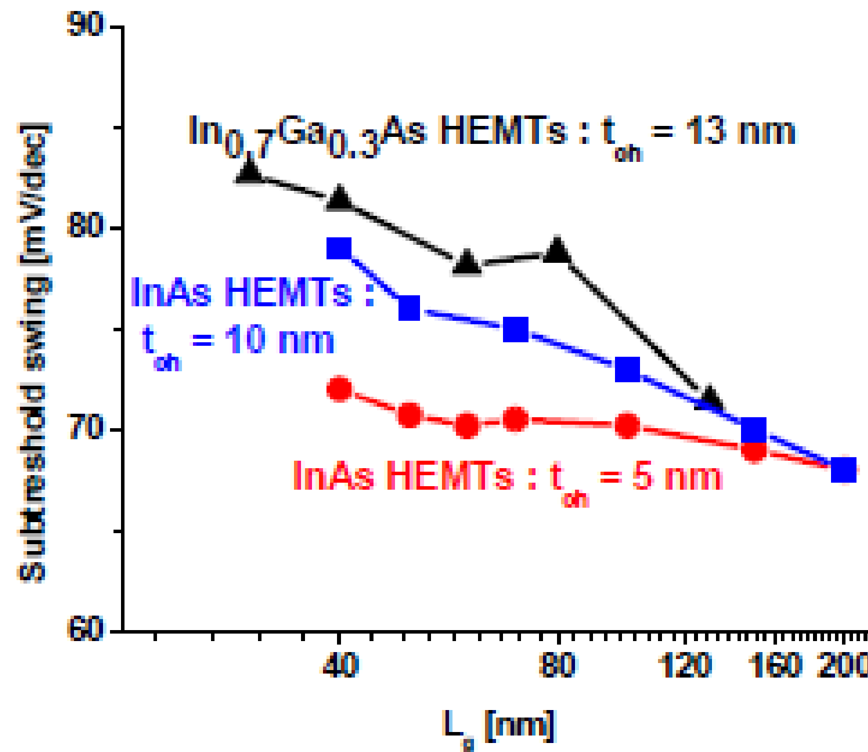


- v_{inj}(InGaAs) increases with InAs fraction in channel
- v_{inj}(InGaAs) $> 2v_{inj}$(Si) at less than half V_{DD}

Lessons from III-V HEMTs

2. Quantum-well channel key to outstanding short-channel effects

Kim, IPRM 2010

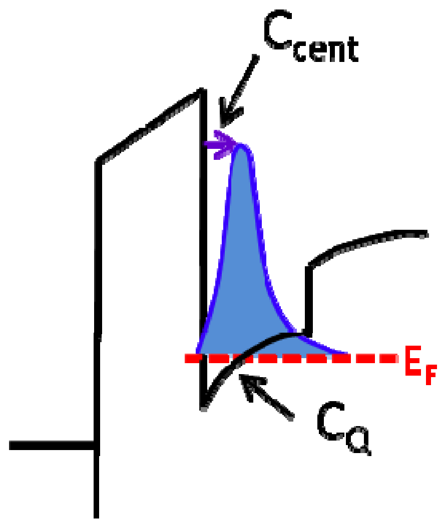


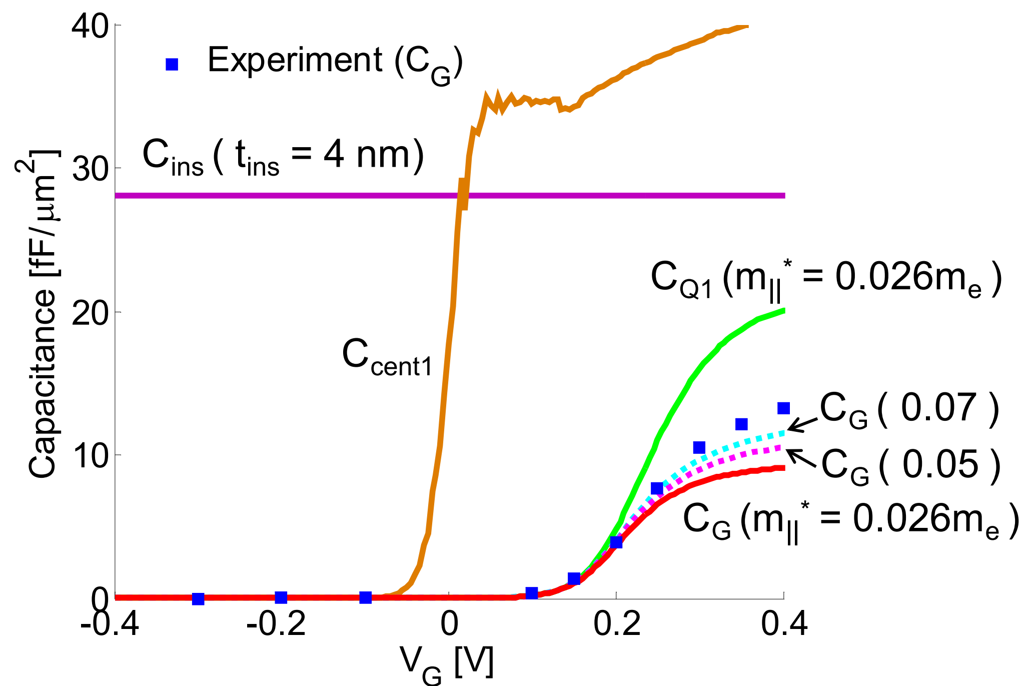
- Dramatic improvement in short-channel effects in thin channel devices

Lessons from III-V HEMTs

3. Quantum capacitance less of a bottleneck than commonly believed

InAs channel: t_{ch} = 10 nm

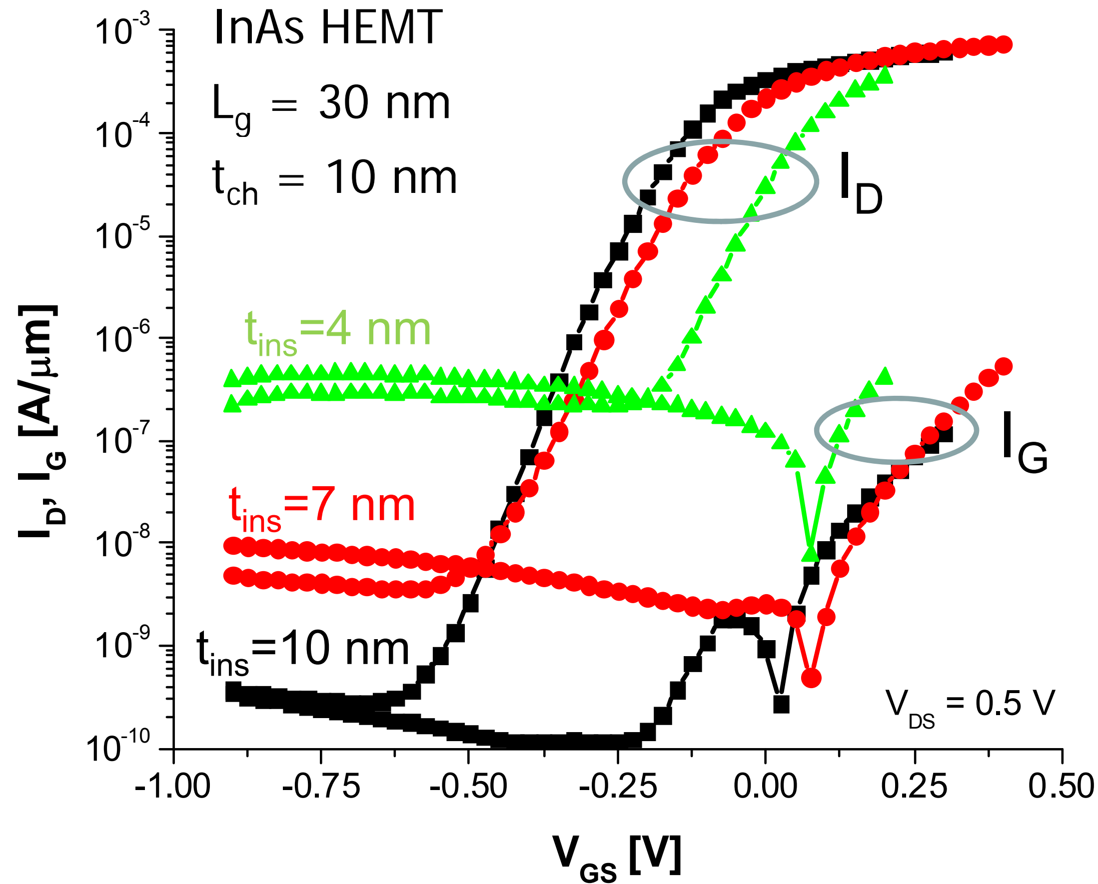


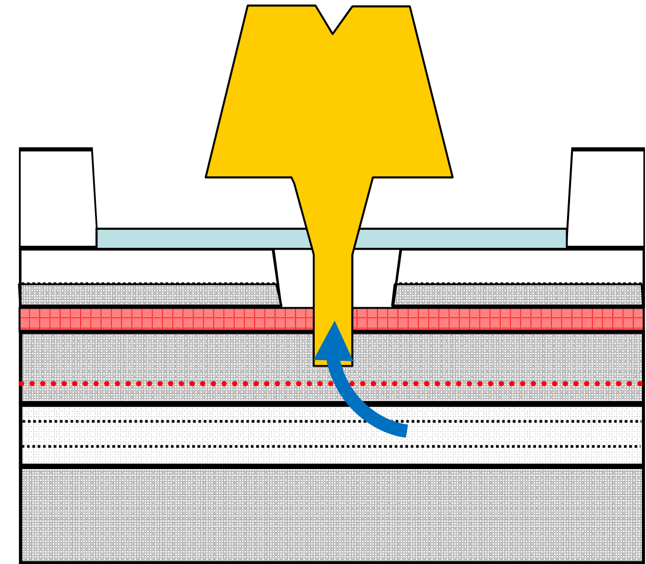


Biaxial strain + non-parabolicity + strong quantization increase $m_{||}^*$ → C_G↑

Jin, IEDM 2009

Limit to III-V HEMT Scaling: Gate Leakage Current



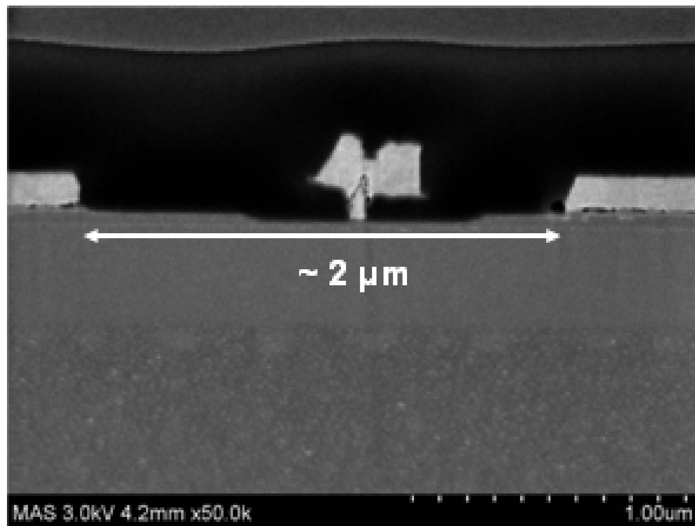


$t_{ins} \downarrow \rightarrow I_G \uparrow$

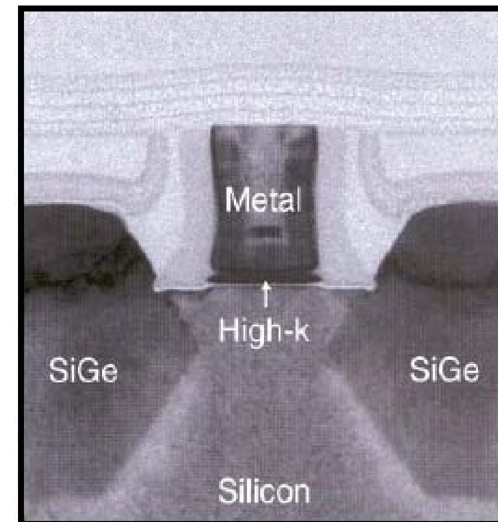
→ Further scaling requires high-K gate dielectric

The Challenges for III-V CMOS: III-V HEMT vs. Si CMOS

III-V HEMT



Intel's 45 nm CMOS

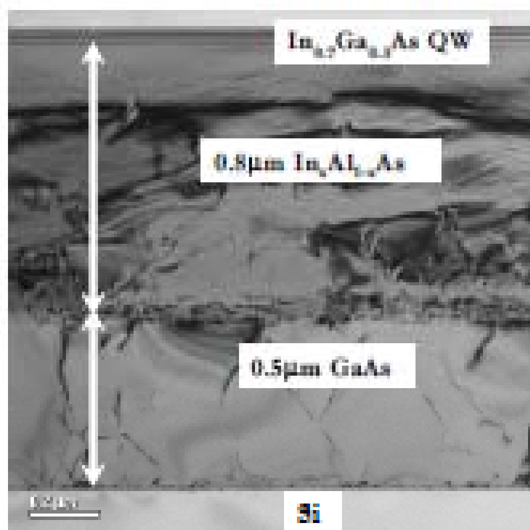


Critical issues:

- Schottky gate → MOS gate
- Footprint scaling [1000x too big!]
- Need self-aligned contacts
- Need p-channel device
- Need III-V on Si

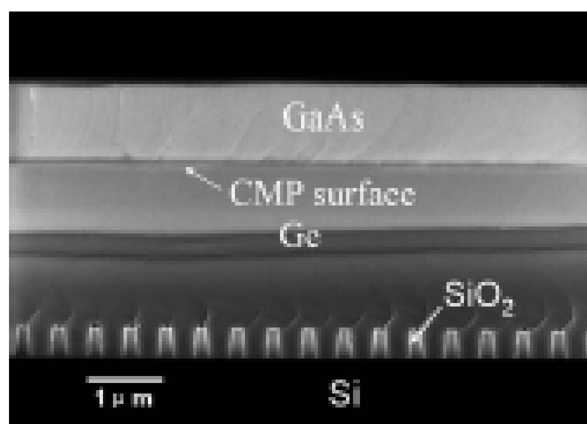
III-V's on Si

- The challenge:
  - III-V heterostructures on large-area Si wafers
  - Thin buffer layer
  - Low defectivity
- Some notable work:



Direct III-V MBE on Si (Intel)

Hudait, IEDM 2007



Aspect Ratio Trapping (Amberwave)

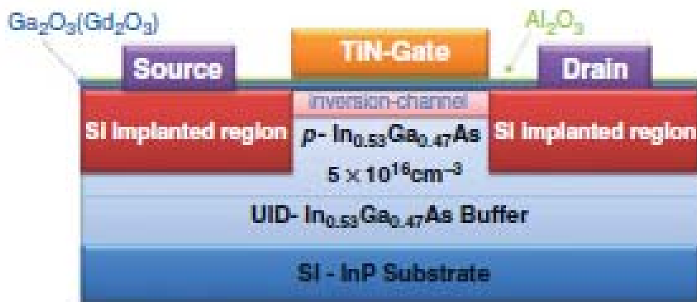
Wu, APL 2008

InAs Nanoribbon MOSFETs on Insulator (UCB)

Ko, Nature 2010

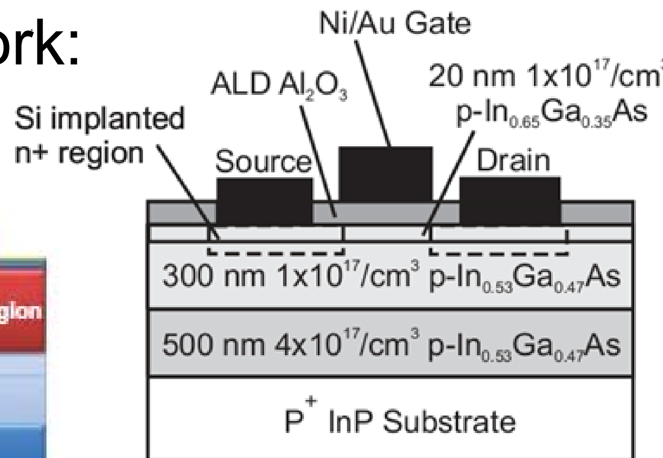
The gate stack

- Challenge: metal/high-K oxide gate stack
  - Fabricated through *ex-situ* process
  - Thin EOT (<1 nm)
  - Low leakage (<10 A/cm^2)
  - Low D_{it} (<10^{11} eV^{-1}.cm^{-2} in top ~0.3 eV of bandgap)
  - Reliable
- Some notable work:



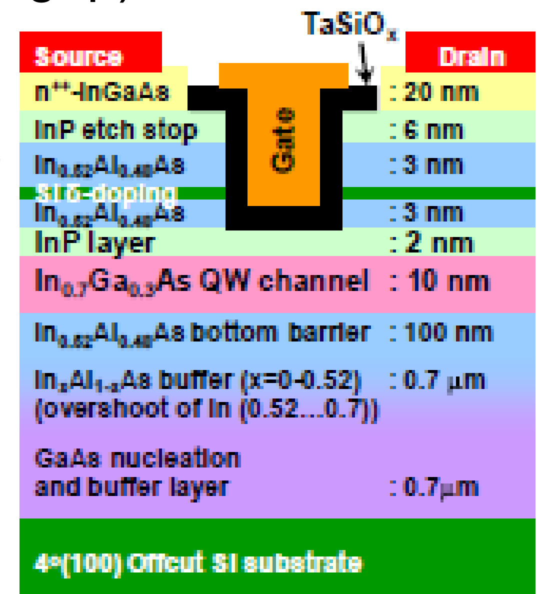
Al_2O_3 /GGO on InGaAs by MBE/ALD (Tsinghua)

Hong, MRS Bull 2009



Al_2O_3 by ALD (Purdue)

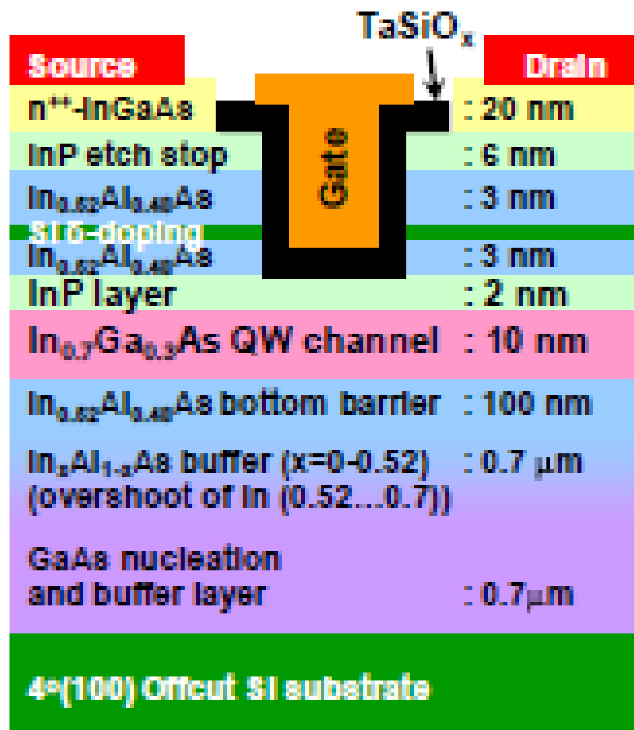
Wu, EDL 2009

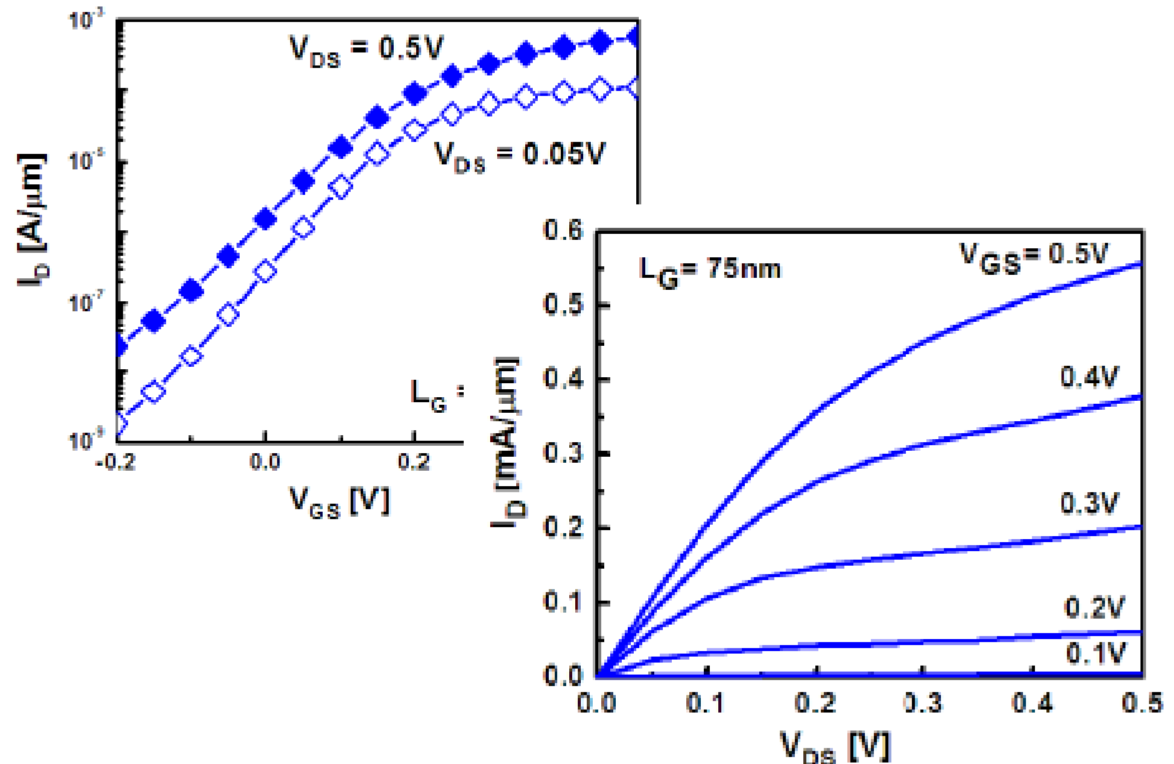


$TaSiO_x$ on InGaAs by ALD (Intel)

Radosavljevic, IEDM 2009

$In_{0.7}Ga_{0.3}As$ Quantum-Well MOSFET (Intel)

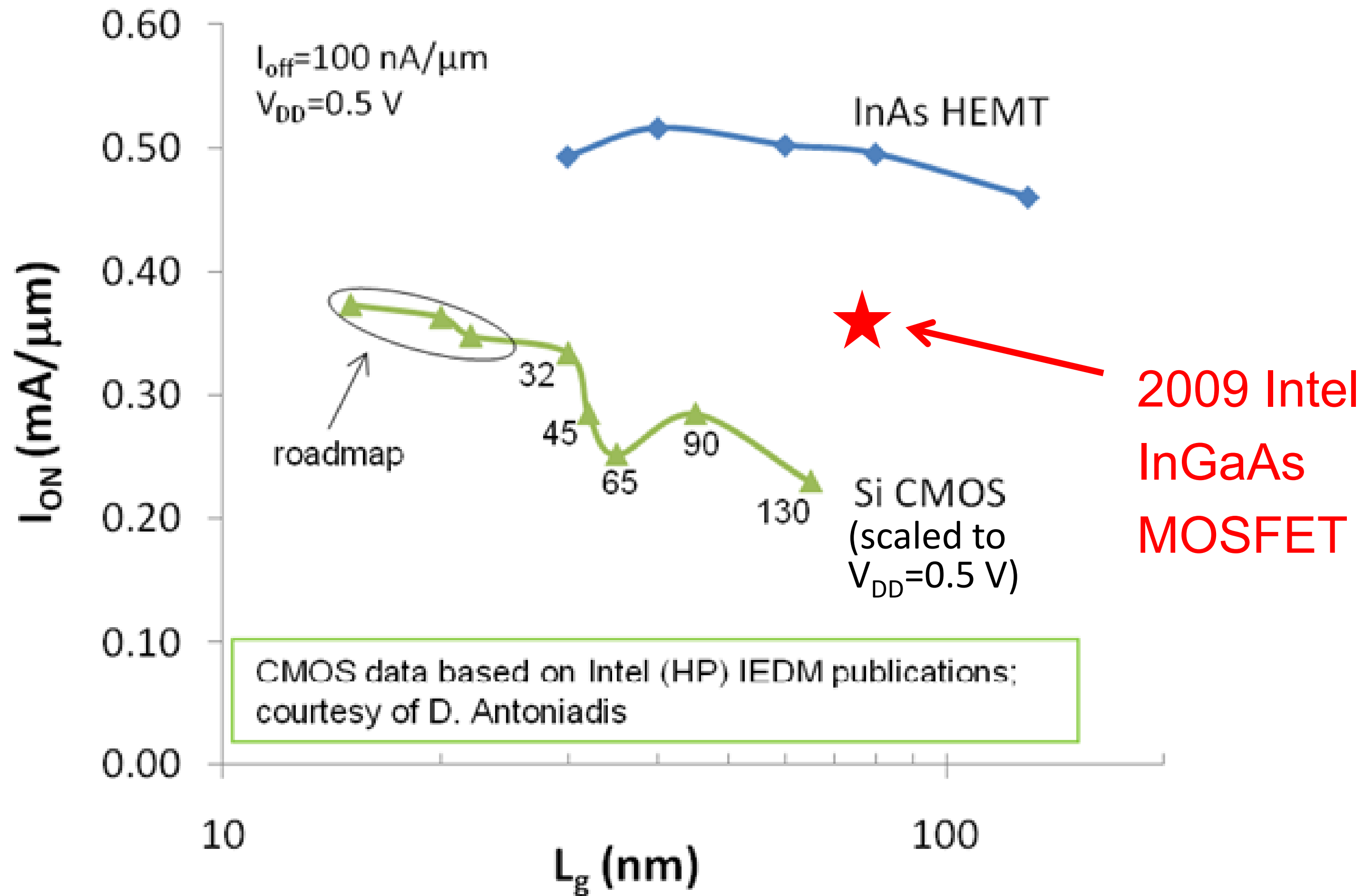




- Direct MBE on Si substrate (1.5 µm buffer thickness)
- InGaAs buried-channel MOSFET (under 2 nm InP etch stop)
- 4 nm $TaSiO_x$ gate dielectric by ALD, TiN/Pt/Au gate
- L_g=75 nm

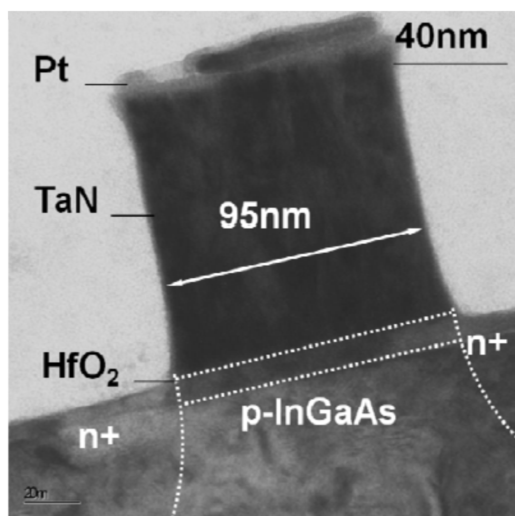
Radosavljevic, IEDM 2009

$In_{0.7}Ga_{0.3}As$ Quantum-Well MOSFET



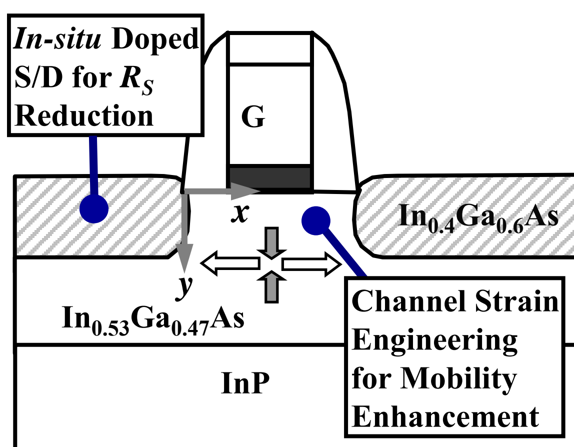
Self-aligned device architecture

- The challenge:
  - MOSFET structures with scalability to 10 nm
  - Self-aligned gate design
- Some notable work:



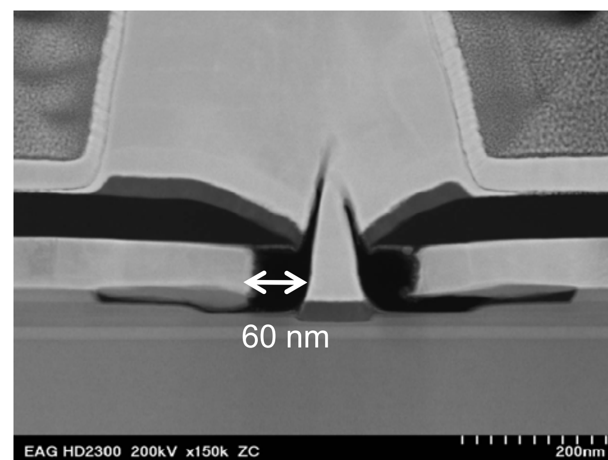
Ion-implanted self-aligned InGaAs MOSFET (NUS)

Lin, IEDM 2008



Regrown ohmic contact MOSFET (NUS)

Chin, EDL 2009



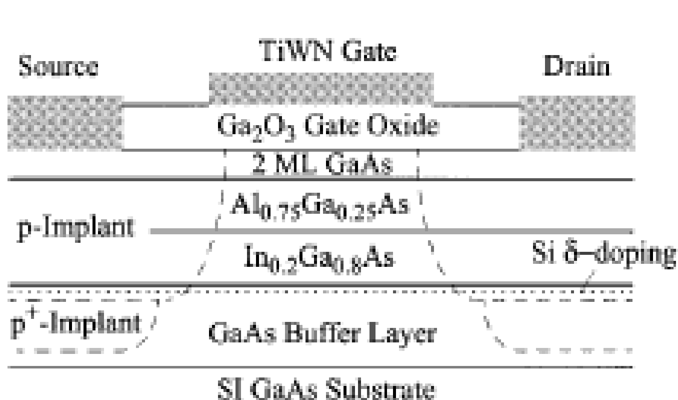
Quantum-well FET with self-aligned W contacts (MIT)

Waldron, TED 2010

P-channel MOSFETs

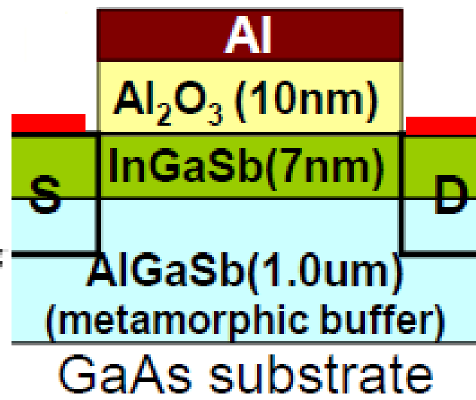
- The challenge:
  - Performance >1/3 that of n-MOSFETs
  - Capable of scaling to <10 nm gate length regime
  - Co-integration with III-V NMOSFET on Si

- Some notable work:



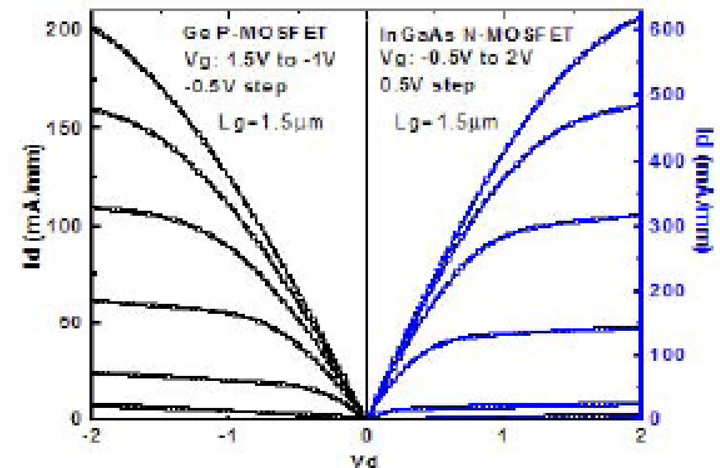
Ga_2O_3/AlGaAs/GaAs MOSFET (Motorola)

Passlack, EDL 2002



Al_2O_3/InGaSb QW-MOSFET (Stanford)

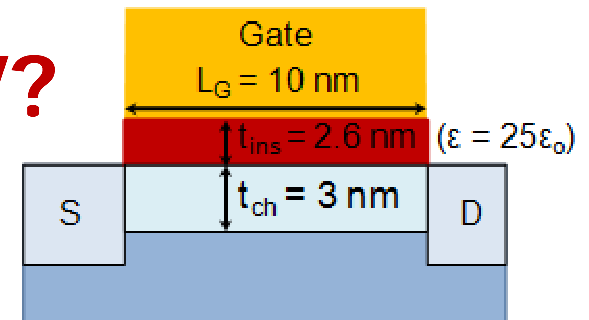
Nainani, IEDM 2010



Al_2O_3 by ALD on InGaAs and Ge MOSFETs (IMEC)

Lin, IEDM 2009

What can we expect from ~10 nm III-V NMOS at 0.5 V?



With thin InAs channel:

$$\begin{aligned} I_D &= q n_s v_{inj} \\ &= 1.6 \times 10^{-19}\ C \times \boxed{4 \times 10^{12}\ cm^{-2}} \times \boxed{3.8 \times 10^{7}\ cm/s} \\ &= 2.4\ mA/\mu m \end{aligned}$$

Assume R_S as in Si (~80 Ω.μm):

$$I_D = 1.5\ mA/\mu m$$

Key requirements:

- High-K/III-V interface, thin channel do not degrade v_{inj}
- Obtaining R_s=80 Ω.μm at required footprint
- Acceptable short-channel effects

Three greatest worries!

Conclusions

- III-Vs attractive for CMOS: key for low V_{DD} operation
  - Electron injection velocity in InAs > 2X that of Si at 1/2X V_{DD}
  - Quantum well channel yields outstanding short-channel effects
  - Quantum capacitance less of a limitation than previously believed
- Impressive recent progress on III-V CMOS
  - Ex-situ ALD and MOCVD on InGaAs yield interfaces with unpinned Fermi level and low defect density
  - Sub-100 nm InGaAs MOSFETs with I_{ON} > than Si at 0.5 V demonstrated
- Lots of work ahead:
  - Demonstrate 10 nm III-V MOSFET that is better than Si
  - P-channel MOSFET
  - Manufacturability, reliability