Formation of Structural Defects in AlGaN/GaN High Electron Mobility Transistors under Electrical Stress

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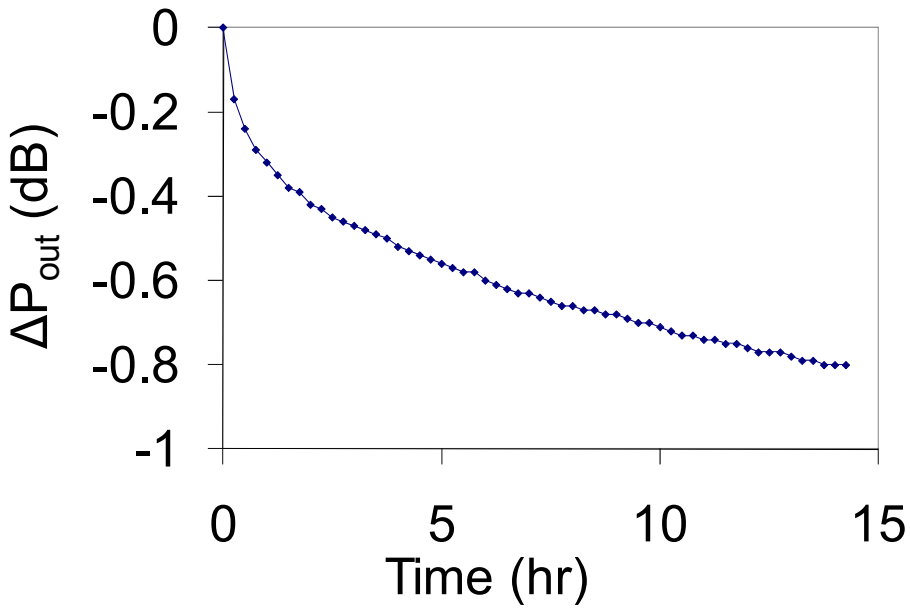
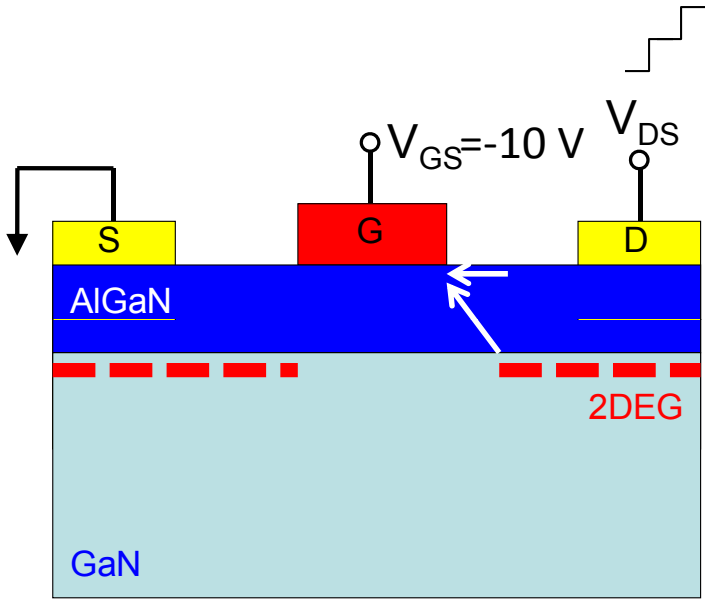
Introduction

- GaN HEMT Reliability: big concern
  - RF power degradation
  - I_D decrease, R_D increase, I_G increase, V_T change…
- Goal: understand degradation mechanism

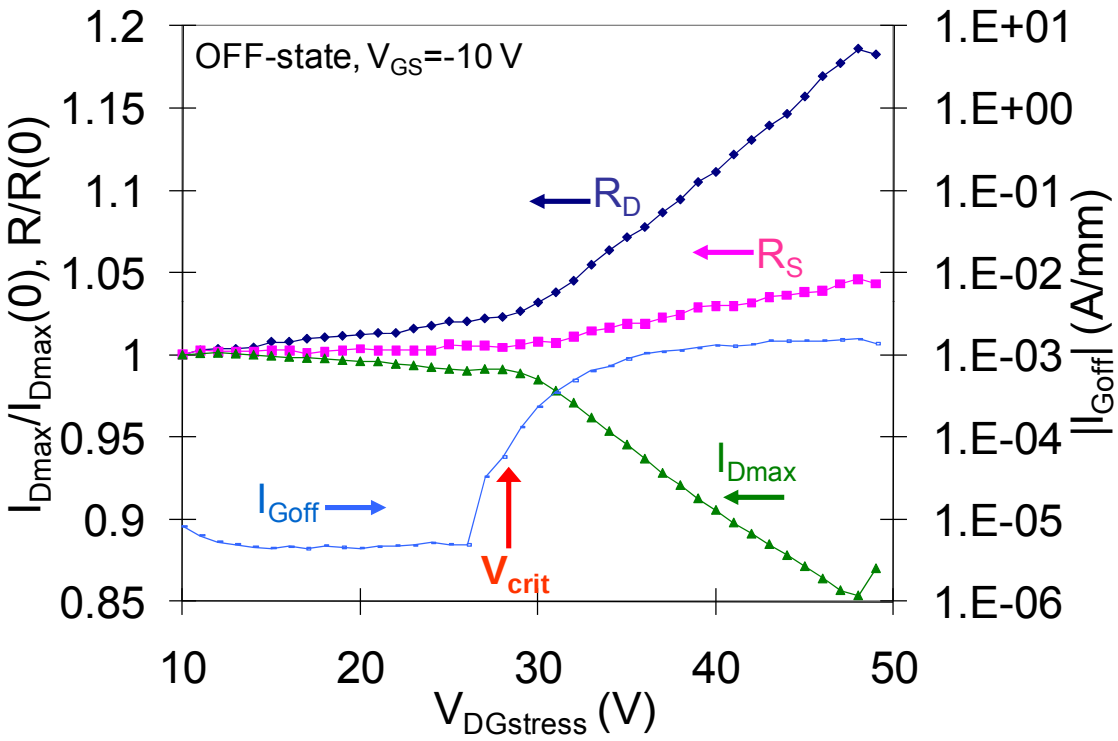
RF stress
10 GHz,V_D=28 V
I_{DQ}=150 mA/mm
P_{in}=23 dBm
P_{out}=33.7 dBm



High Voltage Degradation in GaN HEMTs



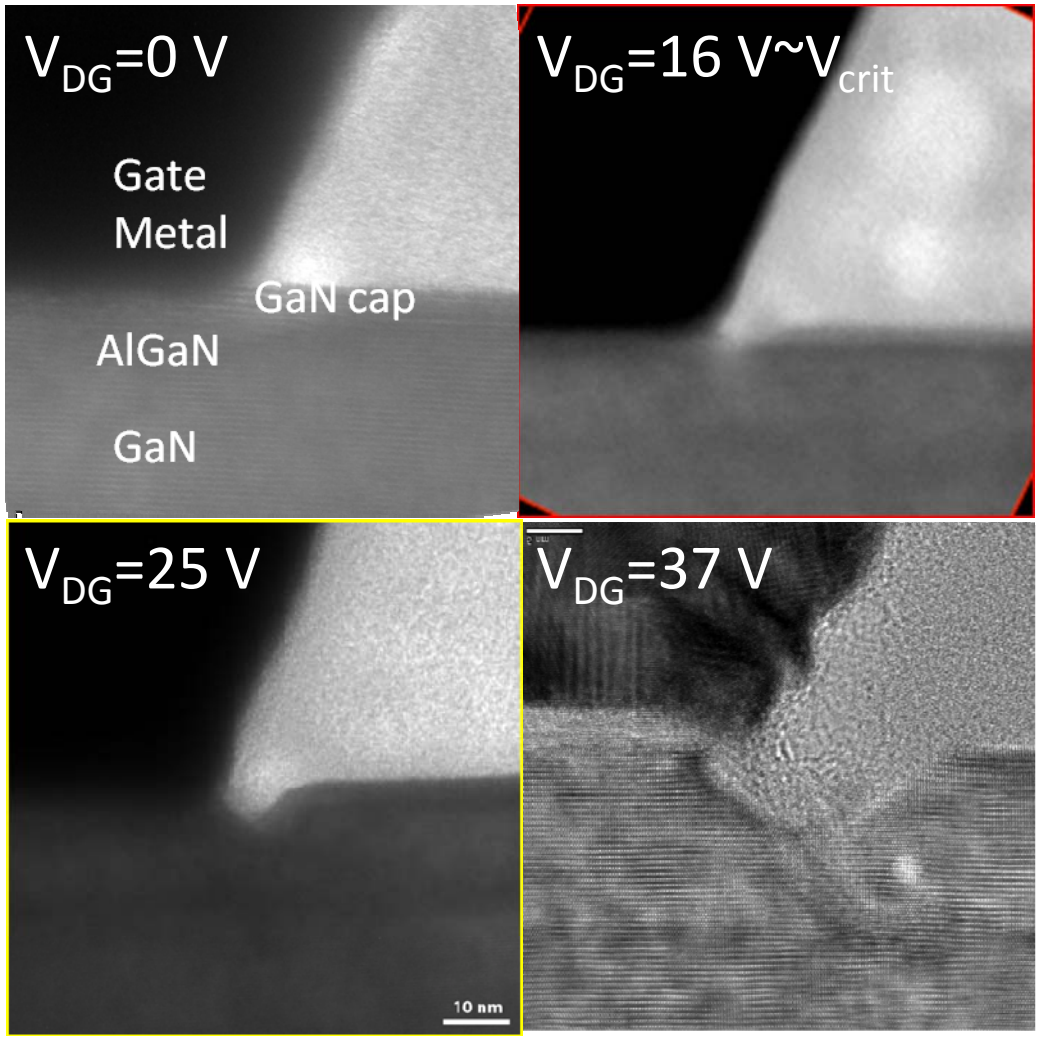
Joh, EDL 2008

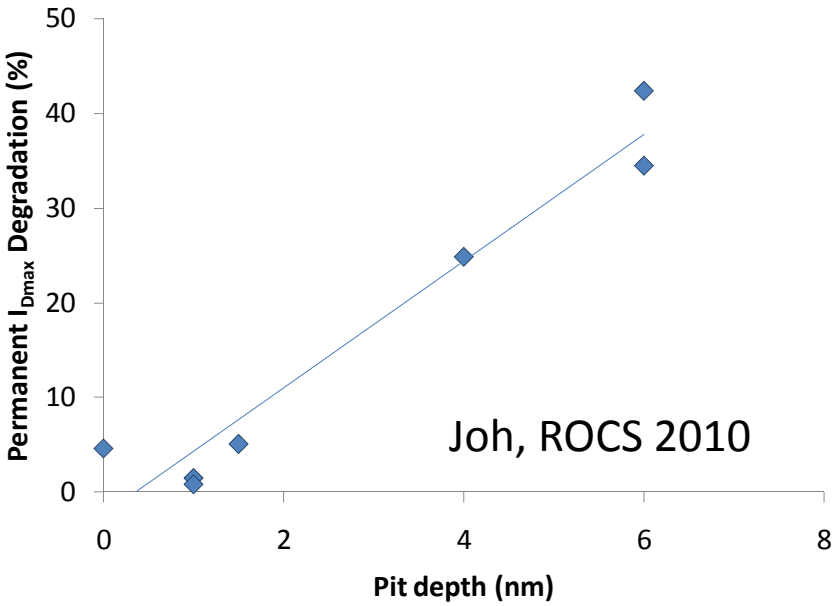


I_{Dmax}: V_{DS}=5 V, V_{GS}=2 V I_{Goff}: V_{DS}=0.1 V, V_{GS}=-5 V

I_D, R_D, and I_G *start to degrade beyond critical voltage (V_{crit})*
(+ trapping behavior – current collapse)
Common physical origin in I_D and I_G degradation

Material Degradation around V_{crit}



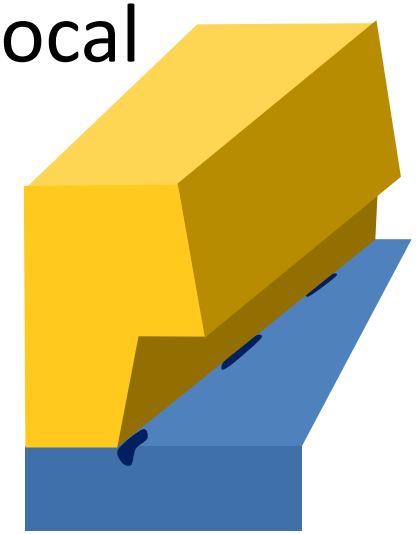


Good correlation between pit depth and electrical degradation

Initial dimple followed by deeper pitting and cracking.

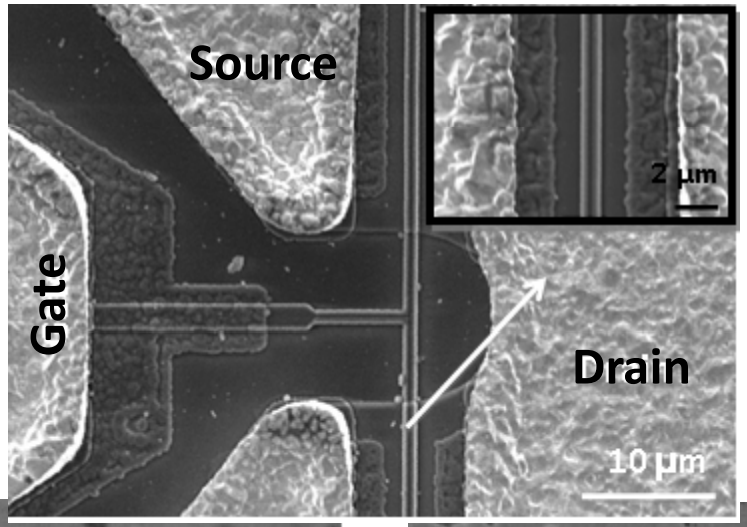
Plan View Approach

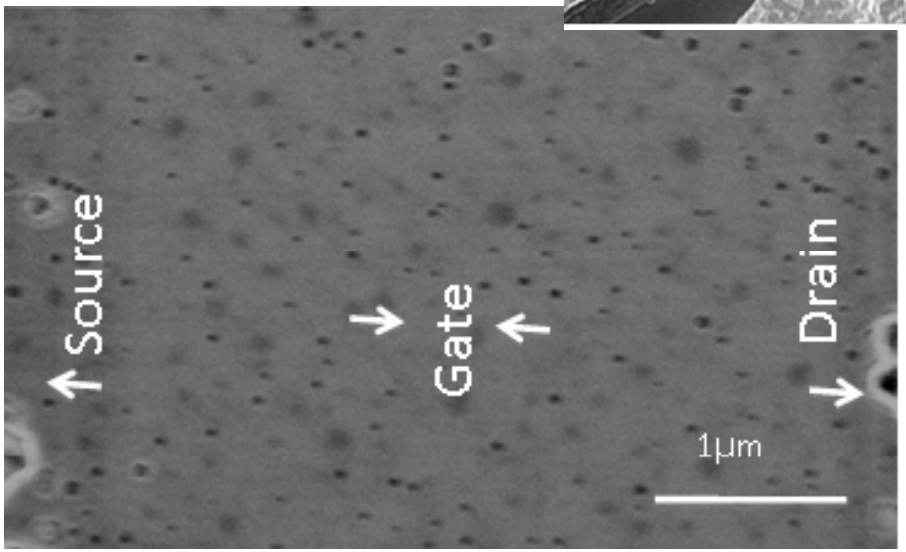
- Limitation of TEM: costly, extremely local



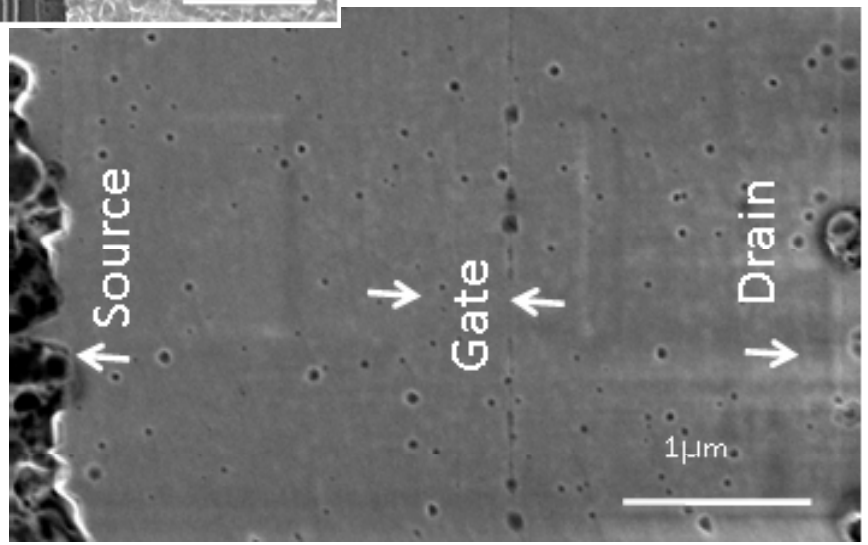
- This work:
  - Removal of SiN passivation and gate
    - SiN passivation: HF etch (1:10 HF: H_2O)
    - Contact and gate metals: aqua regia (3:1 HCl: HNO_3) at 80 ˚C for 20 minutes
    - Surface cleaning: piranha solution (H_2SO_4: H_2O) for 5 minutes at 115 ˚C
  - Plan view imaging through *SEM* and *AFM*

SiN and Gate Removal





Unstressed (high T storage)

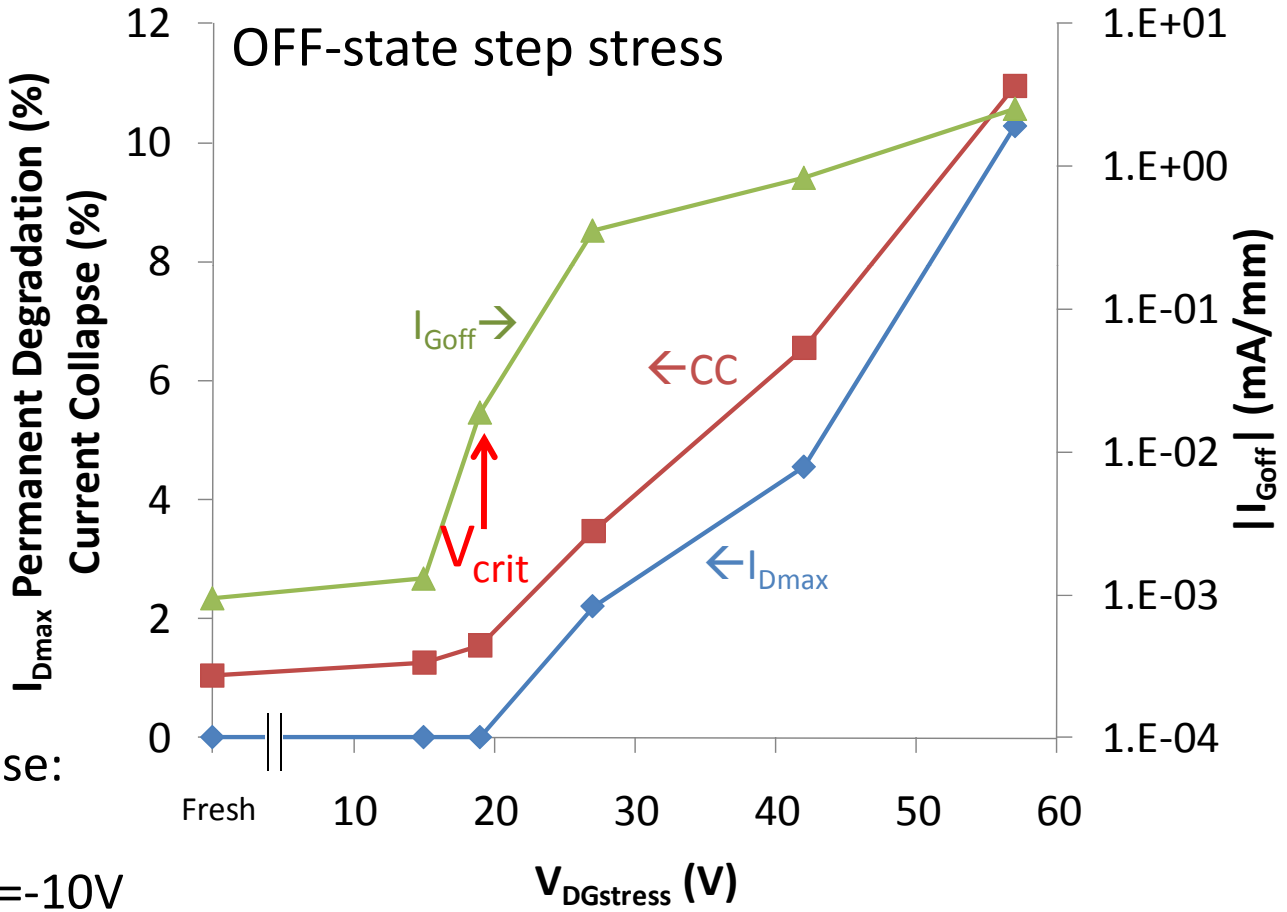


Stressed (> V_{crit})

Experimental

- OFF-state step stress
  - V_{GS}=-7 V
  - V_{DS} stepped from 5 to 8, 12, 20, 35, 50 V (1V/min)
  - T_{base}=150C
- Detailed device characterization:
  - DC device parameters: I_{Dmax}, R_S, R_D, V_T…
  - Trap characterization: current collapse
- Removal of passivation and gate metal
- SEM and AFM plan view imaging

Electrical Degradation



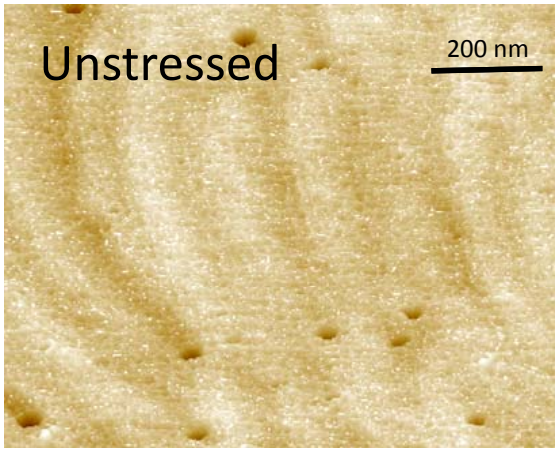
Current collapse:

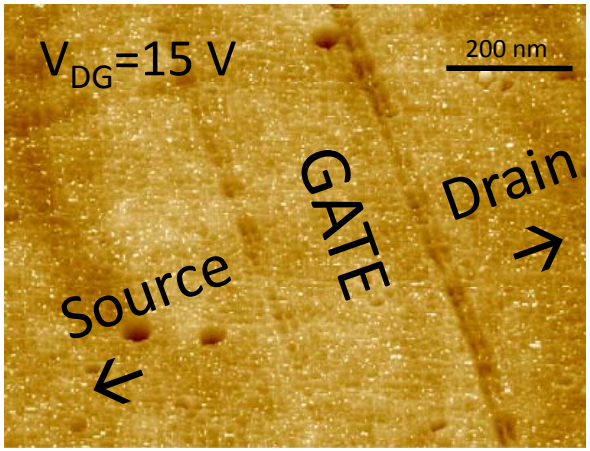
1s pulse

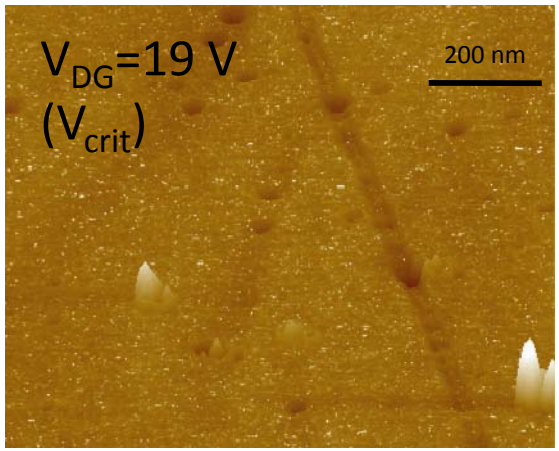
V_{DS}=0, V_{GS}=-10V

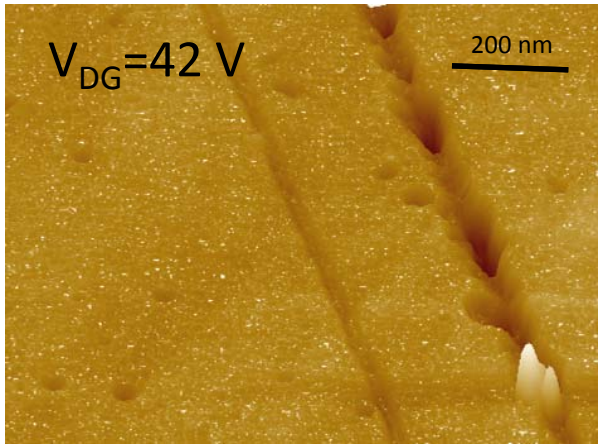
Typical critical behavior beyond 19 V

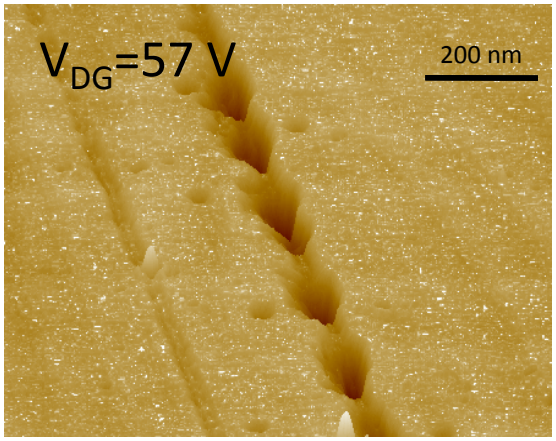
Structural Degradation







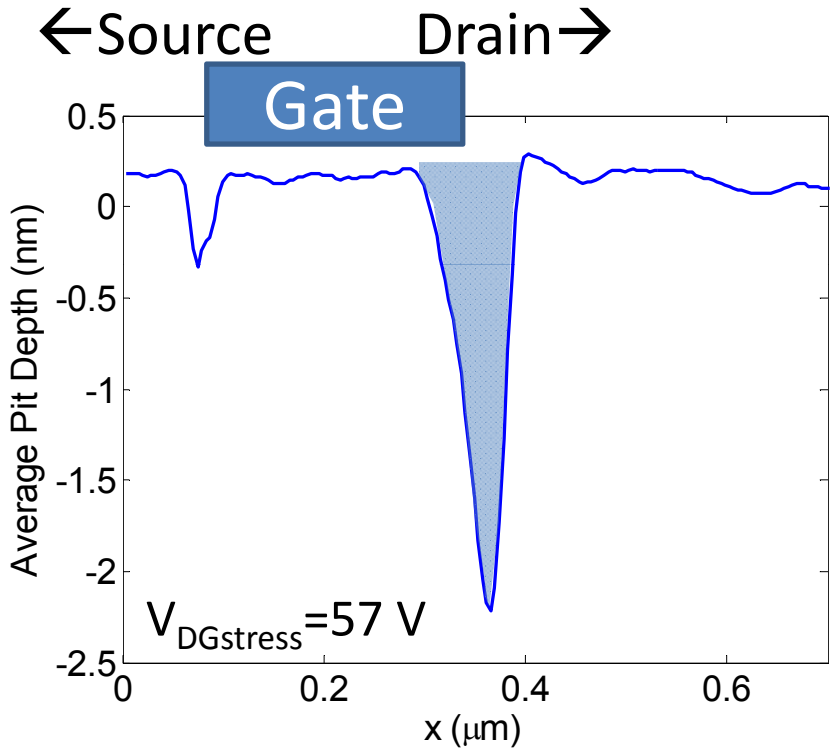


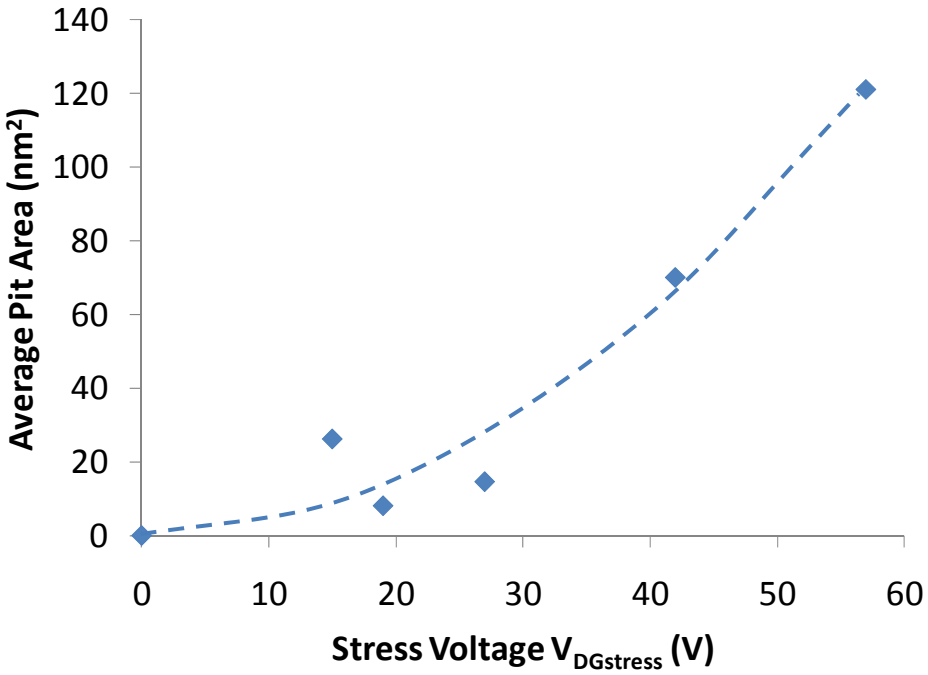


Initial continuous groove formation

Deeper pit formation along the groove

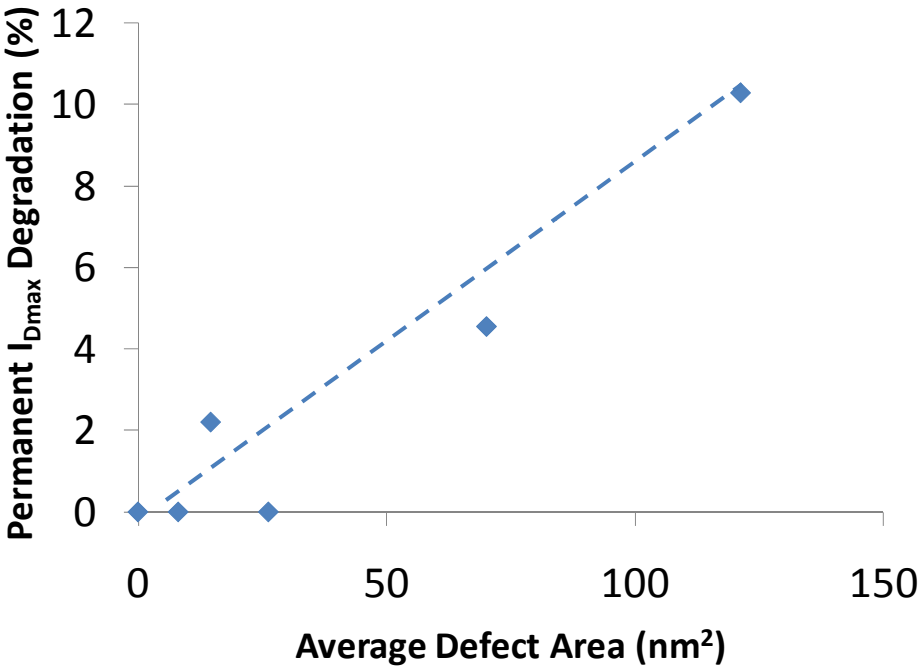
Pit Cross Section Area

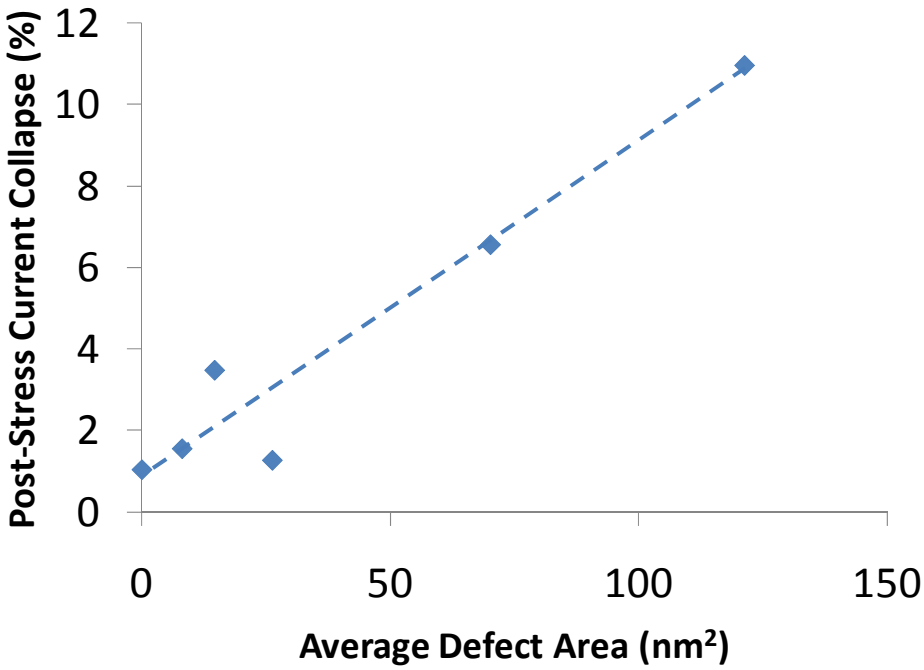




Drain side pit area also shows critical behavior.

Correlation between Electrical and Structural Degradation

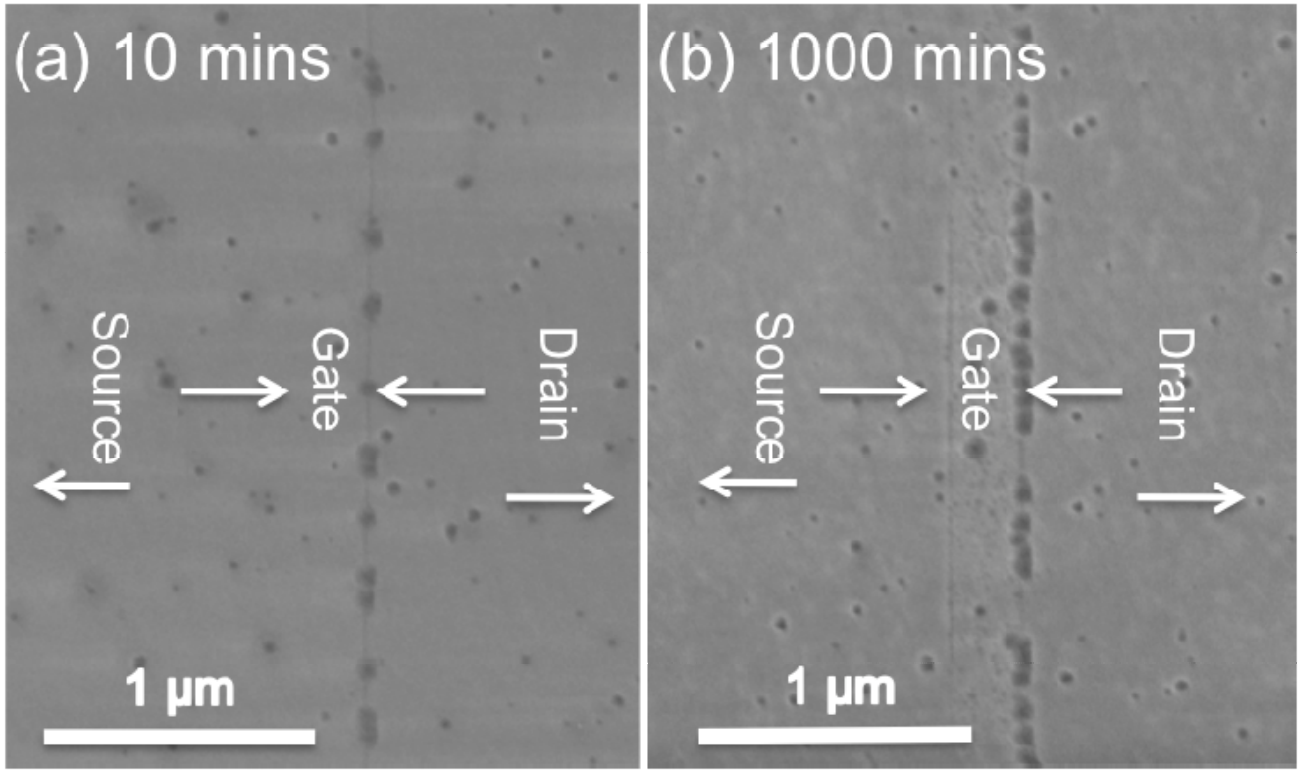




Good correlation between electrical degradation and pit area

Time Evolution

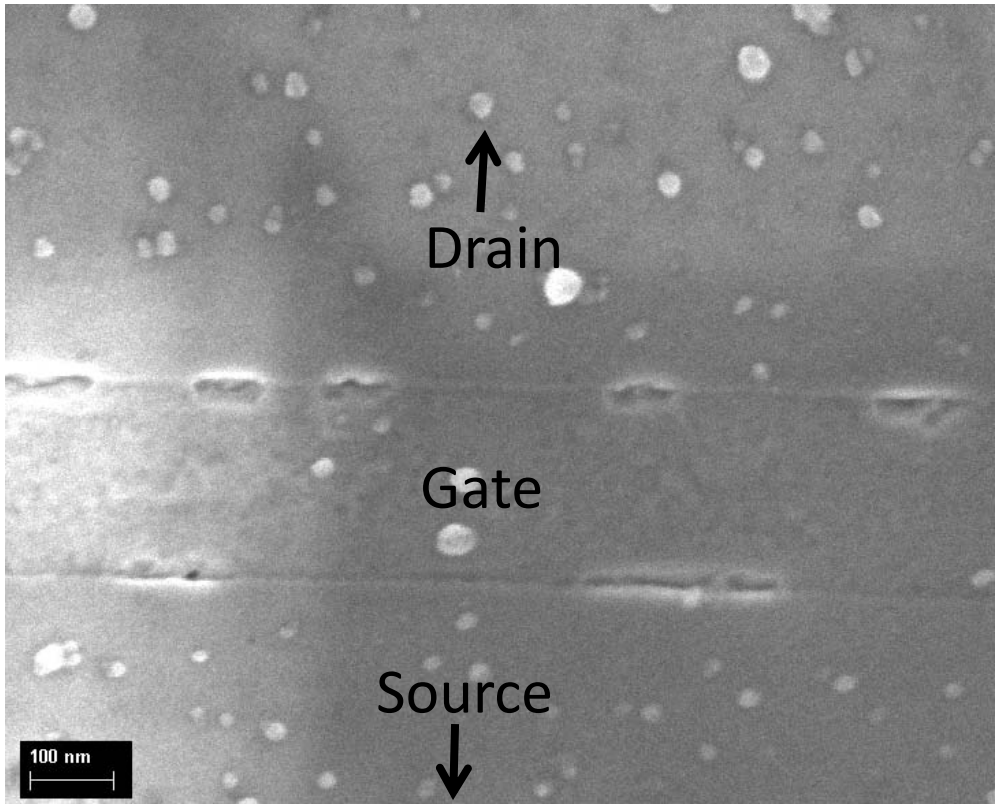
OFF-state stress $V_{DGstress}$=50 V (>V_{crit}), T_{base}=150 C



Source side groove formation

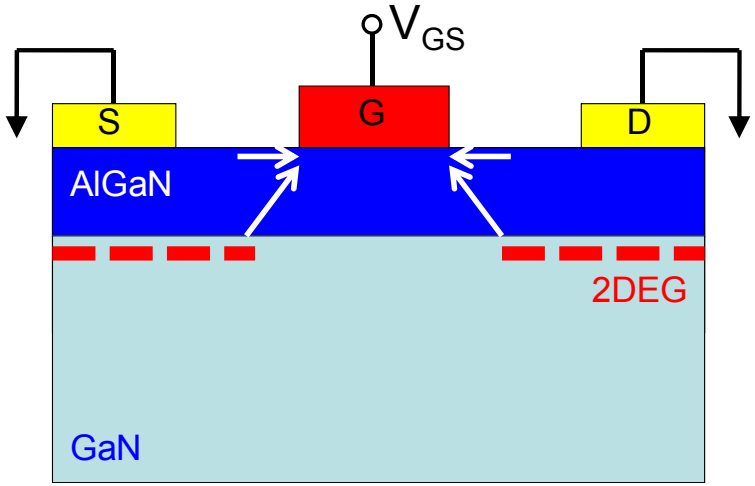
Pits grow in density and merge with each other.

Symmetric Stress (V_{DS}=0)



Stress conditions:

- V_{DS}=0, V_{GS}=-50 V
  (stressed on both sides)
- 40 min.
- Room temperature



Grooves and pits on both sides of the gate

Degradation Mechanisms

- Consistent observation in TEM and plan-view
  - Grooves and pits are not by-product of etching
- Groove formation
  - Field induced oxidation?
  - Electrochemical etching?
- Pit formation
  - Degradation is E-field driven (Little current is needed)
  - Field/stress induced diffusion of material away from gate?
- In any event, mass transport is involved.

Summary

- Developed a simple process for plan-view assessment of structural degradation
- Evolution of structural damage:
  - Below V_{crit}: shallow continuous groove formation at gate edge
  - Above V_{crit}: local pit formation along the groove
  - Number of pits increases with V_{stress} and time and pits merge
- Field induced mass transport is involved in GaN HEMT degradation