Formation of Structural Defects in AlGaN/GaN High Electron Mobility Transistors under Electrical Stress

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Gallium nitride (GaN) based devices are of interest for a variety of radar and communication applications due to their ability to operate at high-power and high frequency. We have previously carried out extensive electrical reliability characterization of AlGaN/GaN high electron mobility transistors (HEMTs) and found that degradation is driven by electric field [1-2]. High-voltage stress results in an increase in off-state gate current, I_{Goff} and drain resistance, R_D, along with a decrease in maximum drain current, I_{Dmax} [1]. Transmission electron microscope (TEM) cross sectional image has shown that electrical degradation is closely related to structural damage in the GaN cap and AlGaN barrier layers [3]. Although the TEM analysis shows a detailed cross section of the defect area, it is an extremely localized technique. In order to better understand the structural degradation of AlGaN/GaN HEMTs under electrical stress, a planar view of defect formation is required.

In this work, we study plane view structural degradation of AlGaN/GaN HEMTs after electrical stress by removing the SiN passivation layer and all the metals from the sample. We then use atomic force microscope (AFM) and scanning electron microscope (SEM) to image the semiconductor surface.

In a series of OFF state (low I_D, high V_{DS}) experiments, identical devices were step-stressed up to various V_{DG}'s from 15 to 57 V at 150 C of base plate temperature. The critical voltage V_{crit} for which a sharp increase of gate current occurs [2] was determined to be around 20 V for this condition. For $V_{stress}>V_{crit}$, significant permanent decrease in I_{Dmax} of up to 10% as well as a large increase in current collapse took place. While the surface of a non-stressed device was found to be smooth after gate removal, AFM images of stressed devices revealed that a line-shaped indentation developed along the gate edge on the drain side for all stressed devices. For devices stressed at high voltage, the same feature, but more shallow, was found on the source side as well. In addition, beyond the critical voltage we observed nanopipe or pit formation at the drain side edge of the gate. These pits grow in density and size along the gate as the stress voltage increases.

In order to understand time evolution of these crystallographic defects, we have also performed OFF-state stress tests at V_{DG}=50 V. Two devices were stressed for 10 and 1000 minutes, respectively. We observe that as the device is stressed for longer times, the pits grow and merge to form a continuous defective region along the gate finger.

This represents the first planar view of structural defects in electrically stressed GaN HEMTs. The methodology described here will enable better understanding of the evolution of defect formation under various electrical stress conditions.

[1] Joh, *IEEE IEDM Tech. Digest*, pp. 415-418, 2006.
[2] Joh, *IEEE Electron Dev. Lett.*, vol. 29, pp. 287-289, 2008.
[3] Chowdhury, *IEEE Electron Dev. Lett.*, vol. 29, pp. 1098-1100, 2008.

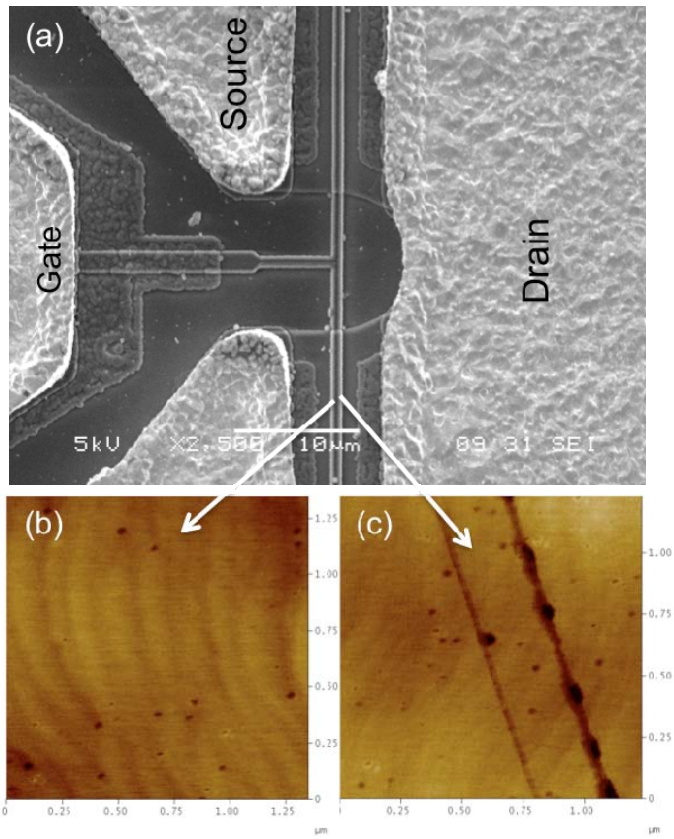

Figure 1: (a) SEM image of the device before metal removal. AFM image after gate metal removal of (b) untested device (c) device stressed at V_{DG}= 57 V.

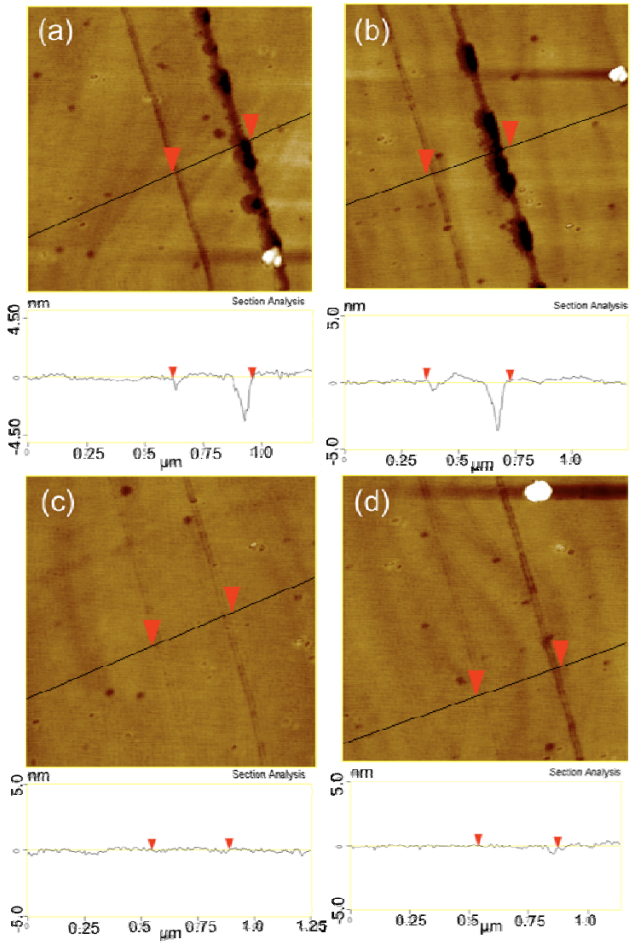

Figure 2: AFM images of a device stressed at (a) V_{DG} =57 V, (b) V_{DG}=35 V, (c) at V_{DG}= 20V, and (d) V_{DG}= 15V (at below V_{crit}).

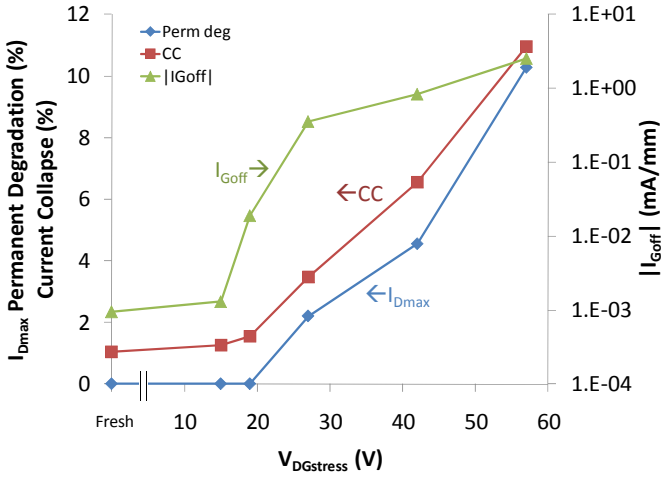

Figure 3: Selected transistor figures of merit at the end of the step-stress experiments as a function of the maximum stress. [OFF state, T_{base} = 150° C]

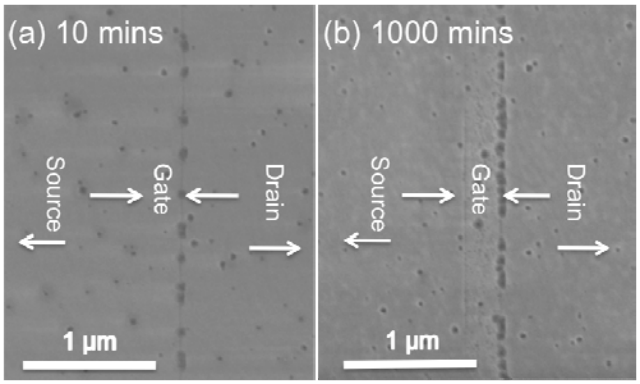

Figure 4: SEM micrograph of devices stressed at V_{DG} = 50 V for (a) 10 and (b) 1000 minutes.