10 nm CMOS: The Prospects for III-Vs

J. A. del Alamo, Dae-Hyun Kim[1], Donghyun Jin, and Taewoo Kim

Microsystems Technology Laboratories, MIT

[1]Presently with Teledyne Scientific

2010 European Materials Research Society Spring Meeting

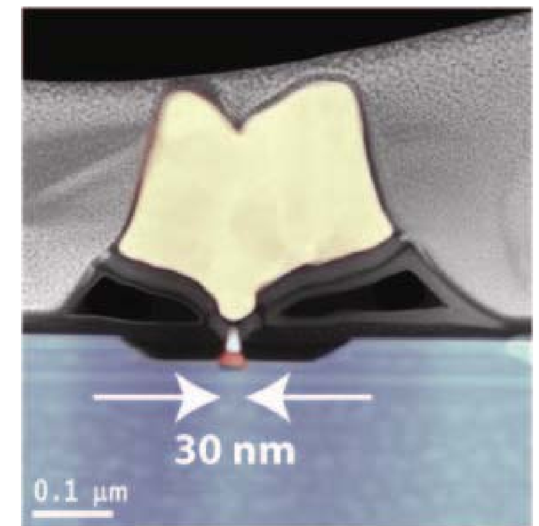
June 7-10, 2010

Sponsors: Intel, FCRP-MSD

Acknowledgements:

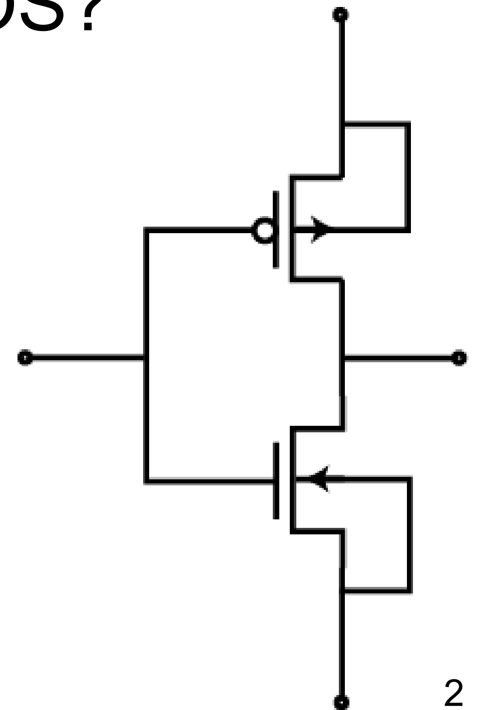
Niamh Waldron, Ling Xia, Dimitri Antoniadis, Robert Chau

MTL, NSL, SEBL



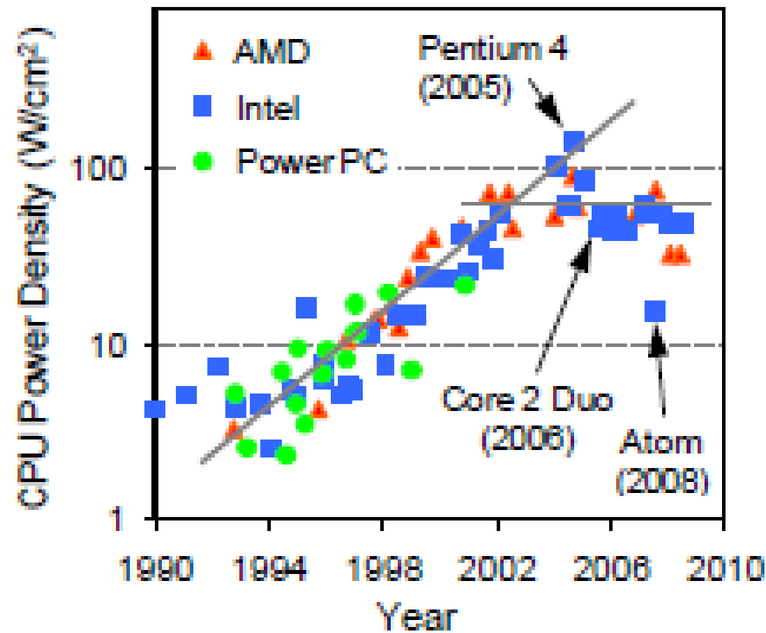
Outline

- Introduction: Why III-Vs for CMOS?
- What have we learned from III-V HEMTs?
- What are the challenges for III-V CMOS?
- The prospects of 10 nm III-V CMOS
- Conclusions

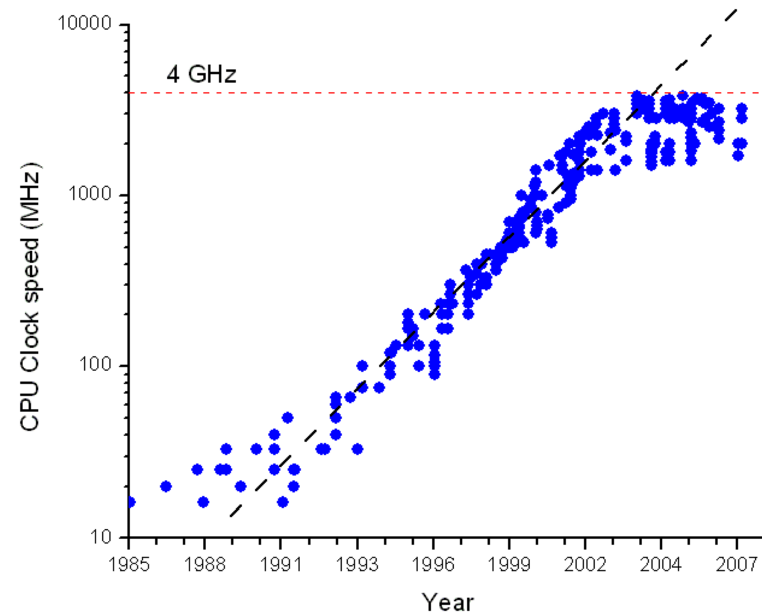


Why III-Vs for CMOS?

- Si CMOS has entered era of *"power-constrained scaling"*:
  - CPU power density saturated at ~100 W/cm^2
  - CPU clock speed saturated at ~ 4 GHz



Pop, Nano Res 2010



http://www.chem.utoronto.ca/~nlipkowi/pictures/clockspeeds.gif

Why III-Vs for CMOS?

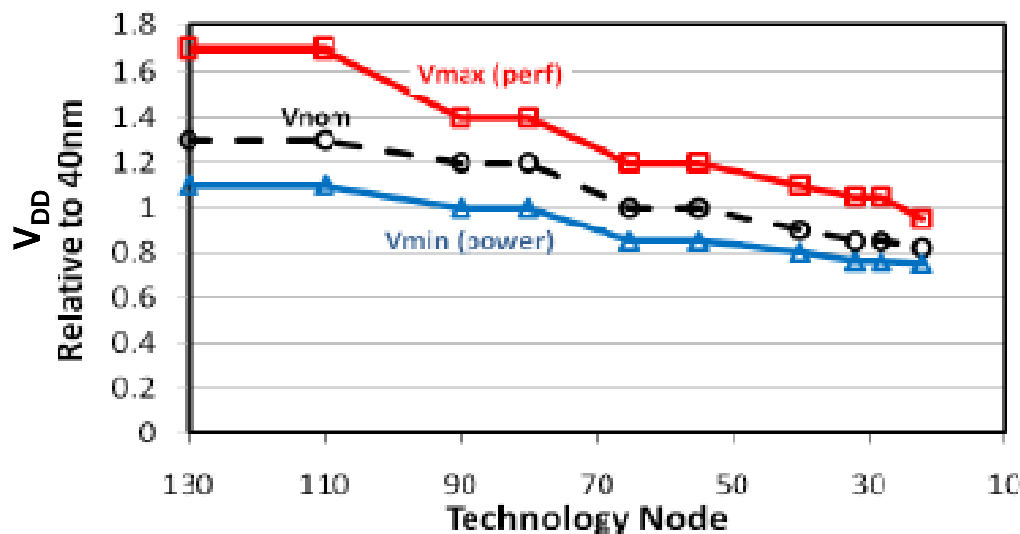
- Under power-constrained scaling:

$$\text{Power} = \text{active power} + \text{passive power}$$

$$\sim f\,C V_{DD}^2 N \Rightarrow N\uparrow \rightarrow V_{DD}\downarrow$$

#1 goal

- But, V_{DD} scaling very weakly:



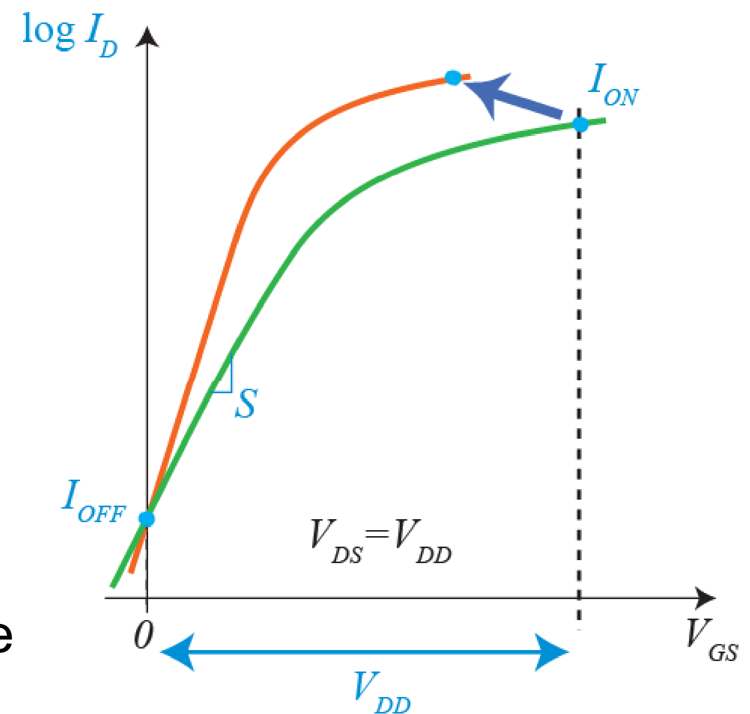
Chen, IEDM 2009

Why III-Vs for CMOS?

- Need scaling approach that allows V_{DD} reduction

- Goal of scaling:
  - reduce footprint
  - extract maximum I_{ON} for given I_{OFF}

- III-Vs:
  - Much higher injection velocity than Si
    → I_{ON} ↑
  - Very tight carrier confinement possible
    → S↓



III-V CMOS: What are the challenges?

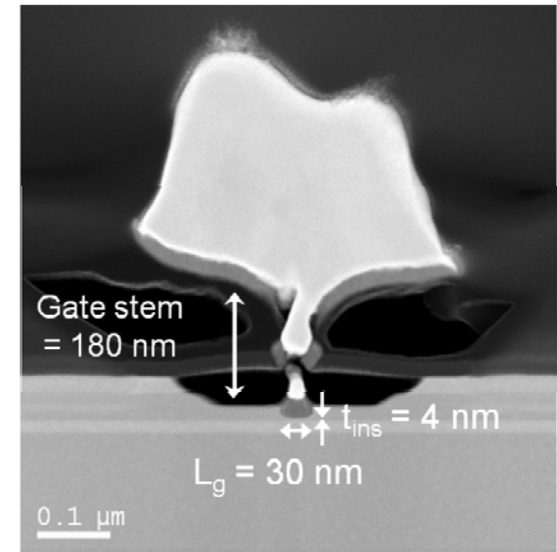
"To know where you are going, you first have to know where you are."

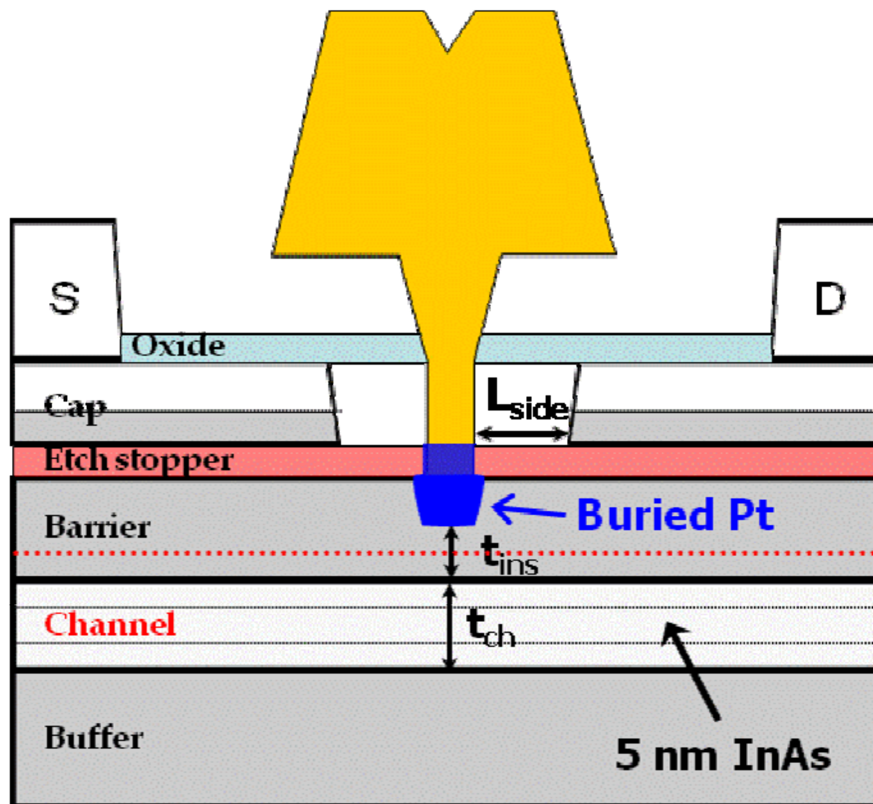
→We are starting from:

III-V High Electron Mobility Transistors

III-V HEMTs

- State-of-the-art: InAs-channel HEMT





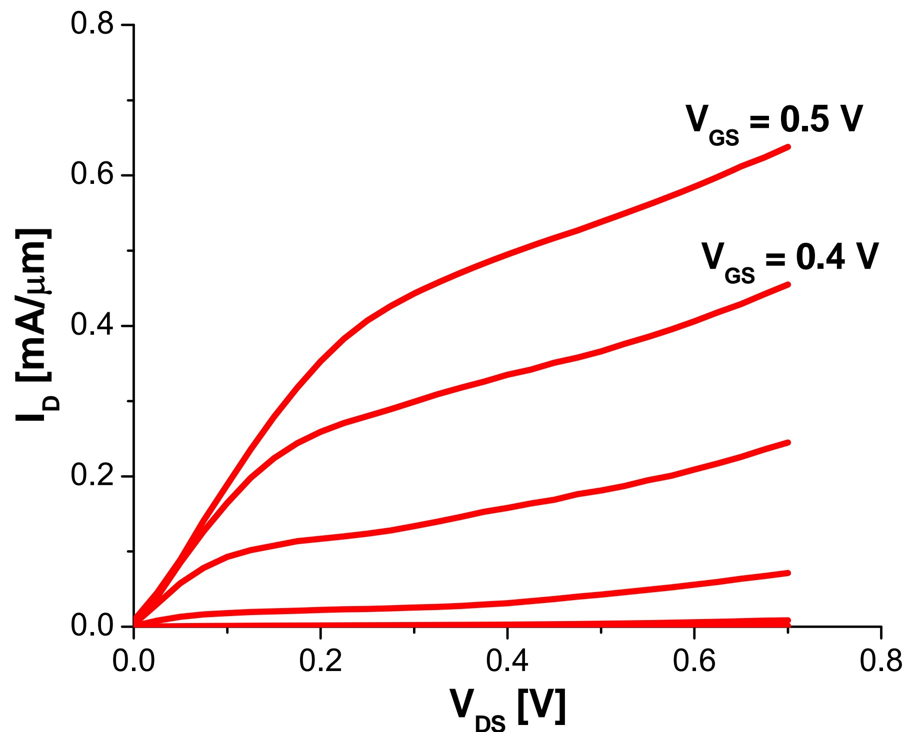
- QW channel (t_{ch} = 10 nm) :
  - InAs core (t_{InAs} = 5 nm)
  - InGaAs cladding
- $\mu_{n,Hall}$ = 13,200 cm^2/V-sec
- InAlAs barrier (t_{ins} = 4 nm)
- Two-step recess
- Pt/Ti/Mo/Au Schottky gate
- L_g=30 nm

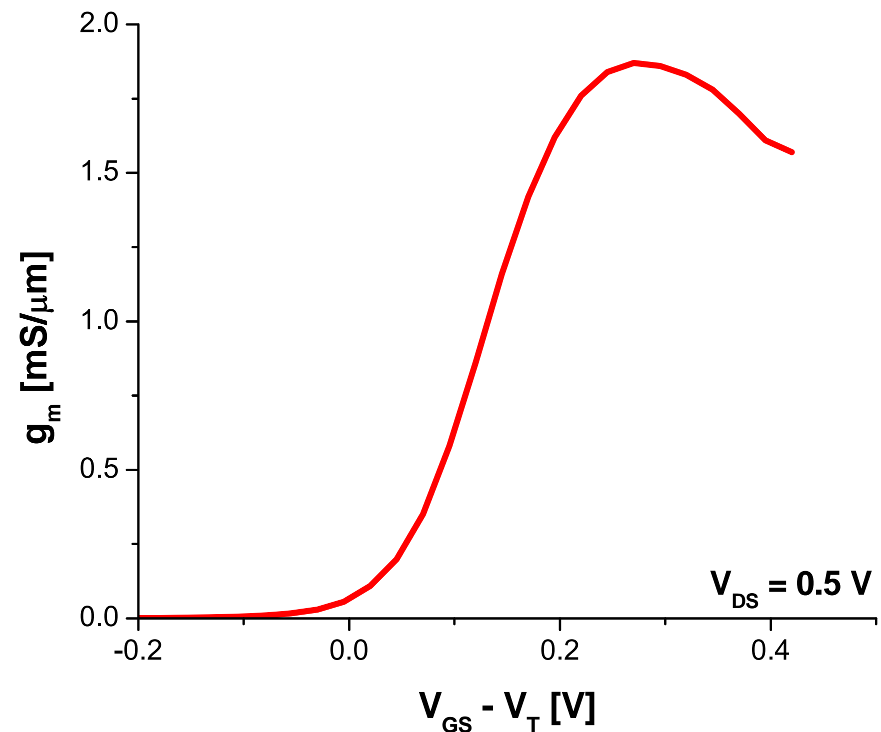
Kim, IEDM 2008

III-V HEMTs

- L_g=30 nm InAs-channel HEMT

Kim, IEDM 2008

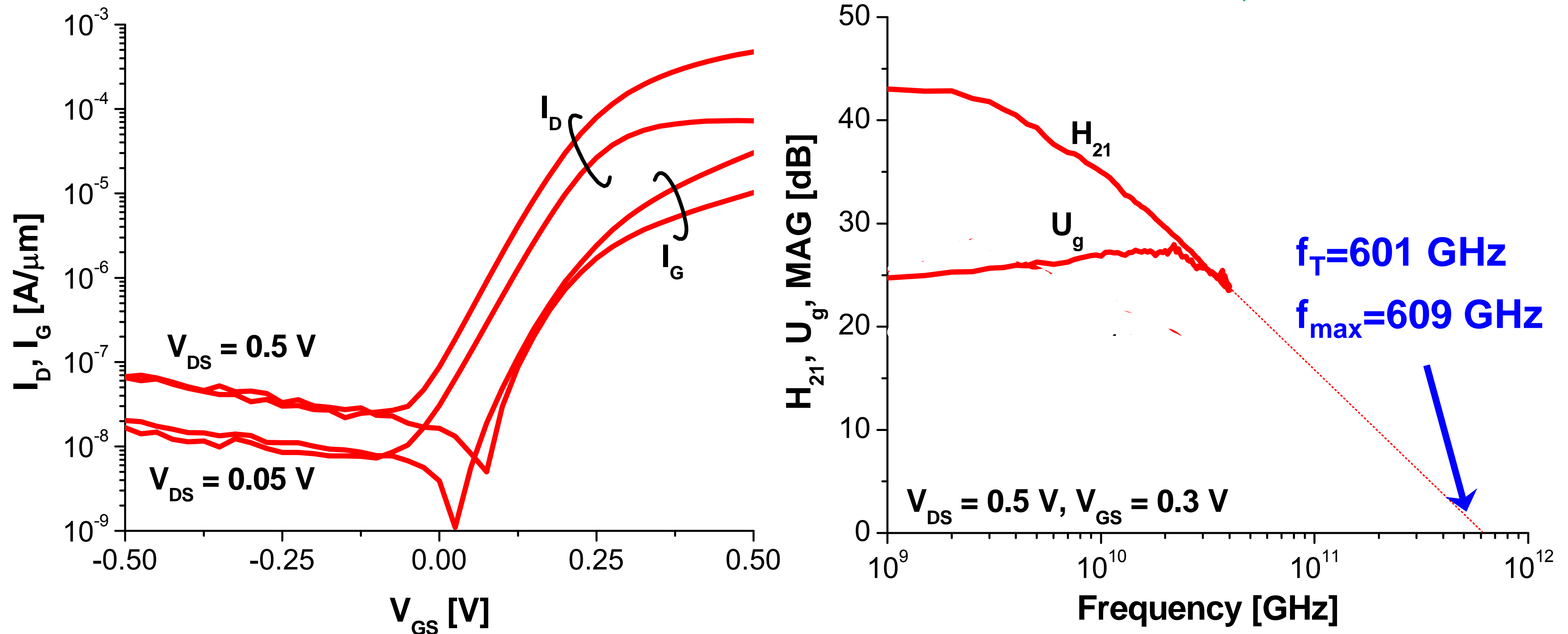




- Large current drive: I_{on}=0.4 mA/μm at V_{DD}=0.5 V
- Enhancement-mode FET: V_T = 0.08 V
- High transconductance: g_{mpk}= 1.8 mS/um at V_{DD}=0.5 V

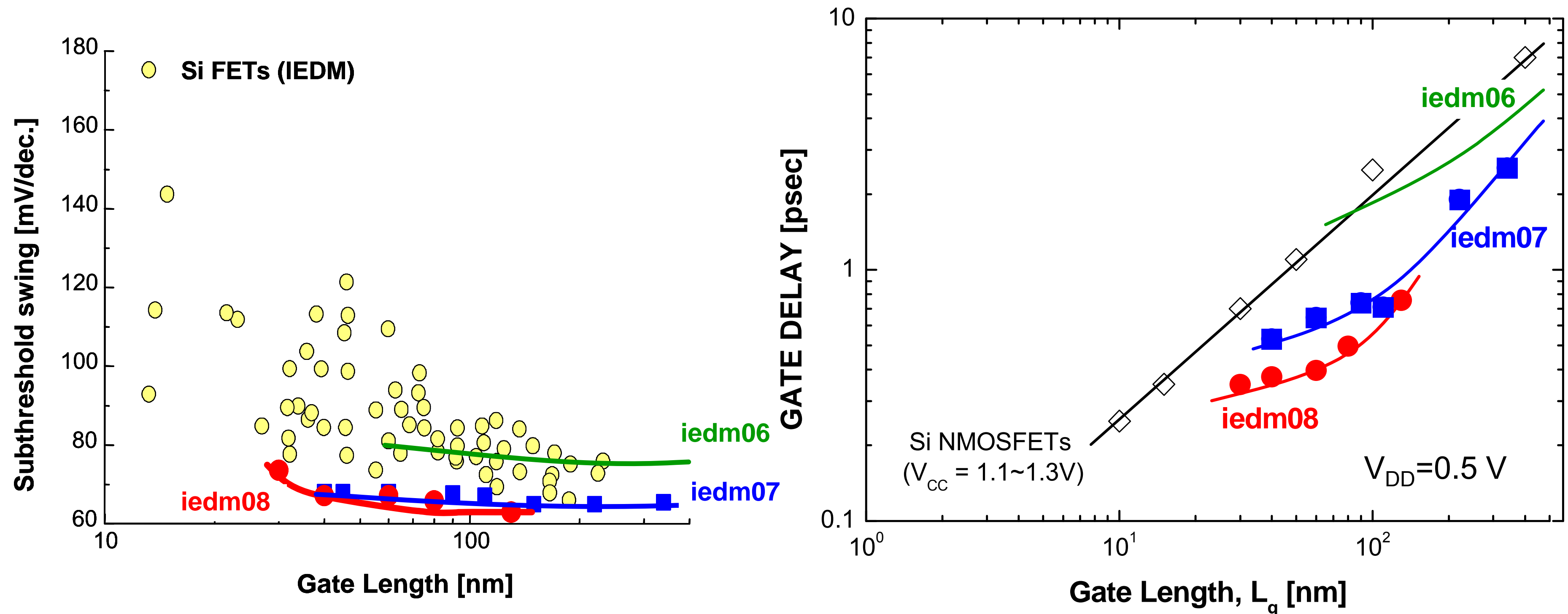
III-V HEMTs

- L_g=30 nm InAs-channel HEMT



- S = 73 mV/dec, DIBL = 85 mV/V, I_{on}/I_{off}=~10^4
- First transistor with both f_T and f_{max} > 600 GHz

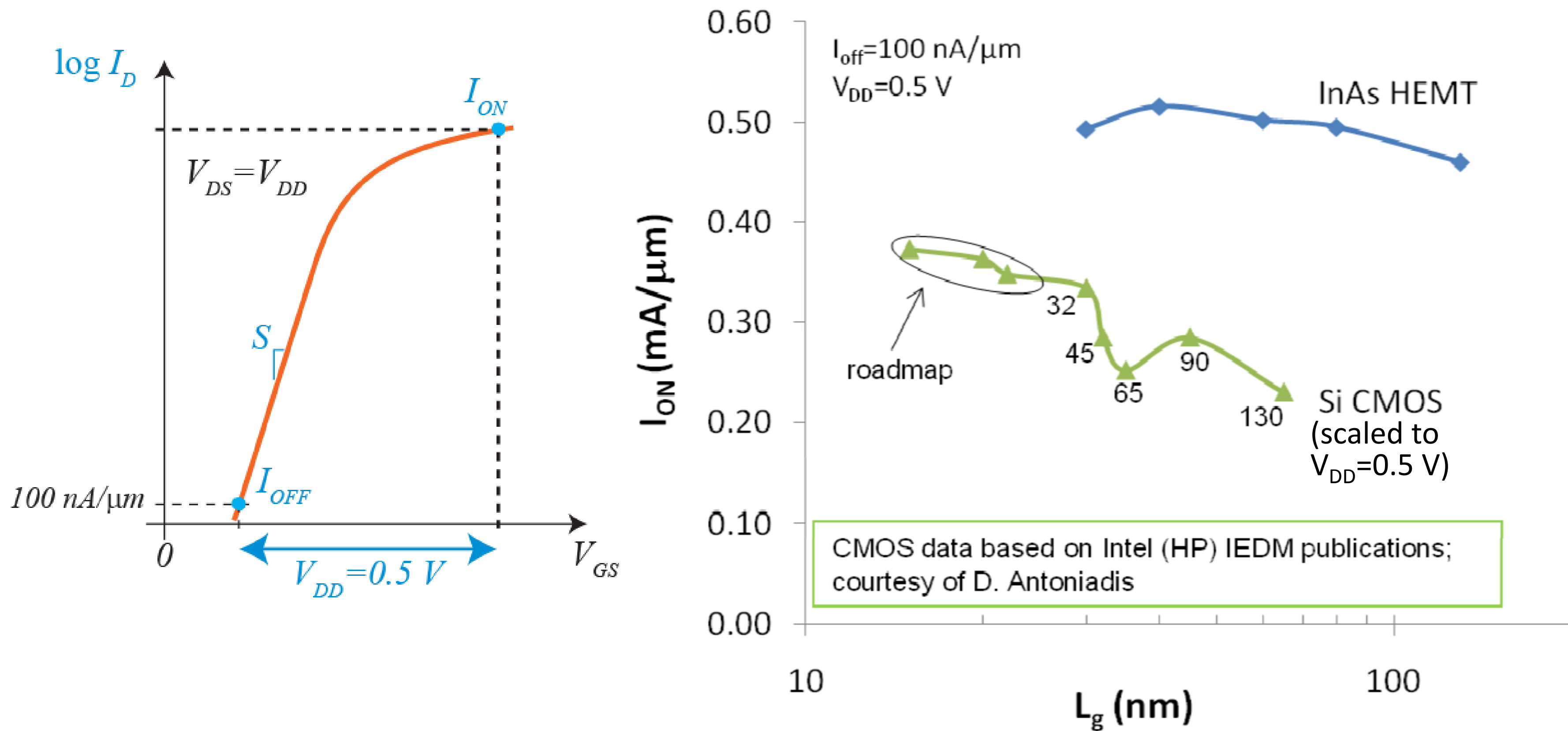
Scaling of III-V HEMTs: Benchmarking with Si



- Superior short-channel effects as compared to Si MOSFETs
- Lower gate delay than Si MOSFETs at lower V_{DD}

Scaling of III-V HEMTs: Benchmarking with Si

- I_{ON} @ I_{OFF}=100 nA/μm, V_{DD}=0.5 V: FOM that integrates short-channel effects and drive current

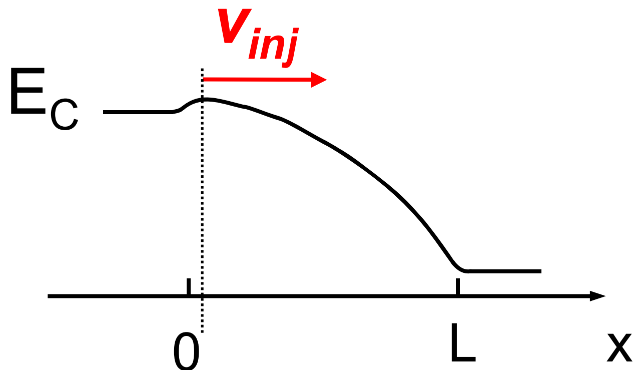


III-V HEMTs: higher I_{ON} for same I_{OFF} than Si

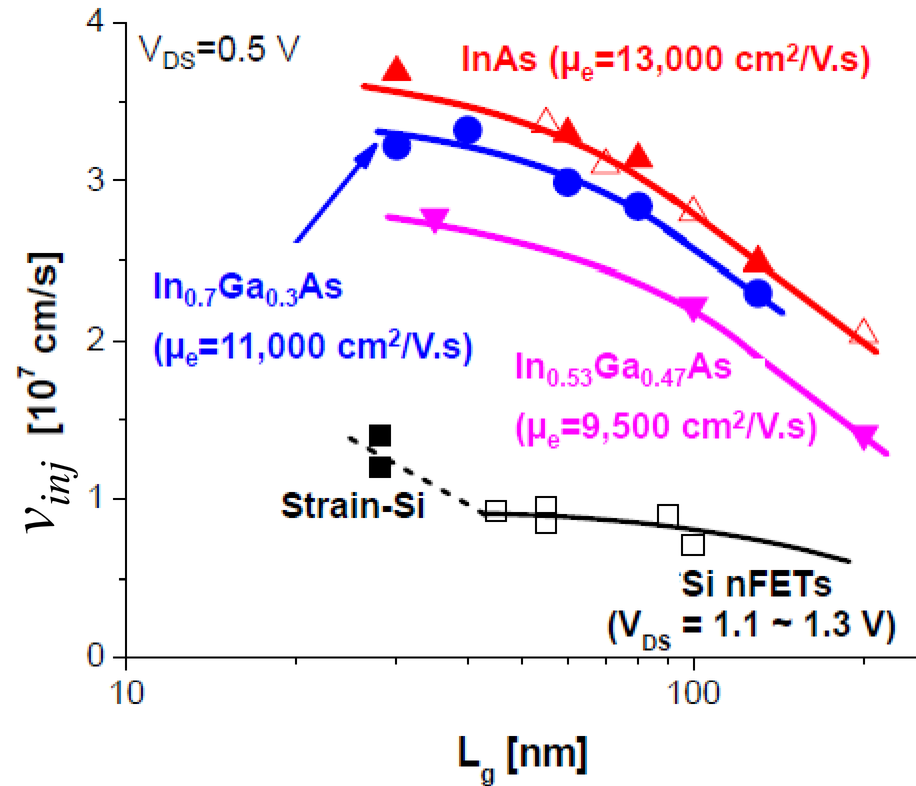
What can we learn from III-V HEMTs?

1. Very high electron injection velocity at the virtual source

Kim, IEDM 2009



v_{inj} ≡ electron injection velocity at virtual source

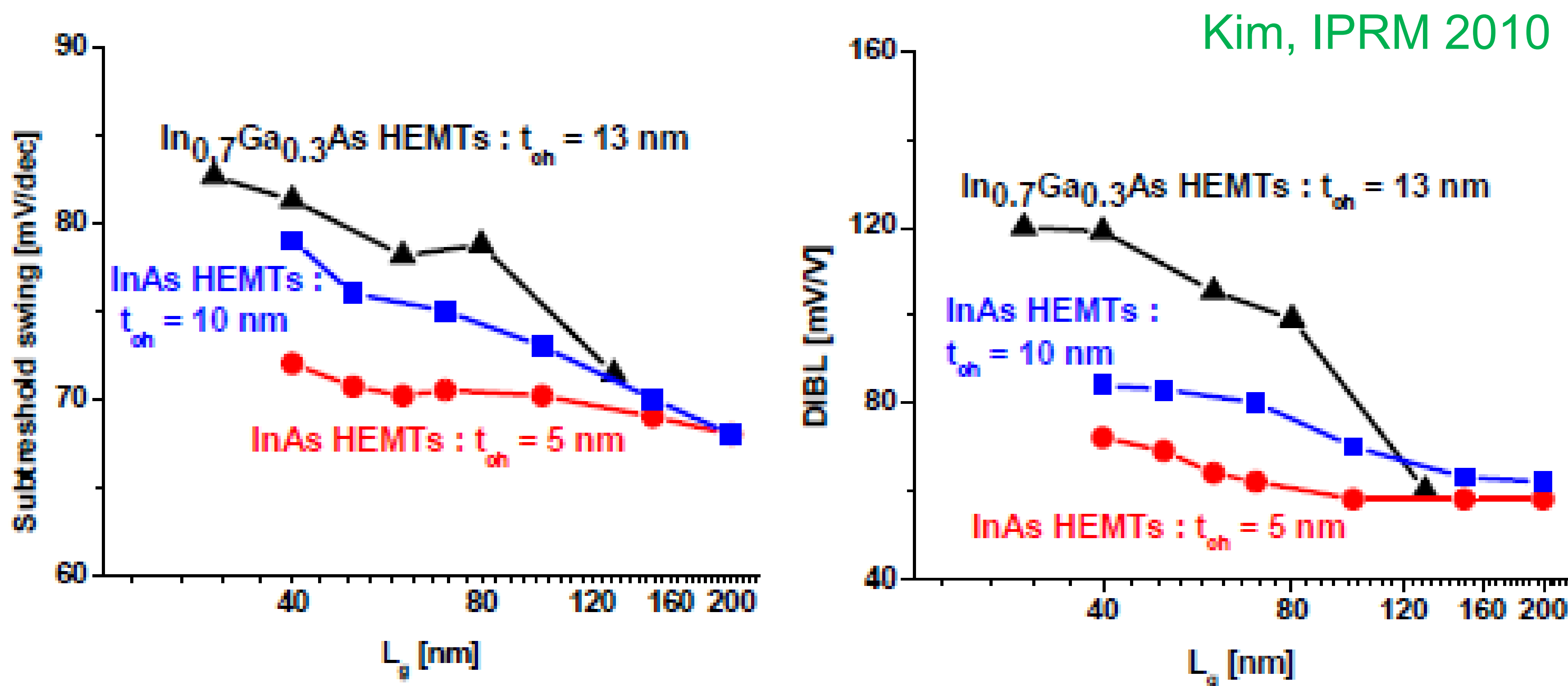


- v_{inj}(InGaAs) increases with InAs fraction in channel
- v_{inj}(InGaAs) $> 2v_{inj}$(Si) at less than half V_{DD}

What can we learn from III-V HEMTs?

2. Quantum-well channel key to outstanding short-channel effects

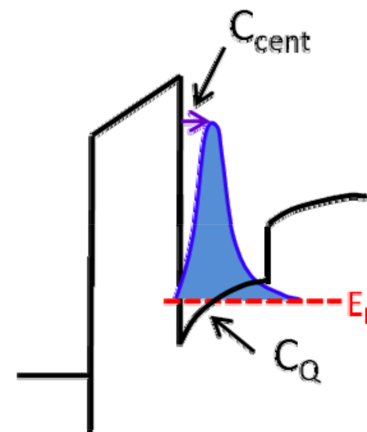
Kim, IPRM 2010



- Dramatic improvement in electrostatic integrity in thin channel devices

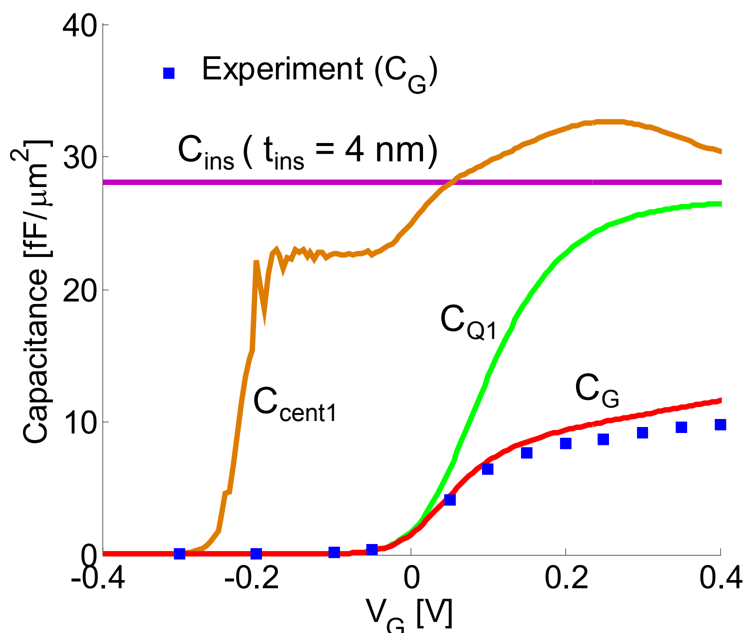
What can we learn from III-V HEMTs?

3. Quantum capacitance less of a bottleneck than commonly believed



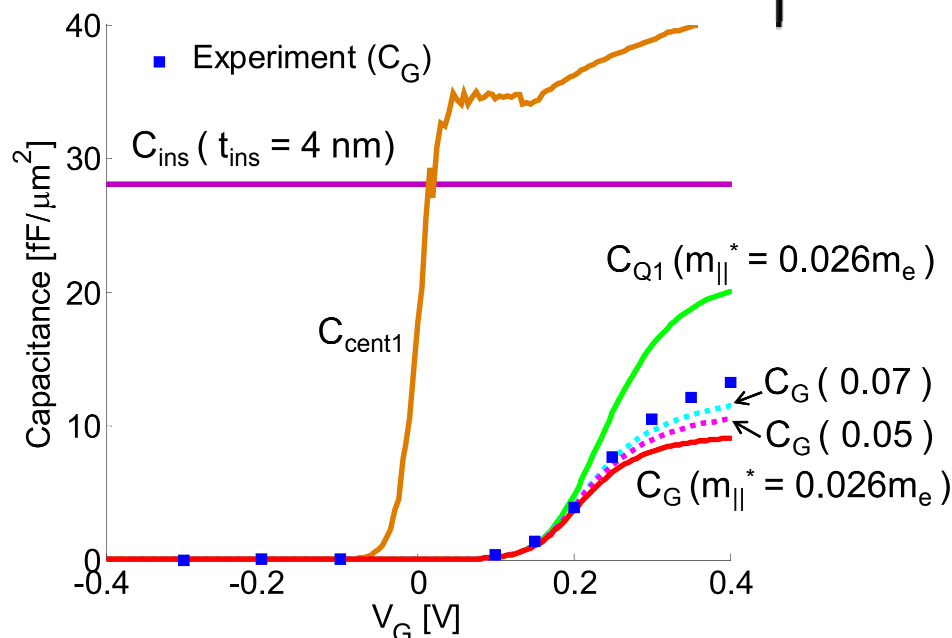
$In_{0.7}Ga_{0.3}As$ channel

t_{ch} = 13 nm



InAs channel

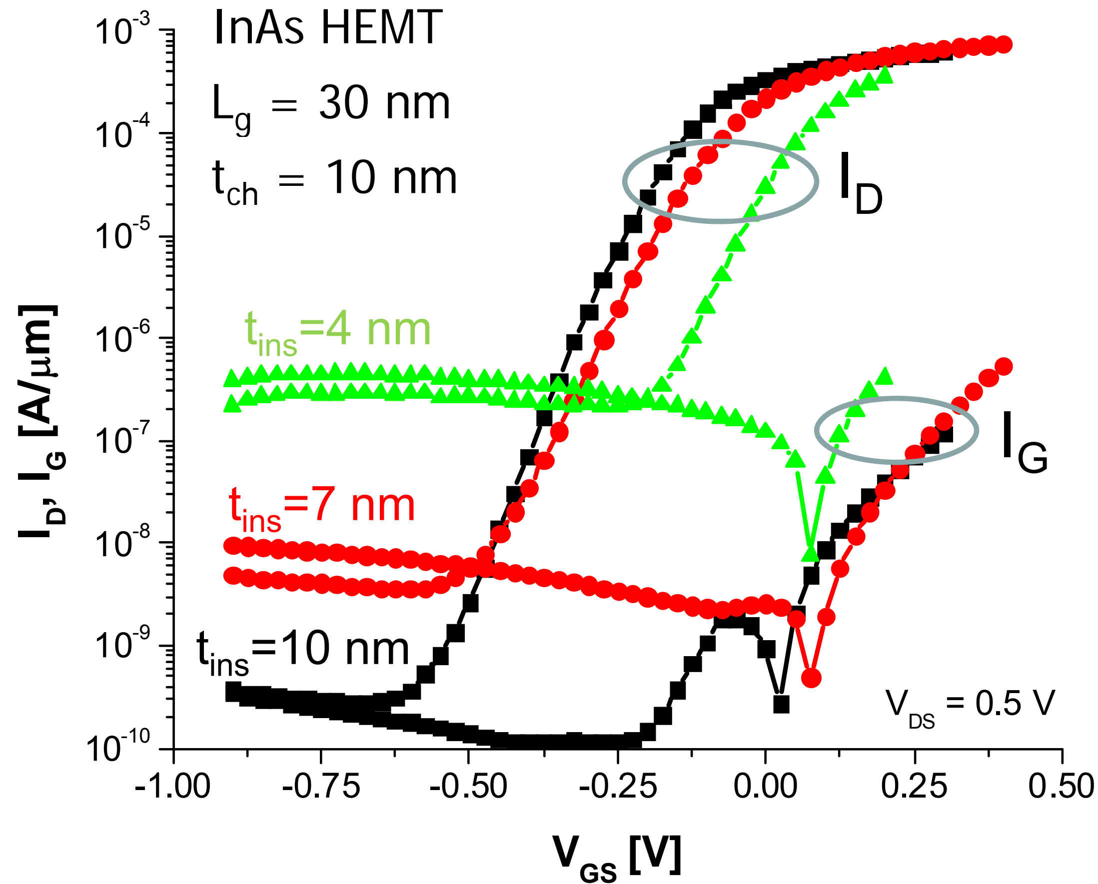
t_{ch} = 10 nm

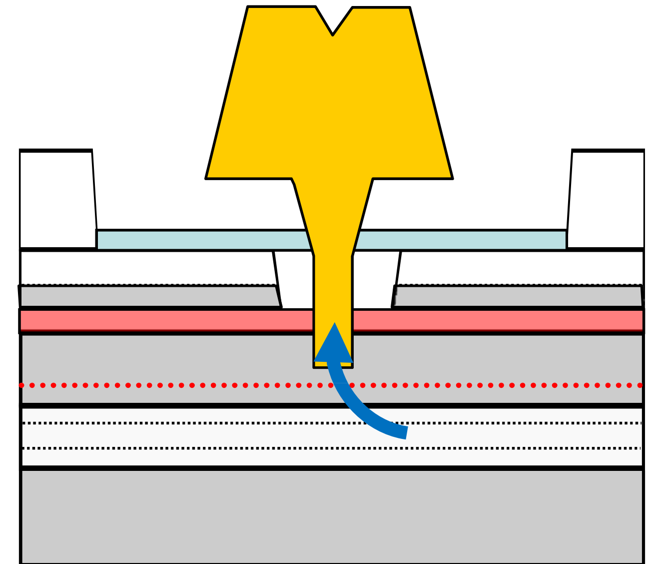


- Biaxial strain + non-parabolicity + strong quantization increase $m_{||}^*$ → C_G↑

Jin, IEDM 2009

Limit to III-V HEMT Scaling: Gate Leakage Current



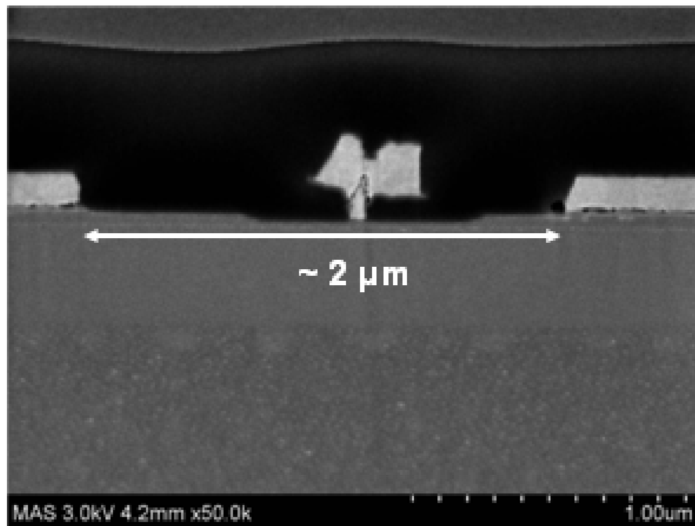


$t_{ins}\downarrow \rightarrow I_G\uparrow$

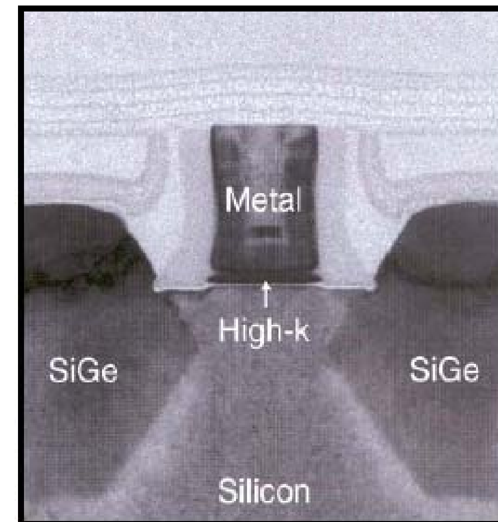
→ Further scaling requires high-K gate dielectric

The Challenges for III-V CMOS: III-V HEMT vs. Si CMOS

III-V HEMT



Intel's 45 nm CMOS

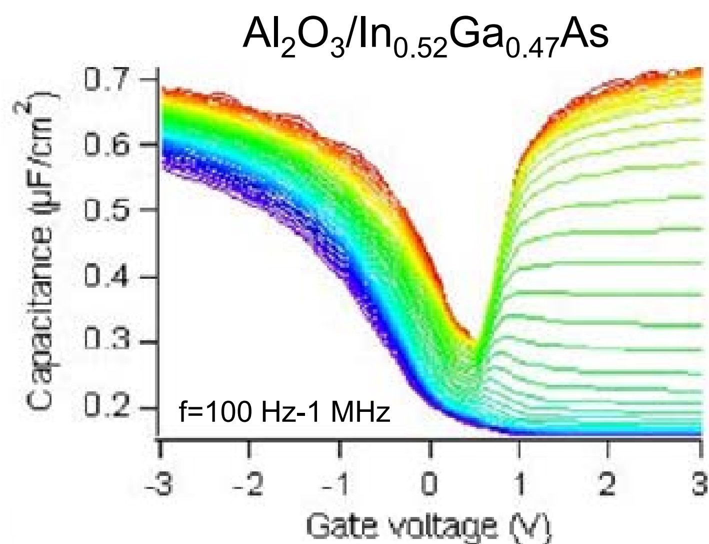


Critical issues:

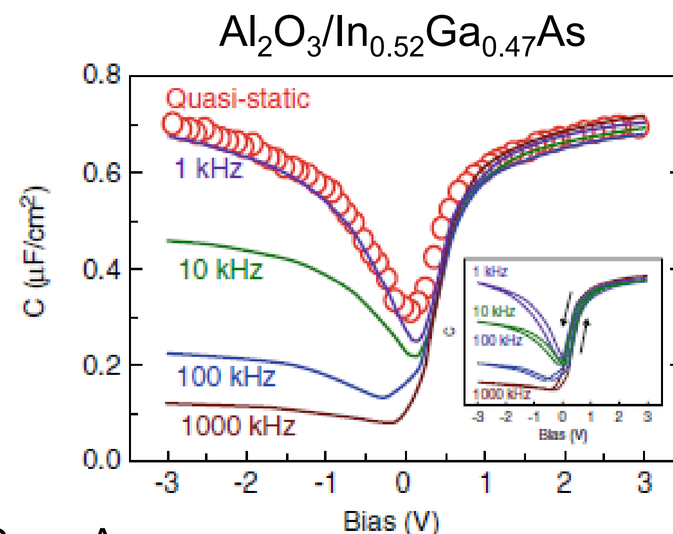
- Schottky gate → MOS gate
- Footprint scaling [1000x too big!]
- Need self-aligned contacts
- Need p-channel device
- Need III-V on Si

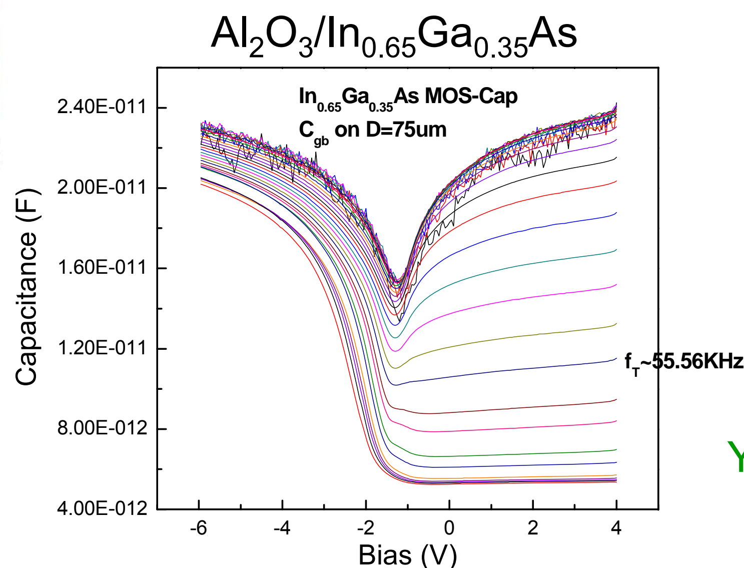
The High-K/III-V System by ALD

- *Ex-situ* ALD produces high-quality interface on InGaAs:
  - Surface inversion demonstrated
  - D_{it} in mid ~10^{11} $cm^{-2}.eV^{-1}$ demonstrated



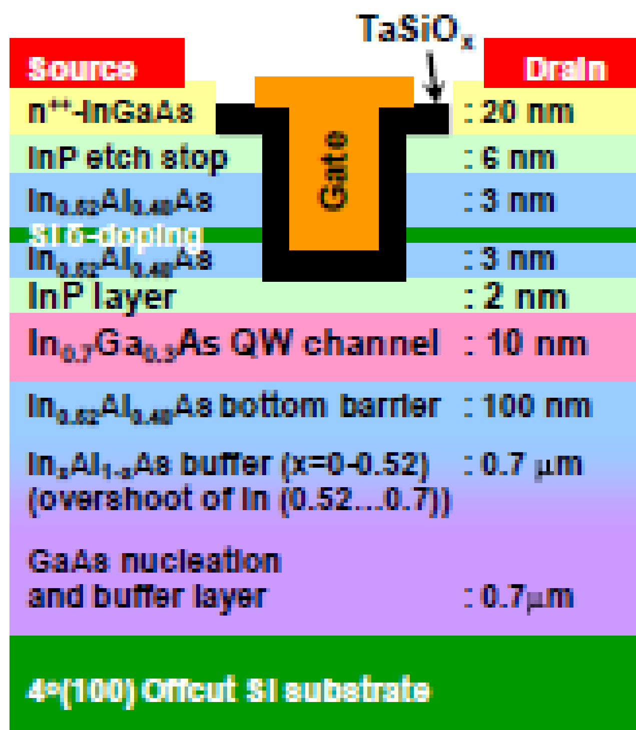
Lin, SISC 2008

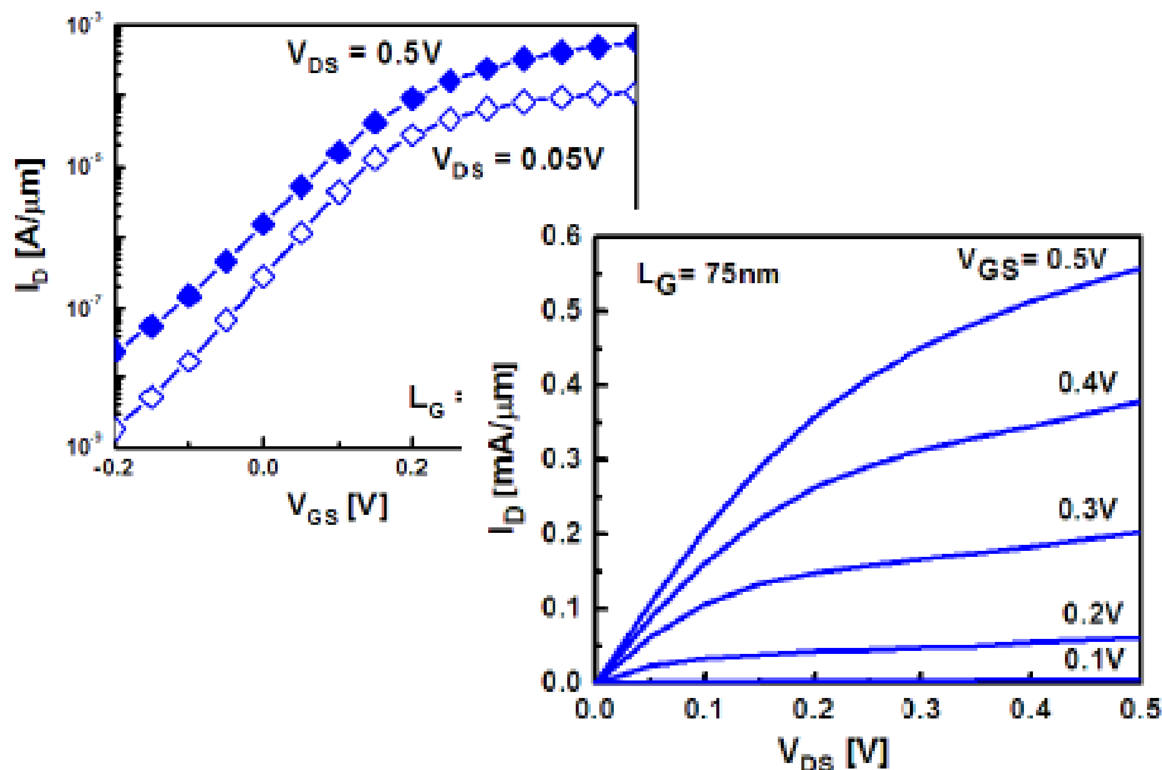




Ye, 2010

$In_{0.7}Ga_{0.3}As$ Quantum-Well MOSFET

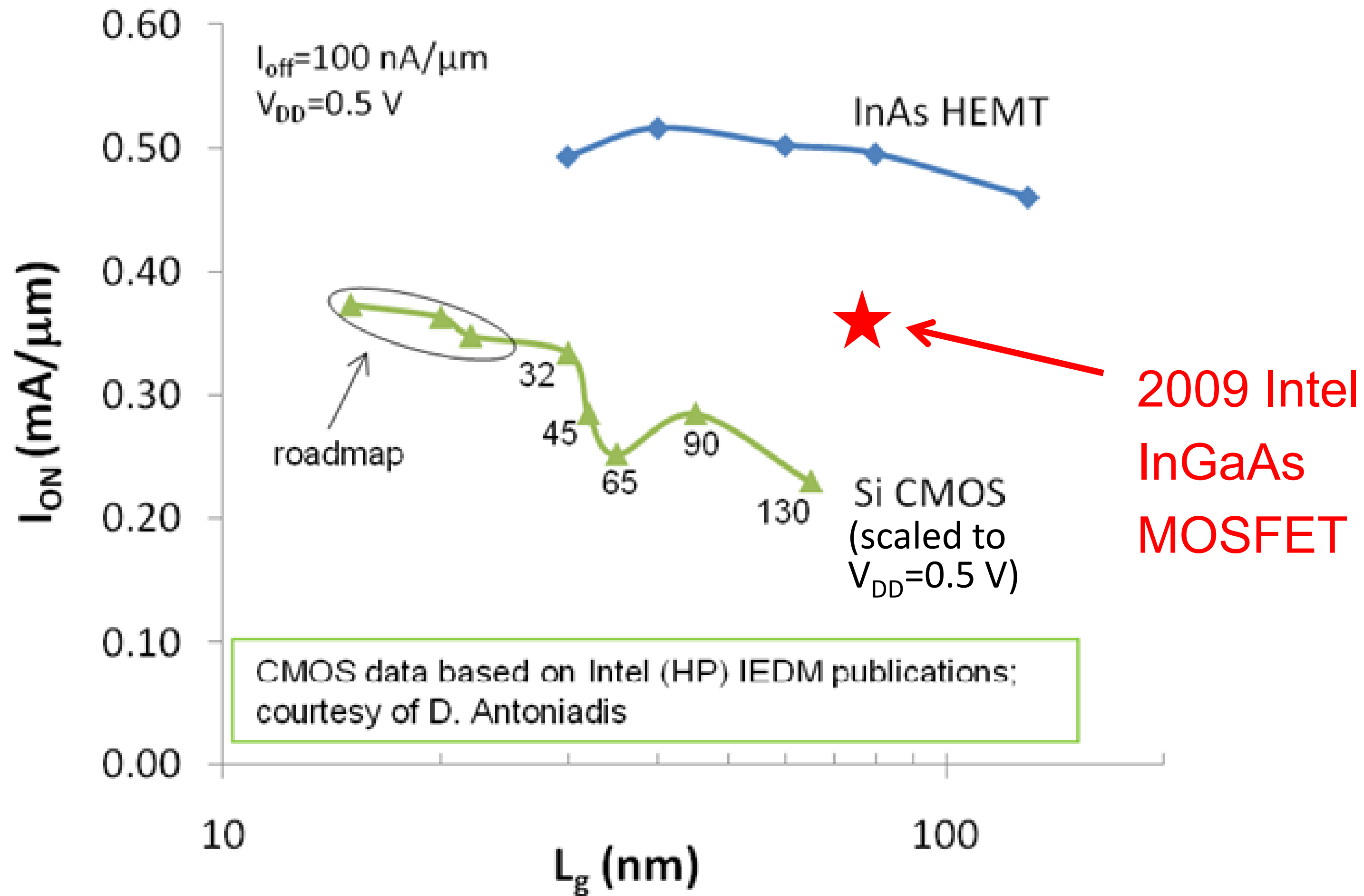




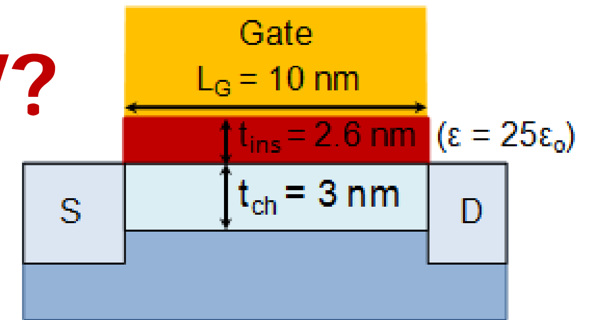
- Direct MBE on Si substrate (1.5 μm buffer thickness)
- InGaAs buried-channel MOSFET (under 2 nm InP etch stop)
- 4 nm $TaSiO_x$ gate dielectric by ALD, TiN/Pt/Au gate
- L_g=75 nm

Radosavljevic, IEDM 2009

$In_{0.7}Ga_{0.3}As$ Quantum-Well MOSFET



What can we expect from ~10 nm III-V NMOS at 0.5 V?



With thin InAs channel:

$$
\begin{aligned}
I_D &= q n_s v_{inj} \\
&= 1.6 \times 10^{-19}\ C \times \boxed{4 \times 10^{12}\ cm^{-2}} \times \boxed{3.8 \times 10^{7}\ cm/s} \\
&= 2.4\ mA/\mu m
\end{aligned}
$$

Assume R_S as in Si (~80 Ω.µm):

I_D=**1.5** *mA/µm*

Key requirements:

- High-K/III-V interface, thin channel do not degrade v_{inj}
- Obtaining R_s=80 Ω.µm at required footprint
- Acceptable short-channel effects

Three greatest worries!

Conclusions

- III-Vs attractive for CMOS: key for low V_{DD} operation
  - Electron injection velocity in InAs > 2X that of Si at 1/2X V_{DD}
  - Quantum well channel yields outstanding short-channel effects
  - Quantum capacitance less of a limitation than previously believed
- Impressive recent progress on III-V CMOS
  - Ex-situ ALD and MOCVD on InGaAs yield interfaces with unpinned Fermi level and low defect density
  - Sub-100 nm InGaAs MOSFETs with I_{ON} > than Si at 0.5 V demonstrated
- Lots of work ahead:
  - Demonstrate 10 nm III-V MOSFET that is better than Si
  - P-channel MOSFET
  - Manufacturability, reliability