Mobility Enhancement in Indium-rich N-channel $In_xGa_{1-x}As$ HEMTs by Application of <110> Uniaxial Strain

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Abstract— As in Si CMOS, the incorporation of mechanical strain offers the possibility of improving the performance of III-V field effect transistors (FETs). Quantifying its potential and providing fundamental understanding of the impact of strain are the goals of this study. This paper reports an investigation of the impact of <110> uniaxial strain on n-type InAlAs/InGaAs HEMTs with a 70% InAs channel core. The main impact of strain is found to be a modification of the electron effective mass and mobility. A comparison between the effect of <110> strain in Si and InGaAs suggests that strain engineering can indeed be leveraged to improve transport properties in deeply scaled InGaAs FETs.

I. Introduction

The incorporation of mechanical strain in the channel has greatly enhanced the carrier velocity and performance of both n- and p-type Si MOSFETs (1). As scaling approaches the end of the roadmap, InGaAs-based FETs are receiving a great deal of attention as a potential post-Si CMOS logic technology. (2-3) Just as with Si, in an effort to explore the ultimate potential of InGaAs for logic, strain is being investigated as a path to improve the performance of InGaAs FETs. (4-5)

In the literature, only a handful of experiments involving strain on actual FETs have been described. (6-7) In these studies, it is hard to attribute the observed changes entirely to strain-induced effects such as mobility enhancement, because the effects of strain and channel material composition were not separated (6), or the analysis was not detailed enough (7).

Our previous study showed that uniaxial strain can be used to improve the electrostatic control of n-type AlGaAs/InGaAs Pseudomorphic High Electron Mobility Transistors (PHEMT) with a low InAs mole fraction (15%) channel through the piezoelectric effect but offered little in terms of improved transport. (8) In the present work, we carry out a detailed experimental study of uniaxial strain effects on InAlAs/InGaAs HEMTs with a 70% InAs channel core and a scaled InAlAs barrier. In these devices we found that mobility change dominates the impact on the device characteristics that result from the application of uniaxial strain.

II. Experiments

To introduce controlled uniaxial strain in HEMTs, we designed and fabricated a mechanical apparatus to bend small chips (Fig. 1(*a*)). This apparatus allows the application of uniaxial strain up to ±0.3% to III-V chips with a size down to 2 mm x 4 mm**.** Four metal ridges at the center of the apparatus are used to apply force to the chip. Alternating the relative horizontal positions of the two pairs of ridges changes the type of strain (compressive or tensile) on the top surface of the chip. Due to their fragility, the III-V chips are mounted on a Ti plate together with a strain gauge (Fig. **1** (b)). The devices are wire-bonded to connection pads that connect them to a semiconductor parameter analyzer. The strain level has been calibrated through: 1) *in-situ* strain gauge measurements and 2) *ex-situ* curvature measurements by surface laser reflection.

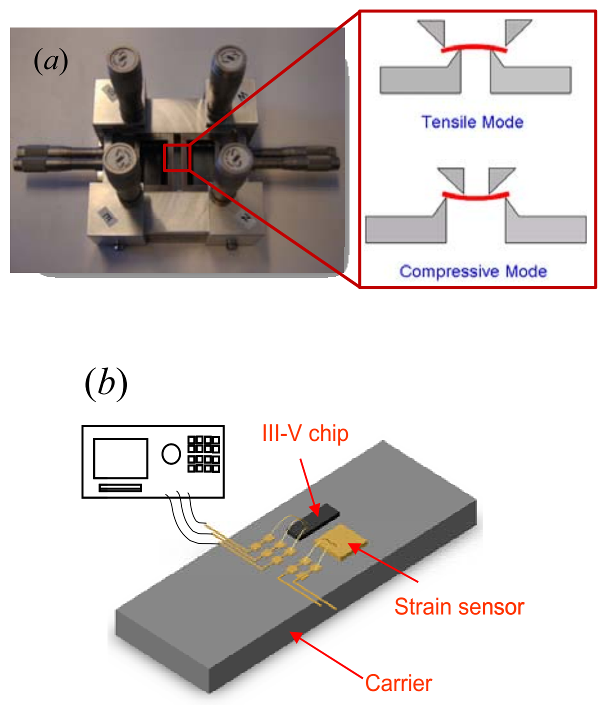

Fig. 1. (*a*) Chip-bending apparatus. (*b*) Experimental setup to characterize devices under uniaxial strain.

The devices used in this study are HEMTs with a thin indium-rich $In_{0.70}Ga_{0.30}As$-channel core. Fig. 2 sketches a cross section of these devices. Devices made on the same heterostructure have shown excellent logic scaling behavior down to gate lengths (L_g) of 30 nm. (9) In this study, in order to avoid short-channel effects, devices with L_g = 2 µm were fabricated. The gate was driven into the InAlAs barrier by a platinum-sinking technique (2). The final InAlAs barrier thickness is estimated to be 10 nm. Fig. 3 shows typical transfer characteristics of a representative device.

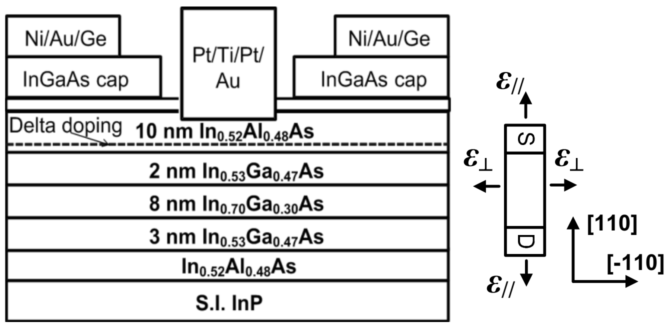

Fig. 2. (Left) Cross section of HEMTs used in this study. L_g = 2 µm. (Right) The configuration of applied strain.

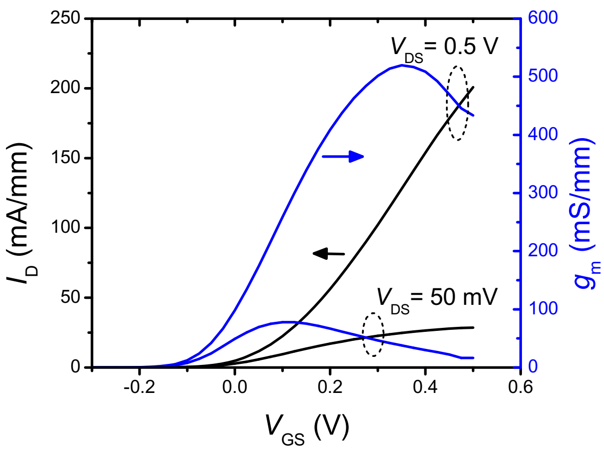

Fig. 3. Transfer characteristics of the device under study.

We performed bending experiments on devices with the channel oriented along the [110] direction. We sequentially applied tensile and compressive strain, both parallel ($\varepsilon_{//}$) and perpendicular ($\varepsilon_{\perp}$) to the channel direction, as indicated in Fig. 2. A set of electrical parameters were extracted by a benign characterization suite during bending experiments. We studied the strain dependence of V_T, defined at I_D=1 mA/mm, as a proxy for the device electrostatics, and the linear-regime drain current (I_{Dlin}) as a proxy for low-field transport. Both V_T and I_{Dlin} are determined at V_{DS}=50 mV to minimize heating effects and parasitic ohmic drops.

III. Results and Discussion

Fig. 4 shows the sequential change of V_T with $\varepsilon_{//}$. The fact that V_T tightly follows the loading and unloading of strain indicates that strain was successfully applied to the device and that no relaxation took place in the course of the experiment. Similar results were obtained with strain applied normal to the channel.

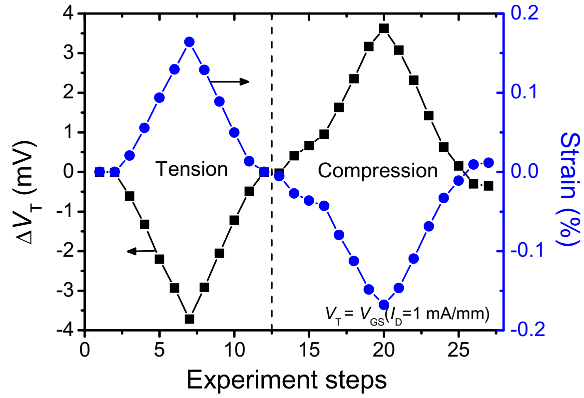

Fig. 4.Threshold voltage shift under $\varepsilon_{//}$.

Fig. **5** shows the change of threshold voltage (ΔV_T) for both strain along [110] ($\varepsilon_{//}$) and [-110] ($\varepsilon_{\perp}$). ΔV_T for the two <110> directions shows exactly the same dependence on strain. To avoid any interference from mobility change when using the constant current V_T definition, we also extracted V_T defined as the value of V_{GS} that corresponds to the extrapolation of the linear-regime drain current to zero. The conclusion that ΔV_T is independent of the strain orientation does not change.

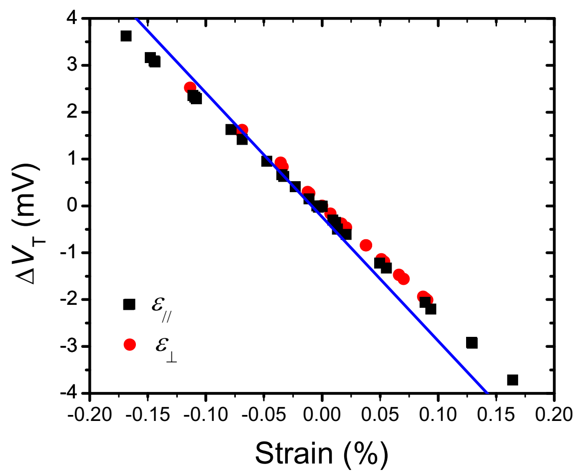

Fig. 5. Change of V_T as a function of <110> strain. The line corresponds to a model accounting for strain-induced $\Delta\phi_B$.

Fig. 6 shows the change in the Schottky barrier height ($\Delta\phi_B$) extracted from a thermionic-emission model for the forward *I-V* characteristics of the gate-source diode as a function of the change in V_T. The linear regression of $\Delta\phi_B$ to ΔV_T reveals that the dependence of ΔV_T on strain can be almost fully attributed to the strain-induced change in ϕ_B, which is due to the hydrostatic component of the applied strain and is orientation independent (8). The coefficient that determines the change in ϕ_B with strain is the conduction band deformation potential (a_c). a_c extracted from our experiment is -13 eV, which is within the range of -3.4 eV to -21 eV that is reported in the literature (13).

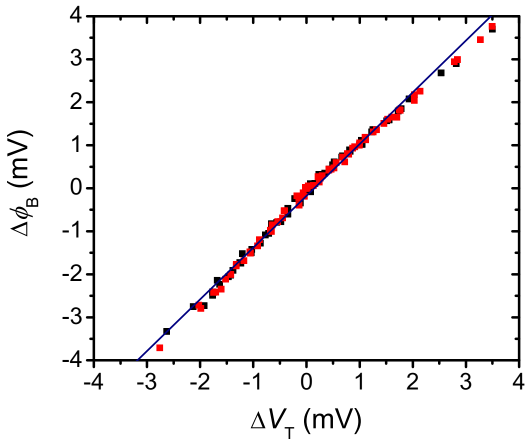

Fig. 6. Linear regression of $\Delta \phi_B$ to ΔV_T.

The orientation-independent ΔV_T behaviour observed in these InAlAs/InGaAs devices is different from our earlier report on AlGaAs/InGaAs PHEMTs (8). In the devices in (8), the sign of ΔV_T changes as one alters the strain direction from [110] to [-110]**.** This was attributed to the piezoelectric effect. The orientation-independent ΔV_T in the present InAs-rich devices indicates that the piezoelectric effect is negligible. The reason for this is the much reduced barrier and channel thicknesses in the present devices and the small piezoelectric constants of the InAs-rich alloys in the barrier and the channel. (10) The orientation-independent ΔV_T also implies that the change of the centroid capacitance, which is the primary mechanism behind the gate capacitance (C_G) shift in the AlGaAs/InGaAs PHEMTs (8), becomes insignificant in the present devices.

To investigate the impact of strain on transport in our InGaAs HEMTs, we have extracted the linear-regime drain current (I_{Dlin}) defined at a constant gate overdrive (V_{GS}-V_T=0.2 V) and V_{DS}=50 mV. Similar to strained Si MOSFETs, if C_G stays constant with strain, I_{Dlin} can be used as an indicator of mobility shift (11).

Fig. 7 shows the relative change of I_{Dlin} for strain along the two <110> directions. It is clearly seen that tensile $\varepsilon_{//}$ increases I_{Dlin}, and tensile $\varepsilon_{\perp}$ decreases I_{Dlin}. Compressive strain has the contrary effect.

Monte Carlo simulations of biaxial strain effects on $In_xGa_{1-x}As$ (12) show that strain changes the electron effective mass (m_e^*) and, as a consequence, the electron mobility (μ_e). To facilitate understanding of the essential physics, we have carried out 8x8 *k.p* simulations and calculated the band structure of InGaAs as affected by uniaxial strain. Band parameters from (13) were used. A Poisson ratio of 0.33 was used, which corresponds to the Ti plate as the mounted chip deforms with it.

Fig. 8 shows constant energy contours of the conduction band on the 2DEG plane. The constant energy contours elongate along the direction of compressive strain (left) and contract along the direction of applied tensile strain (right). The contrary happens along the normal direction. The elongation and contraction of the energy contours respectively correspond to the increase and decrease of m_e^*.

Values of m_e^* were extracted from the curvature of *E-k* curves along <110>. A pronounced anisotropy of m_e^* change is seen with <110> uniaxial strain. The relative change for the in-plane effective mass parallel to strain ($m_{//}^*$) is -7% per 1% strain, and +7% per 1% strain for the in-plane effective mass perpendicular to strain ($m_{\perp}^*$).

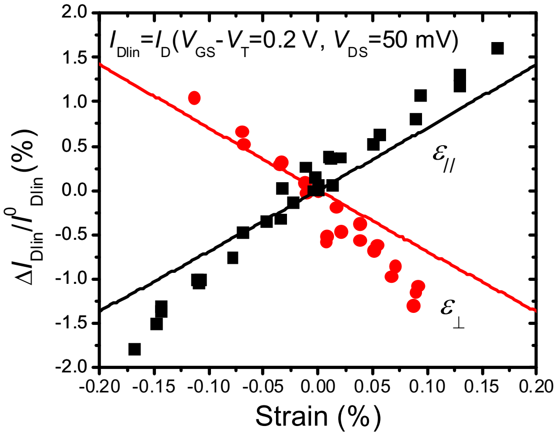

Fig. 7. Relative change of drain current in linear regime under <110> strain. The lines are results from *k.p* simulations.

In theory, the change in mobility ($\Delta\mu_e$) is a combination of changes in the conductivity effective mass (m_c^*) and scattering time (τ). However, in our present devices, little change is expected in τ. To the first order, the value of τ is determined by m_{DOS}^* (= $\sqrt{m_{//}^* m_{\perp}^*}$). Under <110> uniaxial strain, our k.p simulation results suggest that changes in $m_{\perp}^*$ and $m_{//}^*$ almost precisely cancel out. Hence, $\Delta\mu_e$ is mainly determined by changes in $1/m_c^*$. m_c^* is equal to $m_{//}$* when $\varepsilon_{//}$ is applied and to $m_{\perp}$* when $\varepsilon_{\perp}$ is applied. The solid lines in Fig. 7 represent the relative change in μ_e considering the change in $1/m_c^*$ due to <110> uniaxial strain as obtained from our *k.p* simulations. The μ_e reduction/enhancement factors predicted by $1/m_c^*$ are +7% and -7% per 1% strain, close to those experimentally measured in I_{Dlin} (+9.9% and -11.0% per 1% strain).

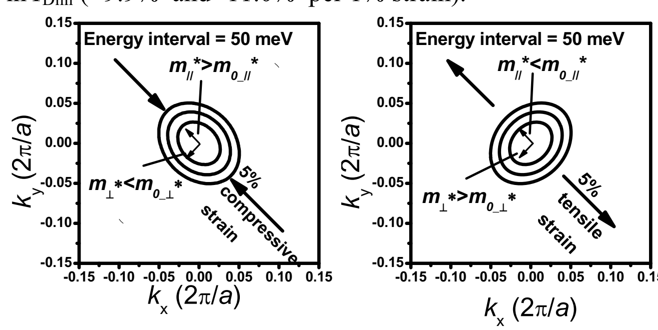

Fig. 8. Constant energy contour on the 2DEG conduction plane of InGaAs, under 5% <110> uniaxial compression (left) and tension (right).

To benchmark the <110> uniaxial strain effect on the InGaAs mobility, we compare it with that of Si (14-17). As shown in Fig. 9, similar to InGaAs, the <110> m_e^* of the 2-fold valleys in Si obtained by empirical non-local pseudopotential simulations changes anisotropically with applied <110> uniaxial strain. (14, 16-17) The <110> experimental μ_e data obtained from ultrathin-body Si FETs manifests this anisotropic change of m_e^*. (14) The mobility enhancement in Si, in addition to the change in m_e^*, might arise from reduced inter-valley scattering. It can be seen that the experimental mobility enhancement (14-15) as a result of 1% $\varepsilon_{//}$ is almost 4x higher in Si than in $In_{0.7}Ga_{0.3}As$.

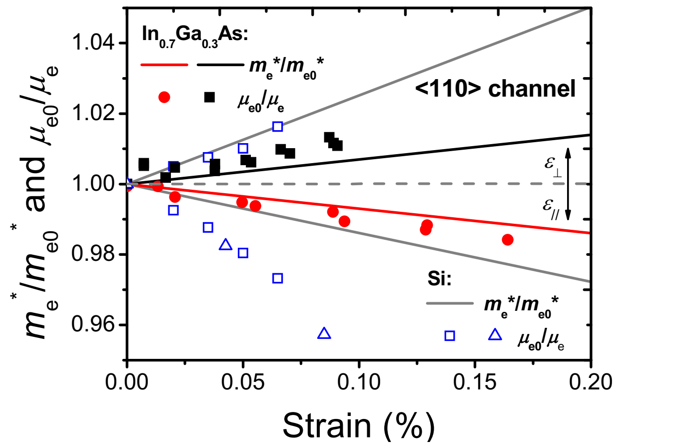

Fig. 9. Comparison of relative change under <110> uniaxial tensile strain in m_e^* and μ_e between Si (14-16) and $In_{0.7}Ga_{0.3}As$. The ratio of unstrained over strained μ_e is plotted, to compare with the effect in m_e^* reduction/enhancement. Continuous lines are simulations and symbols are experimental data.

In very short devices, the most important transport parameter is the high-field electron velocity and not the low-field mobility. (18-19) The effective electron velocity is a portion of the thermal velocity which is itself propotional to $(m_c^*)^{-1/2}$. (18) In fact, HEMTs with InAs channel cores have already demonstrated >2x higher electron injection velocity than strained Si MOSFETs thanks to the much smaller m_e^* in InAs. (20) Fig. **10** shows the simulated m_e^* reduction under 1 GPa <110> tensile stress for $In_xGa_{1-x}As$ with x ranging from 53% to 100% on an InP substrate or fully relaxed as on a suitable metamorphic substrate. For reference, the simulated reduction in m_e* of the 2-fold valleys in Si (14, 16) under the same level of tensile stress is also indicated. The choice of the same stress level (as opposed to strain level) for the comparison is reasonable since stress more closely reflects the technological effort involved.

As more InAs is incorporated into the channel, the m_e^* reduction becomes more pronounced. A pure InAs channel on an InP substrate shows the same level of m_e^* reduction as Si does. Furthermore, if the lattice-mismatch induced biaxial compressive strain in the channel could be relieved, the m_e^* reduction factor can be further enlarged, exceeding that of Si.

One concern of further m_e^* reduction in materials with small m_e^* is that the current drivability of the device suffers as a result of a reduction in gate capacitance that is dominated by the quantum capacitance. (21) However, the quantum capacitance is set by the m_{DOS}^* and, as discussed before, this is little affected by uniaxial strain.

IV. Conclusion

We have investigated <110> uniaxial strain effects on InAlAs/InGaAs HEMTs with an InAs-rich channel by chip-bending experiments. We have found that uniaxial strain changes the electron mobility through a change in the effective mass. *k.p* simulations suggest that the effective mass reduction factor can exceed that of Si by incorporating more InAs in the channel and relieving the lattice-mismatch biaxial strain. This result indicates that strain engineering can be leveraged to improve the transport properties of InGaAs FETs, especially in deeply scaled devices.

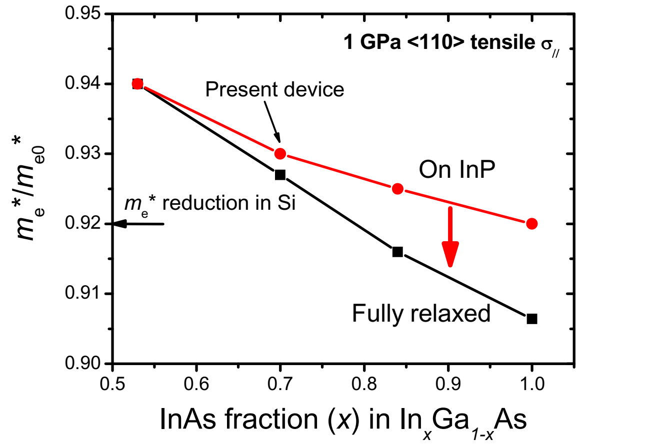

Fig. 10. Effective mass reduction factors obtained from *k.p* simulations for $In_xGa_{1-x}As$ with various InAs fraction. Incorporation of high InAs composition and relief of the lattice-mismatch strain enlarge the m_e^* reduction factor.

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References

(1) S. Tyagi, *et al.*, *IEDM*, 2005, p. 245.
(2) D.-H. Kim and J. A. del Alamo, *IEDM*, 2008, p. 719.
(3) M. K. Hudait, *et al.*, *IEDM,* 2007, p. 625.
(4) H.-C. Chin, *et al.*, *IEEE EDL,* vol. 30, p. 805, 2009.
(5) C. Hock-Chun, *et al.*, *VLSI Symp,* 2009, p. 244.
(6) Y. J. Chan, *et al.*, *IEDM Tech. Dig.*, 1987, p. 427.
(7) S. Suthram, *et al.*, *VLSI Symp.,* 2008, p. 182.
(8) L. Xia and J. A. del Alamo, *APL,* vol. 95, p. 243504, 2009.
(9) D.-H. Kim and J. A. del Alamo, *IEDM*, 2006, p. 719.
(10) S. Adachi, *Properties of Semiconductor Alloys: Group-IV, III-V and II-VI Semiconductors*: Wiley, 2009.
(11) M. Saitoh, *et al.*, *IEDM*, 2009, p. 469.
(12) C. Kopf, *et al.*, *SSE,* vol. 41, p. 1139, 1997.
(13) I. Vurgaftman, *et al.*, *JAP,* vol. 89, p. 5815, 2001.
(14) K. Uchida, *et al.*, *IEDM*, 2005, p. 129.
(15) S. Suthram, *et al.*, *IEEE EDL,* vol. 28, p. 58, 2007.
(16) S. Dhar, *et al.*, *IEEE Transactions on Nanotechnology,* vol. 6, p. 97, 2007.
(17) E. Ungersboeck, *et al.*, *Journal of Computational Electronics,* vol. 6, p. 55, 2007.
(18) A. Khakifirooz and D. A. Antoniadis, , *IEEE TED,* vol. 55, p. 1391, 2008.
(19) A. Khakifirooz and D. A. Antoniadis, *IEEE TED,,* vol. 55, p. 1401, 2008.
(20) D.-H. Kim, *et al.*, *IEDM*, 2009, pp. 861.
(21) D. Jin, *et al.*, *IEDM*, 2009, p. 495.