Logic Characteristics of 40 nm thin-channel InAs HEMTs

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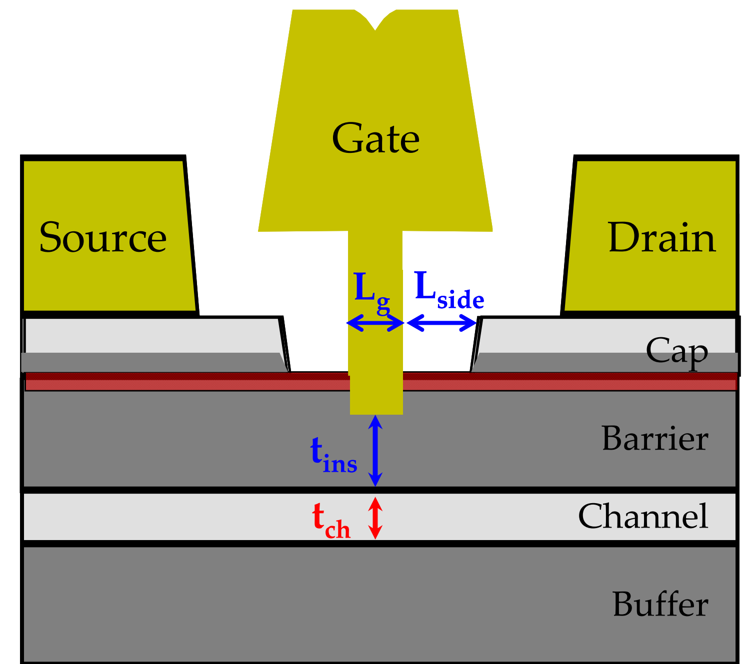
Scaling issues in III-V HEMT

- Motivation
  - ✓ III-V HEMT: Model system for future III-V logic FETs

- Key dimensions:
  - Gate Length (L_g)
  - Barrier Thickness (t_{ins})
  - Side-recess Length (L_{side})
  - **Channel Thickness (t_{ch})**

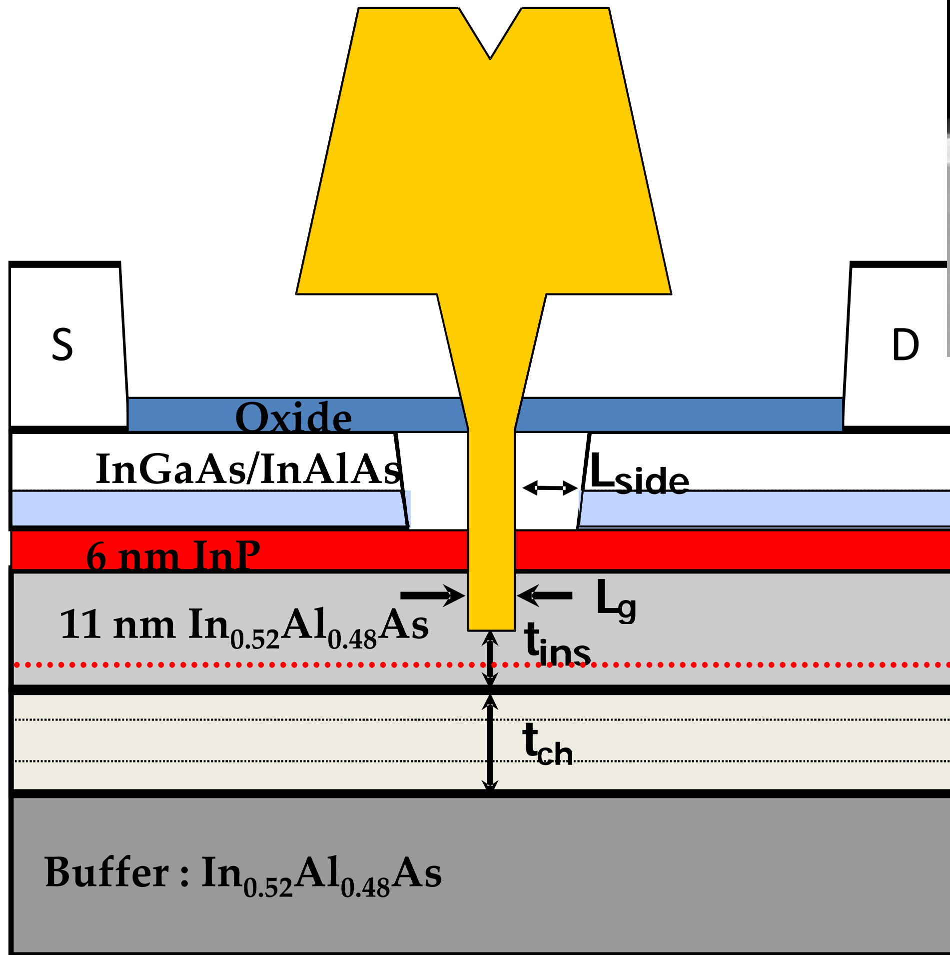
- Scaling trajectory:
  - $L_g \downarrow \rightarrow t_{ins} \downarrow$, $t_{ch} \downarrow$, $L_{side} \downarrow$

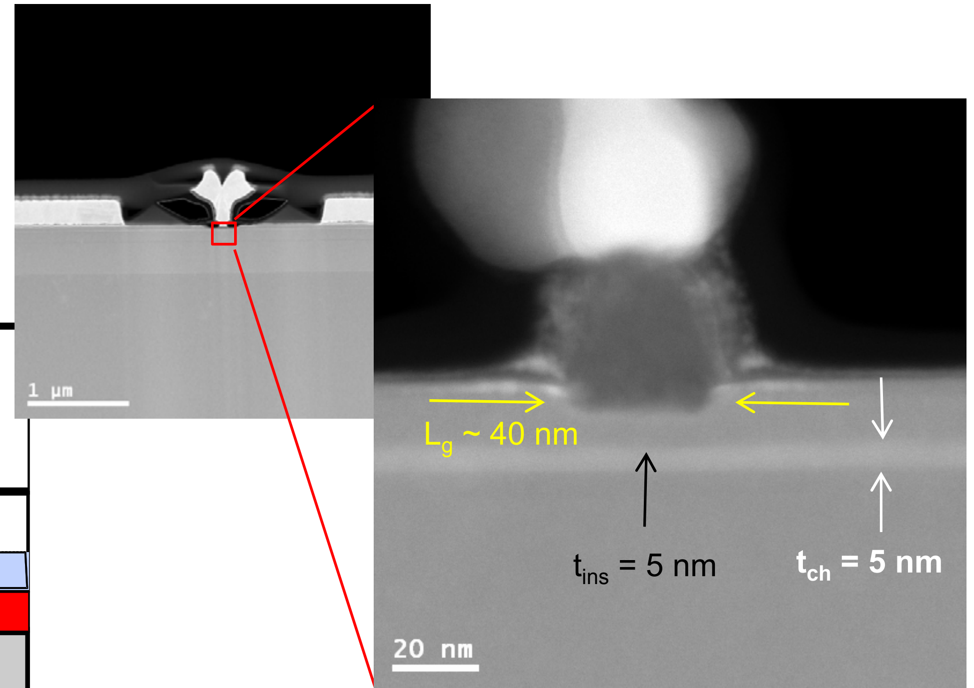


< Schematic of III-V HEMT >

- Goal : Explore trade-offs involved in channel thickness scaling

Thin channel InAs HEMT





$In_{0.7}Ga_{0.3}As$: 1 nm
InAs: 2 nm
$In_{0.7}Ga_{0.3}As$: 2 nm

t_{ch} = 5 nm

$\mu_{n,Hall}$ = 9,950 cm^2/V-sec

Triple-step gate recess process

- Gate metal stack: Ti/Pt/Au
- L_{side} = 80 nm, t_{ins} = 5 nm

Reference : InAs HEMT with t_{ch} = 10 nm
$\mu_{n,Hall}$ = 13,500 cm^2/V-sec
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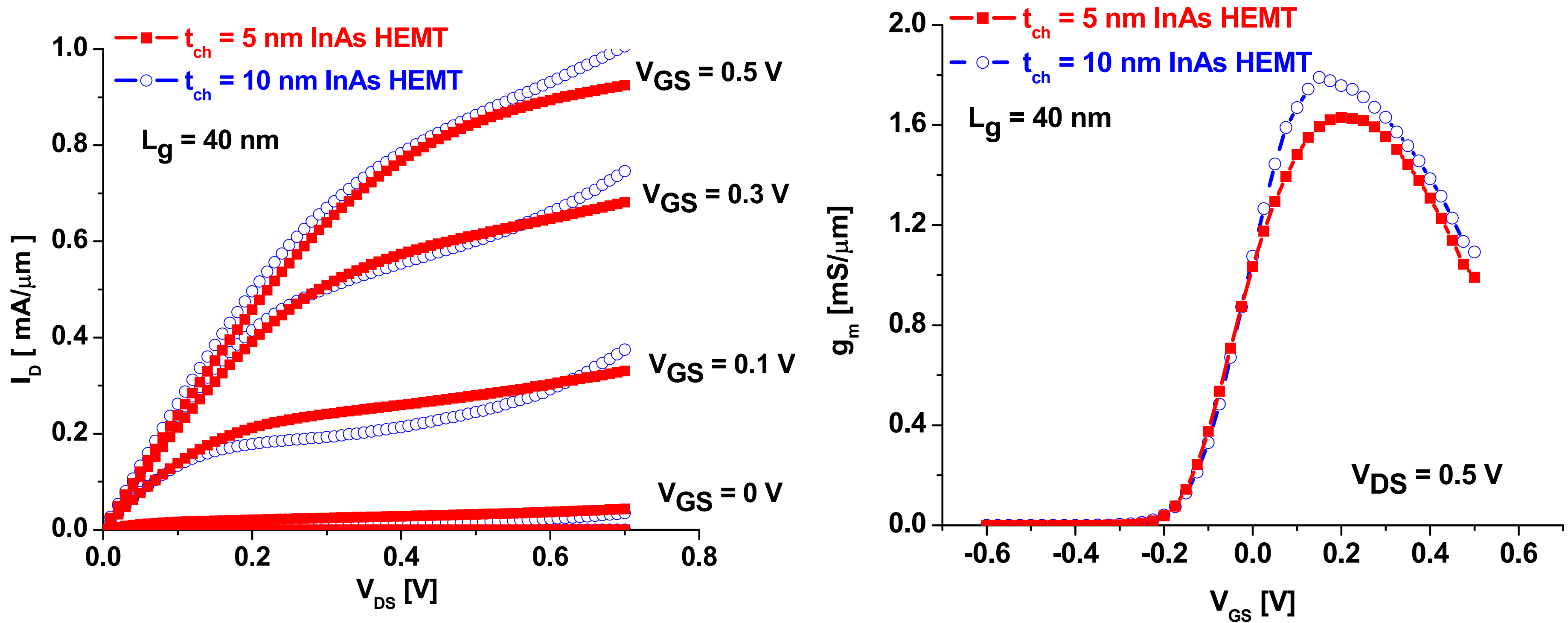
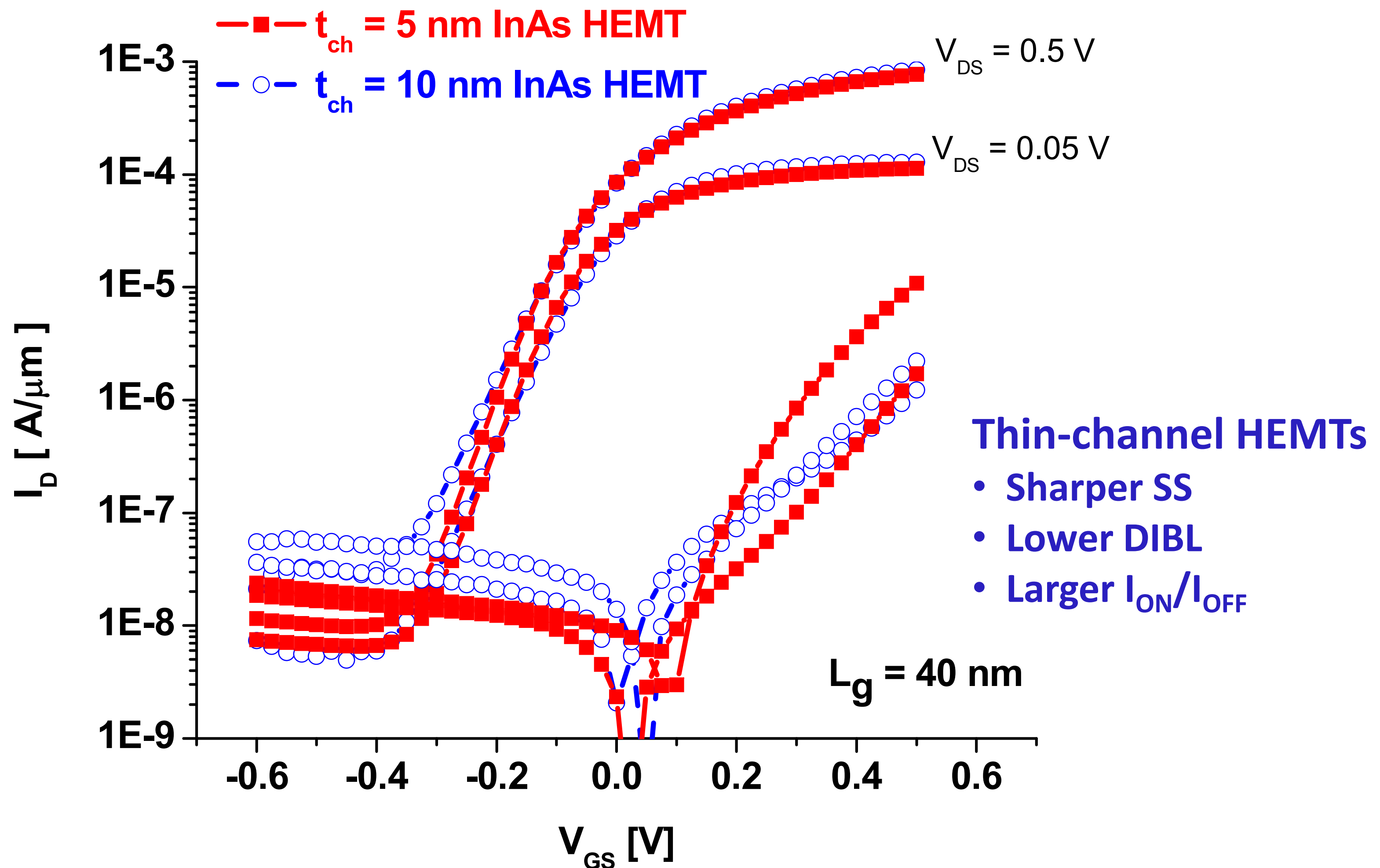
Output & g_m Char.: L_g = 40 nm



- Good I_D saturation, pinch-off behavior

- g_m = 1.65 mS/μm @ V_{DS}=0.5 V

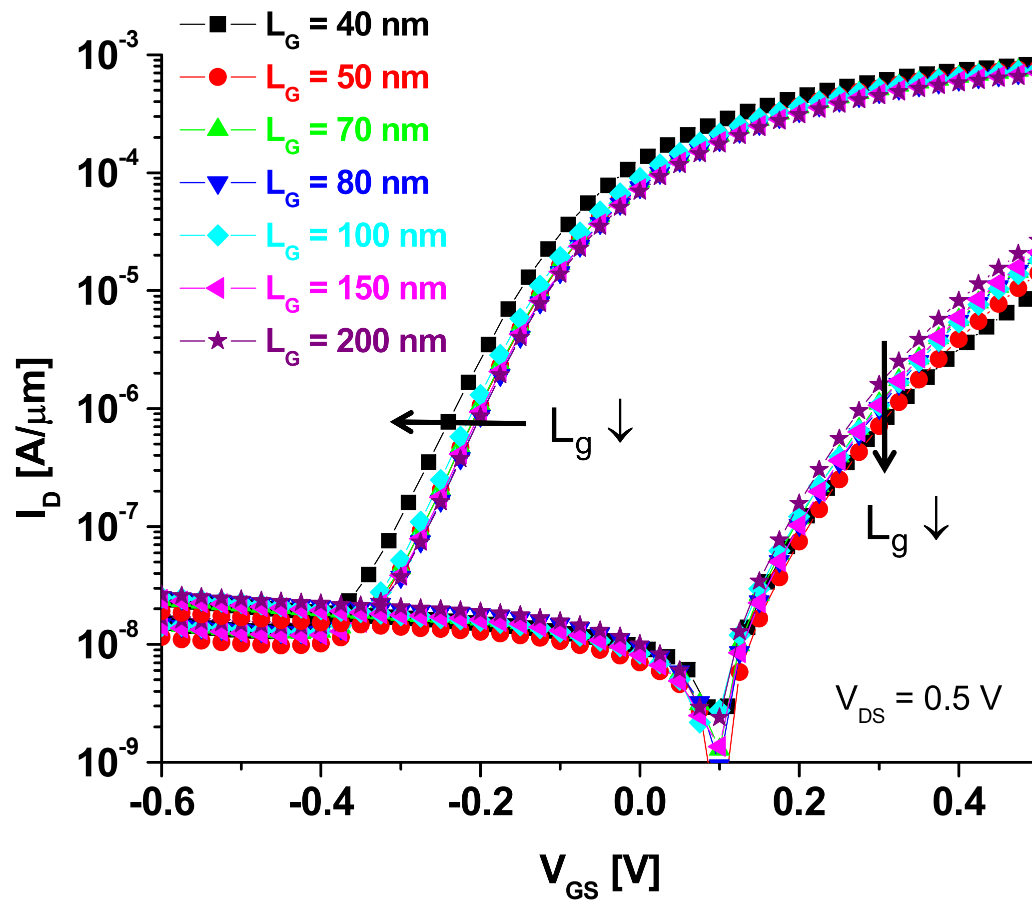
Subthreshold Char.: L_g = 40 nm



For t_{ch} = 5 nm device at V_{DS} = 0.5 V,

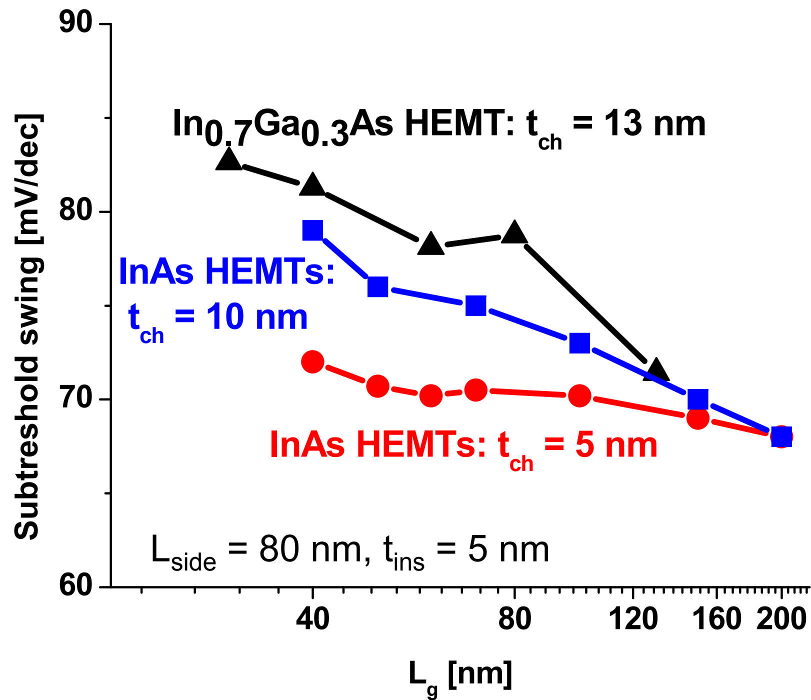
SS = 72 mV/dec, DIBL = 72 mV/V and I_{ON}/I_{OFF} = 2.5 x 10^4

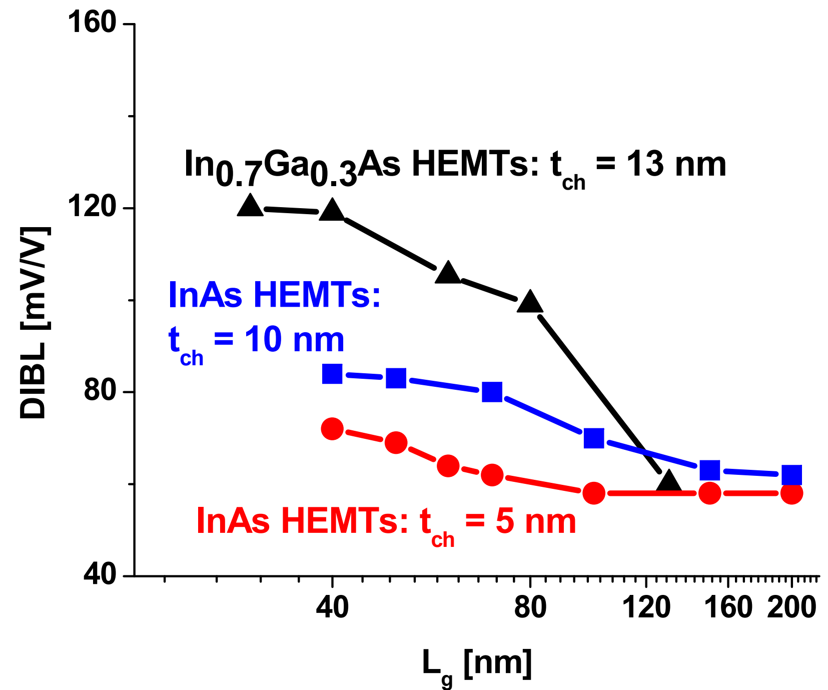
Subthreshold Char. vs L_g



- Harmonious scaling ➔ Very small V_T roll off with L_g (34 mV)

SS & DIBL vs. L_g





✓ Excellent electrostatic integrity and scalability with thin channel

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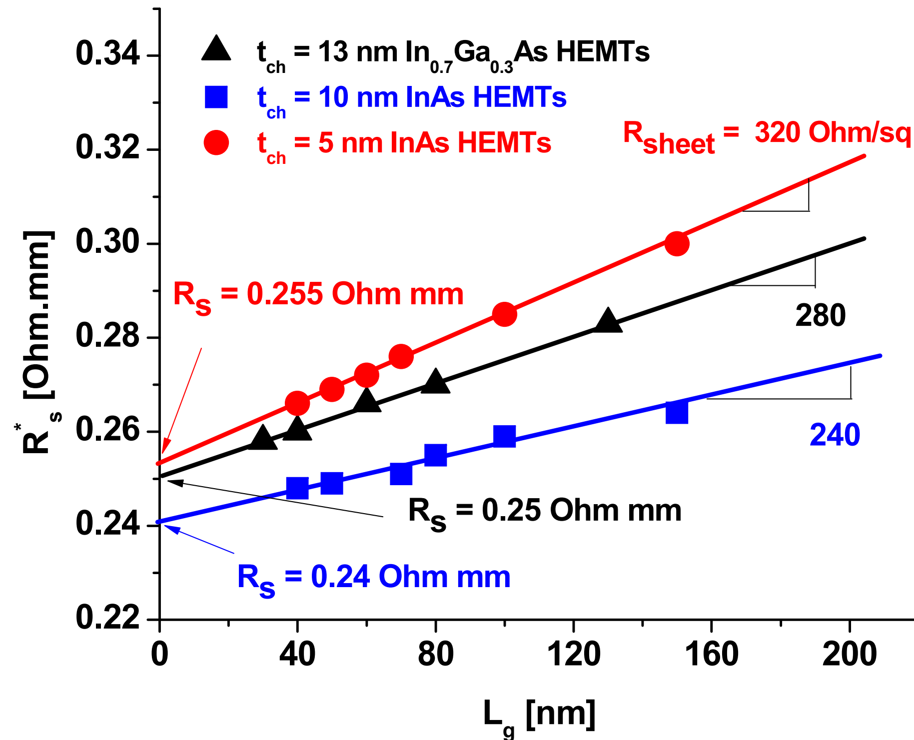
Key trade-off: Source resistance

< Gate current injection technique>



Thin-channel InAs HEMTs:

- Higher R_{sh} ➔ higher R_s

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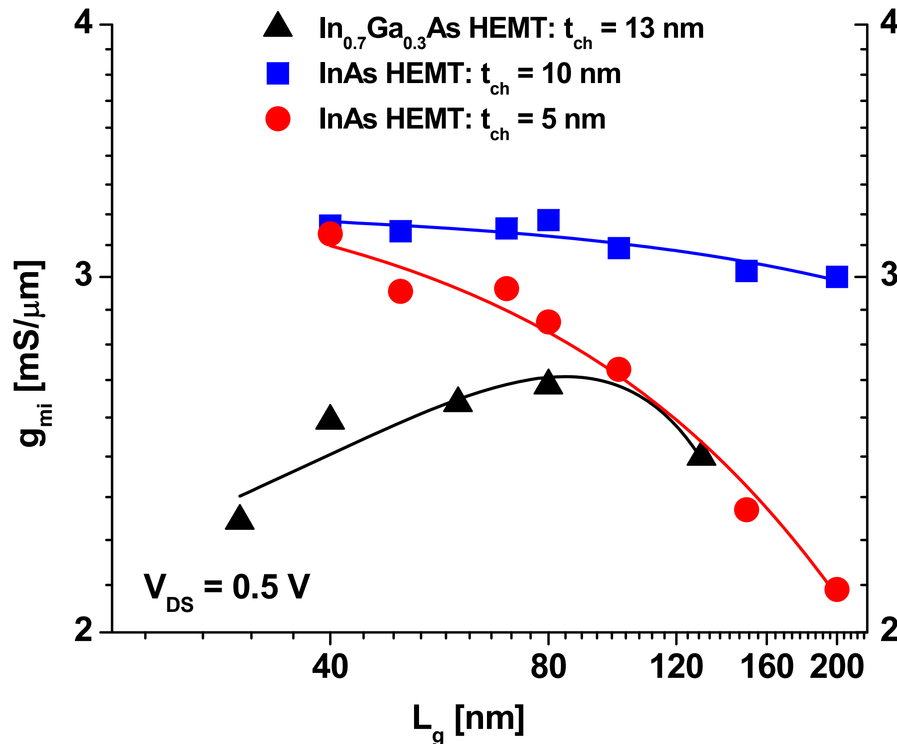
Scalability of g_{mi}

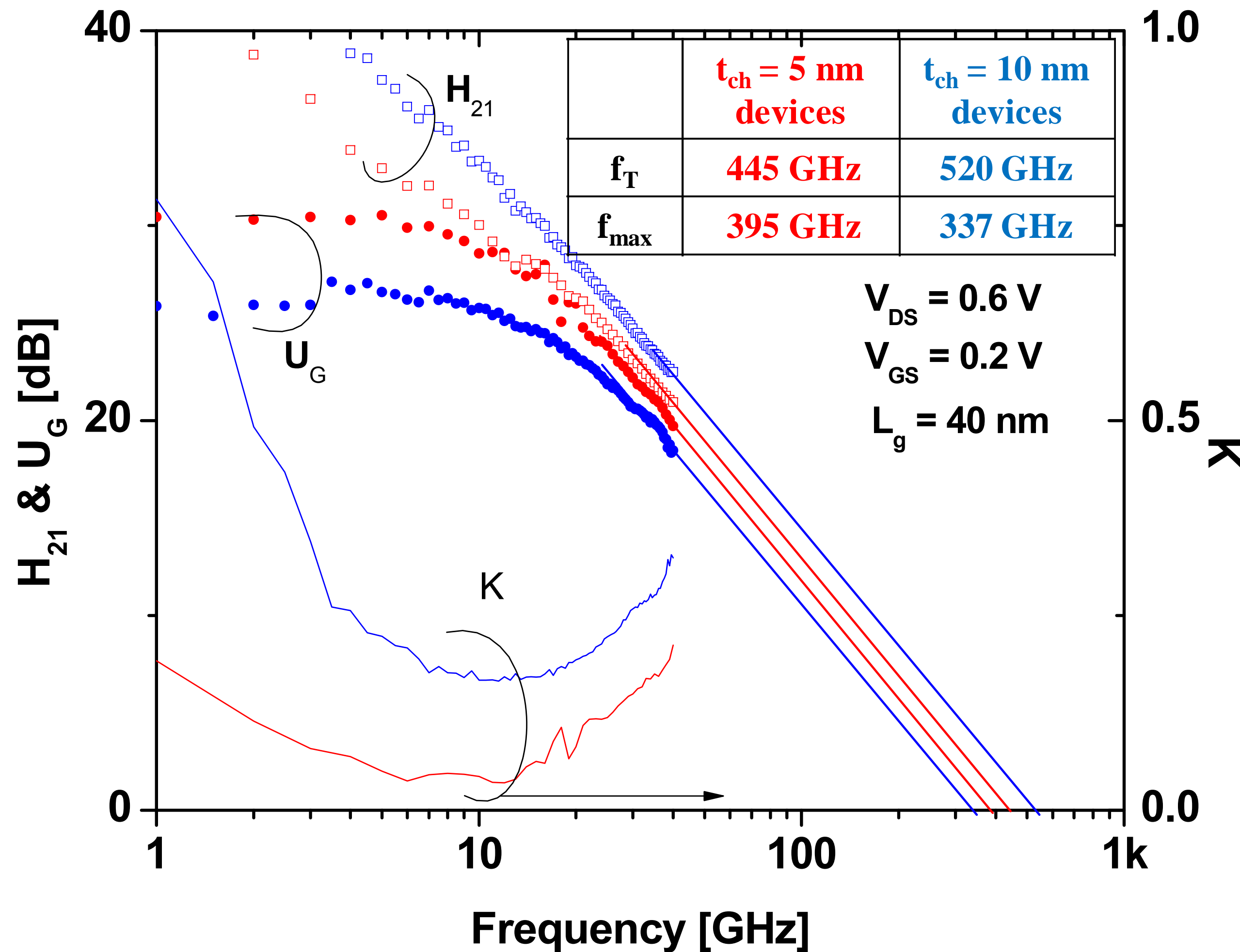
<g_{mi} from S-parameters>



Thin-channel InAs HEMTs:

- Lower values of g_{mi} due to lower μ_n
- But velocity less affected ➔ better g_{mi} scalability down to 40 nm

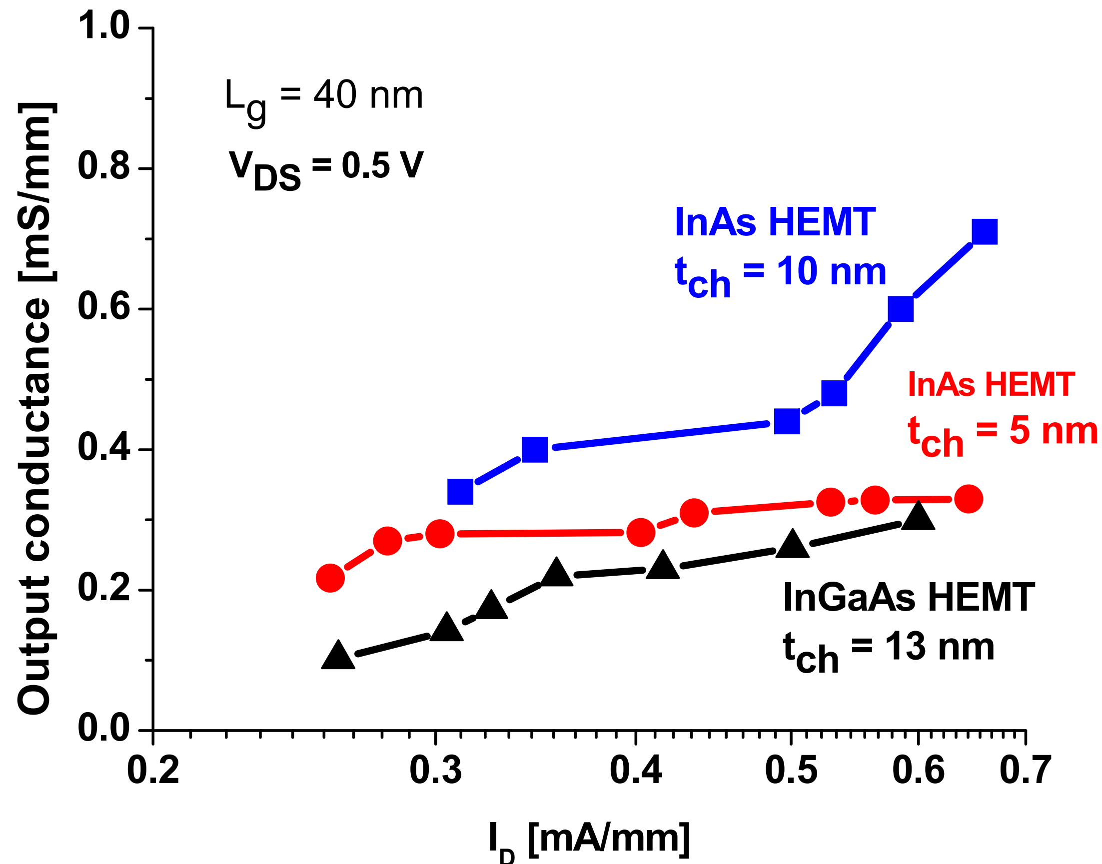
f_T & f_{max} char. : L_g = 40 nm



	t_{ch} = 5 nm devices	t_{ch} = 10 nm devices
f_T	445 GHz	520 GHz
f_{max}	395 GHz	337 GHz

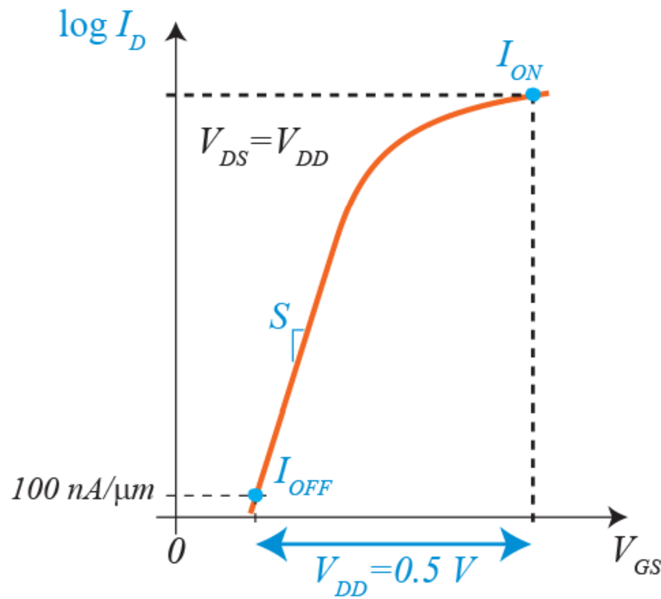
For thin-channel InAs HEMT: Low f_T but high f_{max}

Why high f_{max} ? ➔ Evaluation of g_o

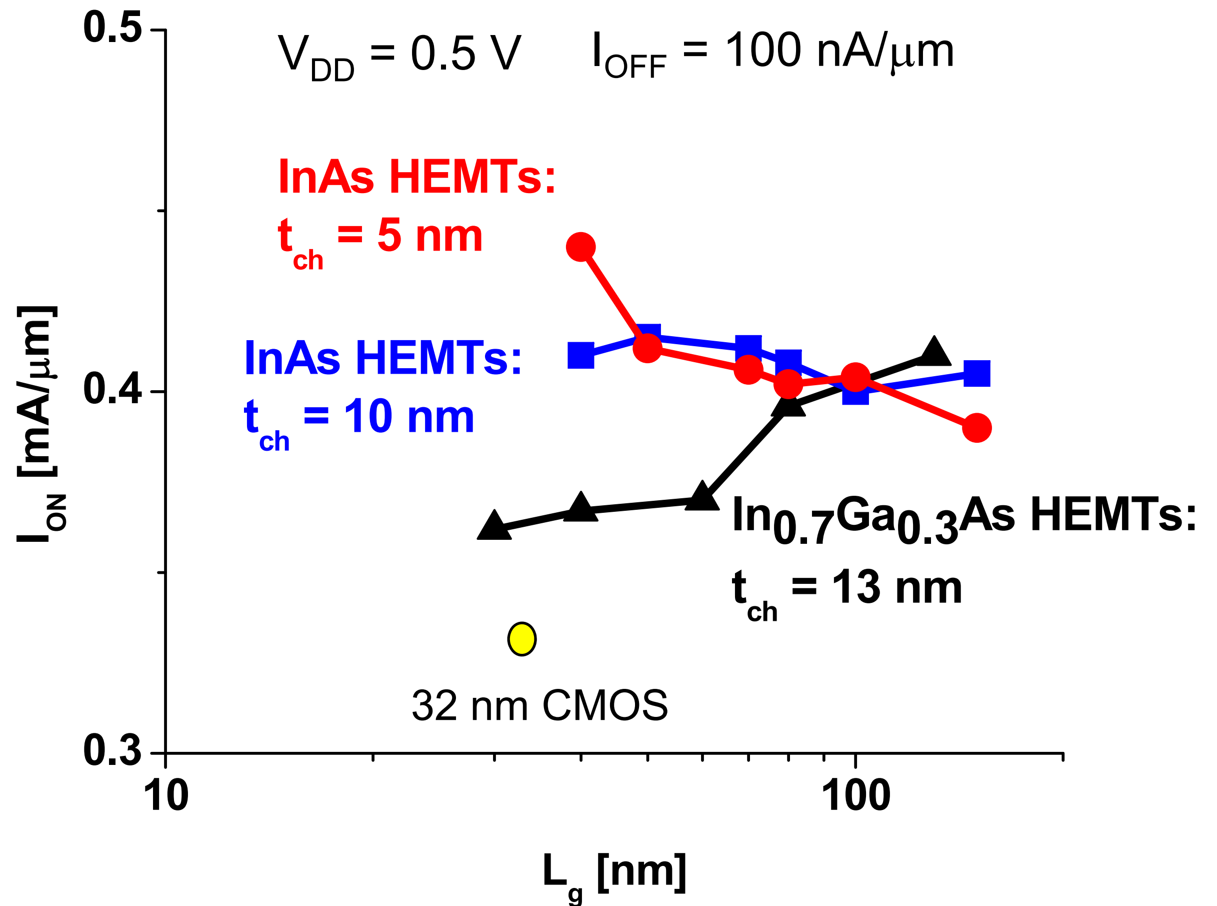


- **Lower DIBL, lower Impact ionization:**
  ➔ improved output conductance with thin channel

Unified FOM for Logic



I_{ON} at given I_{OFF} and V_{DD}



For thin-channel InAs HEMT:

➔ Better scalability in sub – 100nm regime

Conclusion

- **Thin-channel (t_{ch} = 5 nm) InAs HEMTs**
  - At L_g = 40 nm, thin-channel HEMTs are excellent
    - DIBL = 72 mV/V, S = 72 mV/dec and $I_{ON}/I_{OFF} > 10^4$
  - Main advantage: improved electrostatics and scalability
  - Trade-offs: μ_n = 9,950 cm^2/V-sec, R_s = 0.255 Ω·mm

- **Future work:**
  - Increase gate foot stem height ~ 200 nm to improve f_T
  - Extract injection velocity and gate capacitance.
  - Optimize barrier to lower R_s and R_C.