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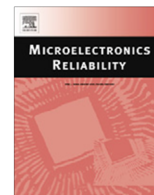

Role of stress voltage on structural degradation of GaN high-electron-mobility transistors

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ABSTRACT

In GaN high-electron-mobility transistors, electrical degradation due to high-voltage stress is characterized by a critical voltage at which irreversible degradation starts to take place. Separately, cross-sectional TEM analysis has revealed significant crystallographic damage for severely degraded devices. Furthermore, a close correlation between the degree of drain current degradation and material degradation has been reported. However, the role of the critical voltage in physical degradation has not been explored. In this work, we investigate the connection between electrical degradation that occurs around and beyond the critical voltage and the formation of crystallographic defects through detailed electrical and TEM analysis, respectively. We find that a groove in the GaN cap starts to be generated around the critical voltage. At higher voltages, a pit develops that penetrates into the AlGaN barrier. The size of the pit increases with stress voltage. We also observe a good correlation between electrical and material degradation.

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1. Introduction

In GaN high-electron-mobility transistors (HEMTs) under high-voltage electrical stress degradation in the drain and gate current is electric field driven [1–3] and is characterized by a sharp onset at a critical voltage beyond which various device performance parameters start to degrade [4–9]. In addition, electrical stress beyond the critical voltage introduces enhanced trapping behavior [5,10]. These modes of degradation are found to be permanent and irreversible [1]. This behavior has been explained through a model that invokes the creation of defects when mechanical stress in the AlGaN barrier layer, introduced through the inverse piezoelectric-effect, exceeds a critical value [4,11]. In this model, the electric field is the primary driver behind degradation.

Cross-sectional transmission electron microscopy (TEM) analysis has revealed the introduction of structural damage in GaN HEMTs after long-term DC and RF life tests at high voltage [12–16]. Crystallographic defects such as pits and cracks have been observed at the drain side of the gate corner in the GaN cap and AlGaN barrier layer. A correlation between the amount of electrical degradation in terms of drain current reduction and the degree of physical damage in the semiconductor has also been reported [13]. In addition, a planar technique has recently been used to investigate the evolution of defect formation as a function of stress voltage [17]. In this work it was found that an almost continuous shallow groove is formed at voltages below the critical voltage. At the critical voltage, localized pits appear along this groove. As the stress voltage increases, these pits grow in size and merge with each other [17]. This planar study has brought great understanding to the nature of structural damage created by high-voltage stress in GaN HEMTs. A complementary study of the evolution of these defects in the cross section as a function of stress voltage is still to be carried out. To fill this gap is the goal of this work.

In this paper, we investigate the correlation between electrical degradation and physical degradation in GaN HEMTs stressed around and beyond the critical voltage through cross-section TEM. We have found that around the critical voltage, a shallow groove appears in the GaN cap layer at the drain side of the gate edge. Then deeper pits grow into the AlGaN barrier layer as the stress voltage increases. At very high stress voltage, a crack is finally formed in the AlGaN barrier. Good correlation between electrical and cross-sectional structural degradation has been found, suggesting that the observed defects are responsible for electrical degradation in GaN HEMTs.

2. Electrical degradation

The devices investigated are experimental 0.25 μm integrated-field-plate gate HEMTs with $W = 2 \times 25$ μm [14,18]. The epitaxial structure that includes a 3 nm GaN cap and a 16 nm $Al_{0.28}Ga_{0.72}N$

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barrier was grown on semi-insulating SiC substrate by MOCVD. These devices are passivated with SiN_x.

We have performed short-term step-stress experiments in the $V_{DS} = 0$ state at 150 °C of base plate temperature. The high temperature was chosen in order to accelerate degradation and also to make the defect formation more uniform across the device width. Also, this high temperature simulates the self heating that takes place under real operating conditions. In the $V_{DS} = 0$ mode, high field electrical stress is equally applied to the source side and the drain side of the device. In these experiments, $|V_{GS}|$ was increased starting at −10 V in steps of 1 V (1 min per step) up to different voltages. The stress voltages were selected in order to map the transition that occurs around the critical voltage [4]. In order to obtain well matched degradation characteristics, all devices used in this work were located in close proximity to each other on the same chip. The devices were otherwise not selected in any particular way.

Fig. 1 shows the evolution of normalized I_{Dmax} (I_D at $V_{DS} = 5$ V and $V_{GS} = 2$ V), R_S, R_D and I_{Goff} (I_G at $V_{DS} = 0.1$ V and $V_{GS} = -5$ V) in five different experiments as a function of stress voltage. As shown here, I_{Goff} sharply increases around a stress voltage of 17 V, and I_{Dmax} starts to decrease and R_D and R_S start to increase at around the same voltage. This is what we term the critical voltage. A higher critical voltage is expected at room temperature [19]. Devices #1–6 represent different stages of degradation:

- Device #1: Most heavily degraded ($V_{DGstress} = 37$ V).
- Device #2: Medium-level degradation (25 V).
- Device #3: Onset of I_D, R_S and R_D degradation with large I_G degradation (17 V).
- Device #4: Medium-level I_G degradation (16 V).
- Device #5: Onset of I_G degradation (15 V).
- Device #6: Unstressed reference device.

As it can be seen in Fig. 1, the pattern of degradation is very reproducible from device to device. This well matched set of devices enables us to study the evolution of degradation as the stress voltage increases as if we had observed it in a single device.

We have electrically characterized these devices in detail at room temperature before and after the stress experiments. First, fully recovered or "uncollapsed" I_{Dmax} is measured after shining microscope light on the devices for 1 min. This light illumination expedites detrapping and quickly brings the device to a reproducible fully detrapped state. The decrease in uncollapsed I_{Dmax} in stressed devices with respect to their unstressed values is defined as *permanent degradation* (or the component of I_{Dmax} degradation that displays no transient characteristics) [20]. Then, we have measured the current collapse through a simple DC technique [21]. We apply a 1 s long voltage pulse with $V_{DS} = 0$ and $V_{GS} = -10$ V to induce electron trapping. Immediately after this pulse, we measure I_{Dmax}. This is the collapsed value. *Current collapse* is defined as the difference between uncollapsed and collapsed I_{Dmax} relative to the uncollapsed value (defined this way, current collapse is always positive).

Fig. 2 summarizes the evolution of current collapse and permanent degradation as a function of the final or maximum stress voltage in each sample. As shown in Fig. 2, both current collapse and permanent degradation increase the higher the stress voltage beyond a critical voltage of about 17 V. This is in agreement with

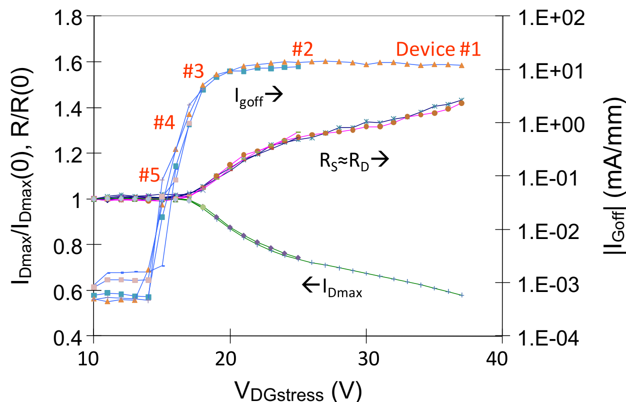

Fig. 1. Evolution of I_{Dmax}, R_S, R_D (normalized to its initial value) and I_{Goff} in $V_{DS} = 0$ step-stress experiments ($T = 150$ °C).

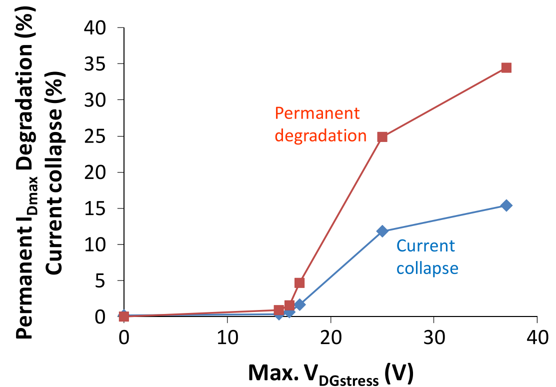

Fig. 2. Permanent degradation in I_{Dmax} and current collapse as a function of maximum stress voltage in the samples of Fig. 1.

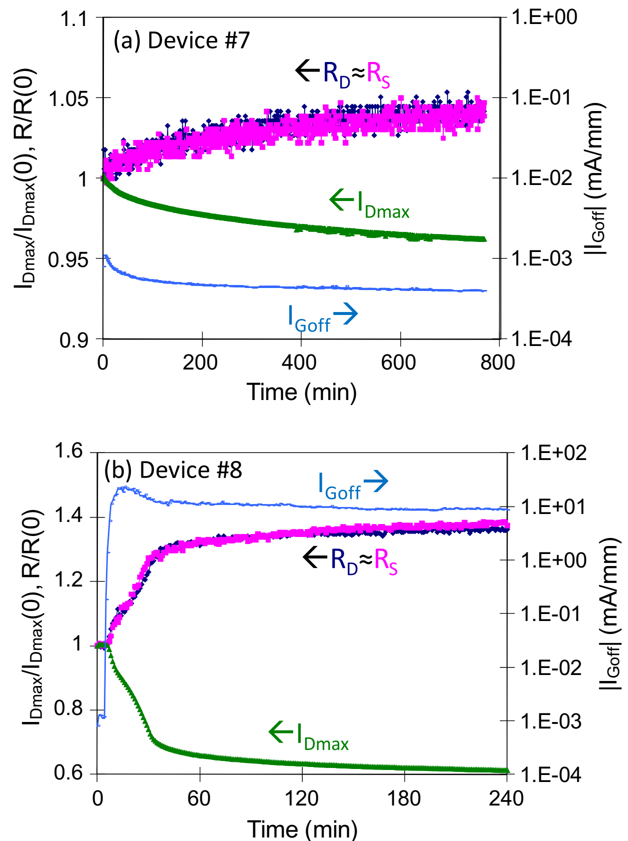

Fig. 3. Change in I_{Dmax}, I_{Goff}, R_S, and R_D during long-term stress in the $V_{DS} = 0$ state. The stress voltage is: (a) $V_{DG} = 11$ V (device #7) and (b) step-stressed from 10 to 40 V for the first 30 min and kept at 40 V afterwards (device #8). $T = 150$ °C.

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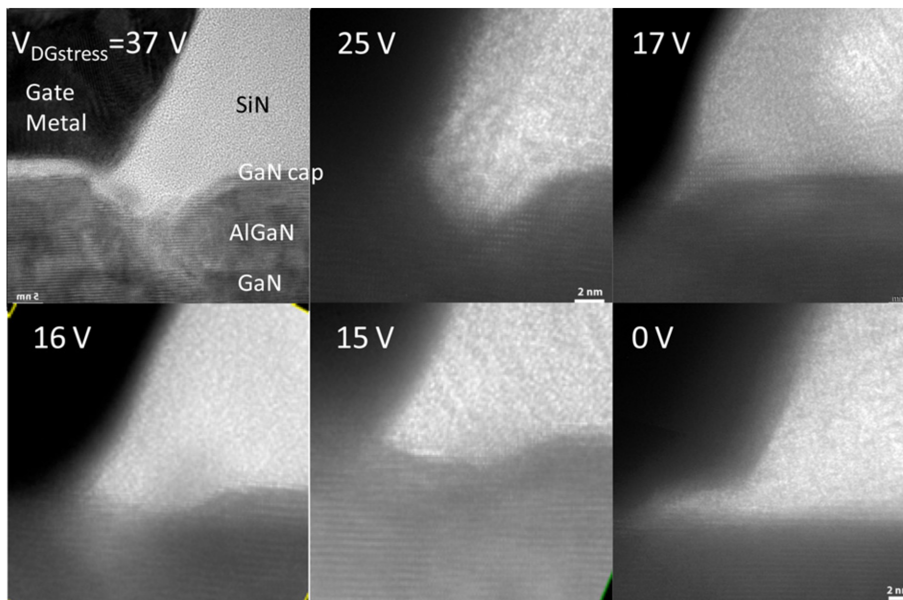

Fig. 4. Cross-sectional TEM images of the drain side of devices stressed at different voltages (device #1–6).

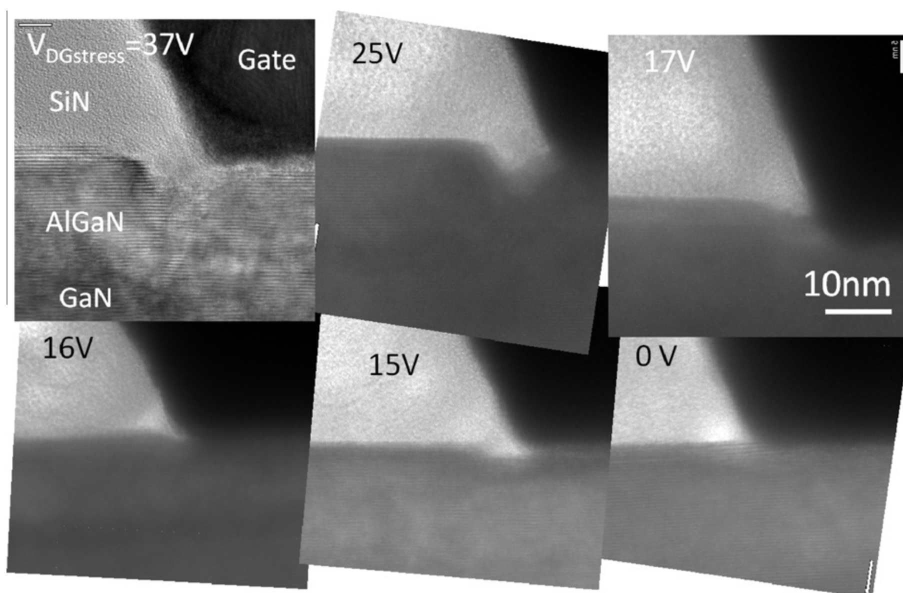

Fig. 5. TEM images of the source side of device #1–6.

the data of Fig. 1. The most heavily degraded device (#1) exhibits about 35% of permanent degradation and 15% of current collapse after the stress. On the other hand, the devices stressed up to 16 and 15 V (devices #4 and 5, respectively) show negligible electrical degradation in the drain current, whether transient or permanent. The average value of current collapse for all devices in their virgin state is 0.2%.

We have also investigated the impact of long-term stress at voltages below and above the critical voltage with the device biased in the $V_{DS} = 0$ regime. First, a device (#7) was stressed at $V_{GS} = -11$ V, which is below V_{crit}, for 12 h at 150 °C. Another device (#8) was first step-stressed up to $V_{GS} = -40$ V in order to confirm the transition through the critical voltage and then stressed at -40 V at 150 °C for an additional 210 min.

As shown in Fig. 3a, long-term stressing below V_{crit} shows no degradation in I_{Goff} although I_{Dmax} and the series resistances slightly degrade over time. For this device, permanent degradation and current collapse after the stress was 5% and 0.6%, respectively. Although current collapse remained at the level of the virgin device, there was a small degree of permanent degradation that is not observed during short-term step-stress below V_{crit} (device #5 above). This suggests that there is a separate long-term degradation mechanism below V_{crit} (and perhaps unrelated to V_{crit}) that permanently degrades I_D without introducing traps.

The device stressed at high voltage for a long time (#8) shows significant degradation in all figures of merit (Fig. 3b). Permanent degradation and current collapse after the stress were 42% and 14%, respectively. Compared to the device stressed up to nearly the same voltage in step-stress experiments (#1), current collapse is almost the same, while there is additional permanent degradation presumably a consequence of the device being held for much longer time at the maximum stress voltage.

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3. TEM analysis

TEM cross section was prepared by in situ lift-out, using an FEI Helios dual beam focused ion beam (DB-FIB). Cross-section TEM analysis was performed using FEI Titan 80–300 TEM at 300 kV. The locations where the device was cut were chosen at random. Only one cut was done per device. TEM images of the entire device cross section were obtained from that cut. We zoomed into the gate corner regions because this is where previous studies have revealed structural damage [12–17]. There was no other region that showed any significant and systematic difference between the stressed and unstressed devices. In these regions and in selected samples, we also performed Electron Energy Loss Spectroscopy (EELS) in order to study material compositions.

Fig. 4 shows TEM pictures obtained for selected devices from the step-stress experiments of Fig. 1. Near the gate edge, the control unstressed device (#6, labeled 0 V in Fig. 4) shows a smooth semiconductor surface. The devices stressed up to 16 V show minimal structural degradation. Only a small indentation less than 2 nm deep and 10 nm wide is observed on the GaN cap surface next to the gate edge. This seems to correspond to the groove that has been observed in a separate plan-view study [17]. For that reason, we will refer to this feature as a groove although TEM cannot confirm whether this feature is continuous in and out of the cross section. Devices that are stressed well beyond V_{crit} (25 and 37 V) show significant physical degradation in the form of deep pits (up to 4–6 nm in depth and 17 nm in width at the surface). For these devices, the pits penetrate into the AlGaN barrier layer. The device stressed at 37 V also exhibits a crack-like feature that extends at an angle from the bottom of the pit to the AlGaN/GaN interface. Since these devices are symmetrically stressed in both the source and drain sides, similar observations were made on the source side (Fig. 5). These pictures reveal that short-term stress is enough to produce significant structural degradation if the stress voltage is higher than the critical voltage. It does also reveal the presence of small surface indentations for voltages below the critical voltage consistent with the grooves observed in [17].

TEM images for long-term stressed devices are shown in Fig. 6. The device stressed below V_{crit} (Fig. 6a) shows a shallow groove of about 1.5 nm in depth and 6 nm in width at the gate corner. However, in spite of the extended stress time, this is again not deep enough to penetrate into the AlGaN barrier. This small structural degradation may account for the small permanent degradation in I_{Dmax}. The sample stressed beyond V_{crit} for a long time (Fig. 6b) shows a deeper (~6 nm) pit that reaches into the AlGaN layer. This result suggests that stress at voltages in excess of V_{crit} is necessary for deep pit formation.

In the TEM analysis performed here we have found no evidence of the consumption of an interfacial layer that is present between the gate metal and semiconductor surface in the virgin devices as a result of long-term high-voltage stress [14,22]. In fact, the existence of this interfacial layer is not altogether evident in all devices. For example, as shown in Fig. 4, it is the most heavily degraded device that shows the most obvious interfacial layer. Thus, we postulate that the existence of the interfacial layer results from process variations and is unrelated to stress although further study is necessary to confirm this.

In EELS analysis, we have found that both the shallow groove and deep pit areas contain much higher oxygen as compared to the undamaged surrounding semiconductor area. EELS can distinguish nitrogen and oxygen, and we have observed a very strong oxygen signal in the defect area. The unstressed device does now

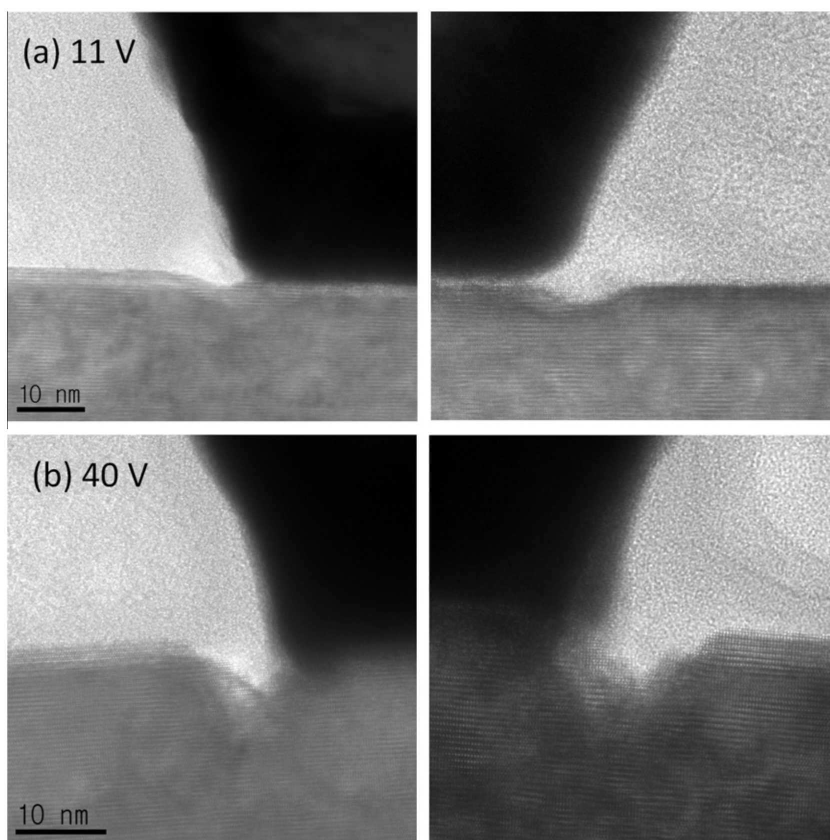

Fig. 6. Cross-sectional TEM images for long-term stressed devices. The source (left) and drain (right) sides are shown. Stress voltages are: (a) V_{DG} = 11 V (device #7) and (b) V_{DG} = 40 V (device #8).

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show any evidence of presence of oxygen in this region. This is consistent with the previous observation with EDX analysis where the defect region contained a high concentration of oxygen [16]. This suggests that the formation of these defects involves some kind of oxidation even in its early stage. A more detailed study of EELS is beyond the scope of this paper.

4. Correlation between electrical and physical degradation

To provide a quantitative comparison between electrical and physical damage, we have measured the width and the depth of the pits that are observed in TEM pictures. We have then graphed the degradation in uncollapsed I_{Dmax} (in absolute amount) and the value of current collapse against the depth of the defective region. This is shown in Fig. 7. The permanent degradation in I_{Dmax} and the current collapse both correlate well with the depth of the defective region. Serious electrical degradation only takes place when the depth of the defective region exceeds the GaN cap thickness (~3 nm). It is noted that the long-term stressed devices (#7 and 8) also fall in the same correlation as the short-term stressed devices (#1–5).

The correlation between electrical degradation, as measured through I_{Dmax}, R_S and R_D, and structural degradation, as evaluated through the depth of the defective region observed in cross-section TEM, is entirely consistent with a similar study that utilized AFM and SEM mapping of the semiconductor surface after gate and dielectric removal [17]. This is true in spite of the fact that, in the present study, a single cut was made at a random location across the width of the device. It is not surprising that the prominent defects observed here and in [17] result in permanent (non transient) degradation of the drain current. The formation of deep pits should induce local strain relaxation which ought to result in a local reduction of piezoelectric-effect induced charge, and a decrease in the sheet carrier density. With stress in the $V_{DS} = 0$ regime, this should also result in a permanent increase in both the source and drain resistances. At the same time, it is reasonable to expect that the introduction of structural defects at the corner of the gate provides trapping sites for electrons leading to current collapse.

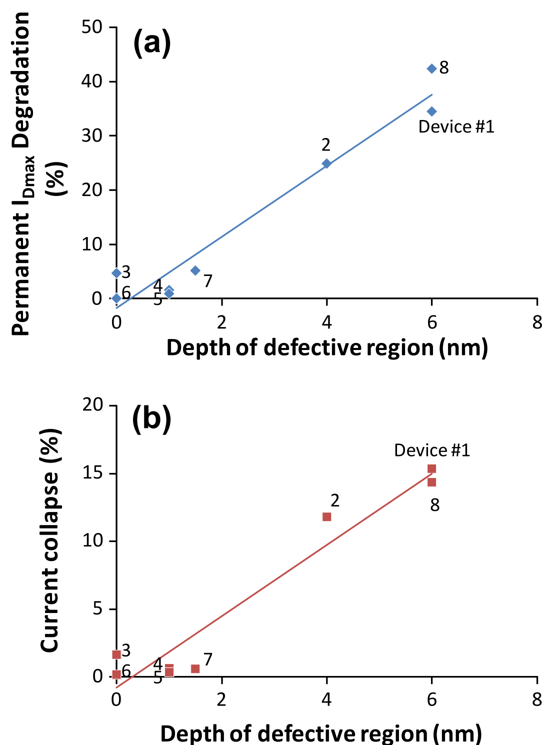

Fig. 7. Correlation between electrical and structural degradation for all samples in this study: (a) permanent I_{Dmax} degradation vs. pit depth and (b) current collapse after stress vs. pit depth.

A separate finding in our work is the imperfect correlation between physical damage and I_{Goff}. In this work and also in [17], the sudden rise in I_{Goff} at the critical voltage appears to be associated with the exposure of the AlGaN barrier as the groove in the GaN cap grows in depth. However, as the stress voltage is increased from this point, the pit becomes deeper in a continued way but the increase in I_{Goff} tends to saturate (this is also observed in [17]). The reason for this is not understood and indicates that further research is necessary.

The strong correlation that we observe between electrical and structural degradation confirms previous studies made in long-term life-test experiments [13]. We now know that serious structural degradation essentially starts right at the critical voltage.

5. Conclusions

In summary, we have found that the critical voltage for electrical degradation of GaN HEMTs marks also the onset of prominent crystallographic degradation of the cap and barrier layers at the gate edge of the device. Physical and electrical degradation are found to correlate closely. Our results provide unequivocal evidence for the observed crystallographic damage to be responsible for the electrical degradation of GaN HEMTs.

Acknowledgements

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