# Effect of Trapping on the Critical Voltage for Degradation in GaN High Electron Mobility Transistors

Sefa Demirtas, Jesús A. del Alamo
Microsystems Technology Laboratories
Massachusetts Institute of Technology
Cambridge, MA 02139
TEL: +1 – 617 – 253 – 1620, FAX: +1 – 617 – 258 – 7393, E – mail: sefa@mit.edu

***Abstract*— We have performed $V_{DS}$ = 0 V and OFF–state step–stress experiments on GaN–on–Si and GaN–on–SiC high electron mobility transistors under UV illumination and in the dark. We have found that for both stress conditions, UV illumination decreases the critical voltage for the onset of degradation in gate current in GaN–on–Si HEMTs in a pronounced way, but no such decrease is observed on SiC. This difference is attributed to UV–induced electron detrapping, which results in an increase in the electric field and, through the inverse piezoelectric effect, in the mechanical stress in the AlGaN barrier of the device. Due to the large number of traps in GaN–on–Si, this effect is clearer and more prominent than in GaN–on–SiC, which contains fewer traps in the fresh state.**

***Keywords– GaN HEMTs, critical voltage, degradation, UV illumination, detrapping***

## I. INTRODUCTION

GaN high electron mobility transistors (HEMTs) are promising devices for high power and high frequency applications. Si is an attractive substrate for GaN HEMTs because of its lower cost, availability in large diameters and sophisticated technology base. However, the larger lattice and thermal mismatch between GaN and Si as compared to the more commonly used substrate, SiC, results in more defects and certain kinds of dislocations [1–2]. Although it has been recently reported that no misfit dislocations are observed and that screw dislocations are present at a density lower than $10^7$ $cm^{-2}$ in GaN on Si, the density of edge and mixed dislocations are on the order of 1–5x$10^9$ $cm^{-2}$ whereas it is in the $10^8$ $cm^{-2}$ range for GaN on SiC [1–3]. The concern is that these defects may compromise the reliability of GaN HEMTs on Si.

We have previously shown that GaN–on–Si HEMTs are affected by a similar degradation mechanism as GaN–on–SiC HEMTs, namely a sharp increase of the gate current at a certain voltage that has been termed the *critical voltage* [4–5]. We have attributed this degradation to defect generation due to excessive mechanical stress introduced by the inverse piezoelectric effect at high voltage [4–5]. In GaN–on–Si HEMTs we have observed relatively high critical voltages with a rather wide range of values even for devices in the same reticle. Separately, we detected significant electron trapping associated with pre–existing traps in virgin devices, much more than in typical GaN–on–SiC HEMTs [6]. In this work, we report an intriguing finding: the high number of traps that are present in GaN–on–Si HEMTs seems to be partially responsible for the high critical voltages for the onset of electric field–induced degradation of the gate current. We postulate that electron trapping during electrical stress leads to lower electric fields and increased robustness against gate current degradation. This finding should be of wide applicability regardless of the characteristics of the substrate.

## II. EXPERIMENTAL

We studied experimental $Al_xGa_{1-x}N$/GaN HEMTs on Si with a 17.5 nm thick $x$ = 0.26 AlGaN barrier. The gate width is 2x25 μm and the gate–source, gate–drain separation and the gate length are 1, 3 and 0.5 μm, respectively. The devices include a source-connected field plate [7–8]. These devices are representative of the capabilities of the GaN–on–Si technology. They exhibit $P_{out}$ = 3.9 W/mm and $PAE$ = 62% at 2.14 GHz under $V_{DS}$ = 28 V. They also show excellent electrical reliability: an average lifetime in excess of $10^7$ hours with $E_a$ = 1.7 – 2.0 eV has been reported [9–11].

The $Al_xGa_{1-x}N$/GaN HEMTs on SiC substrate used in this study have a 16 nm AlGaN barrier with $x$ = 0.28 [12]. The gate width is also 2x25 μm, however the drain and source are located symmetrically at a distance of 2 μm from the gate. Since the peak electric field that is responsible for the onset of inverse piezoelectric degradation is encountered at the vicinity of the gate [5], the difference in gate–source and gate–drain spacing is acceptable when comparing the reliability of both technologies. GaN–on–SiC HEMTs have an integrated field plate [12–13], which plays a similar role to the source field plate in GaN–on–Si HEMTs. These experimental devices exhibit $P_{out}$ = 8 W/mm and $PAE$ = 62% at 10 GHz under $V_{DS}$ = 40 V.

We performed $V_{DS}$ = 0 V step–stress experiments where we grounded the drain and source and stepped the gate voltage starting from –5 V to –80 V by decreasing 1 V every 30 seconds. Important DC figures of merit were continuously measured by a benign characterization suite. In this stress scheme, both the drain and source sides of the gate are stressed with increasing electric field over time. This is a very harsh stress bias condition when compared with the normal operation of the device. We use this stress because it reveals important aspects of the physics of degradation in GaN HEMTs in an accelerated manner [4–5].

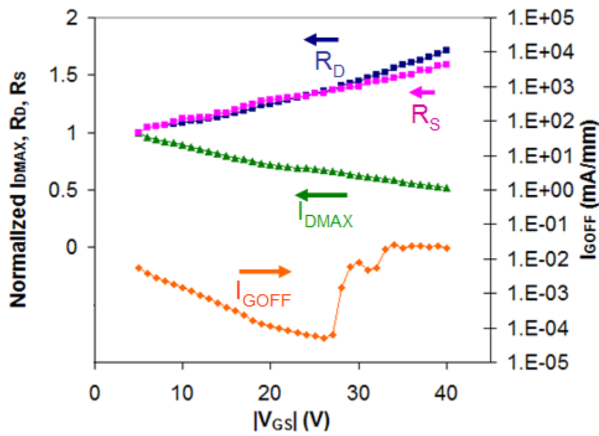


**Fig. 1.** Normalized $I_{DMAX}$, $R_S$, $R_D$ (left axis) and $I_{GOFF}$ (right axis) as a function of $|V_{GS}|$ in a $V_{DS} = 0$ V step–stress experiment on a GaN–on–Si HEMT. $V_{GS}$ is stepped from –5 V by –1 V steps every 30 seconds.

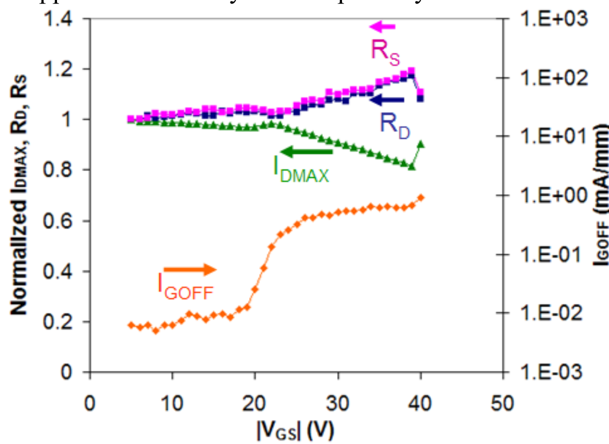


**Fig. 2.** Normalized $I_{DMAX}$, $R_S$, $R_D$ (left axis) and $I_{GOFF}$ (right axis) as a function of $|V_{GS}|$ in a $V_{DS} = 0$ V step–stress experiment on a GaN–on–SiC HEMT. $V_{GS}$ is stepped from –5 V by –1 V steps every 30 seconds.

We also performed OFF–state step–stress experiments, which are more representative of the normal use conditions for these HEMTs. In this approach, $V_{GS}$ is kept constant at –5 V while $V_{DS}$ is stepped in 1 V steps from 5 V to 80 V every 30 seconds. Since the voltage across the gate and source is constant throughout the experiment, it is the drain side of the device that is exposed to high electrical stress. This difference is also why $V_{DS} = 0$ V stress is harsher than OFF–state stress [4]. On the other hand, $V_{DS} = 0$ V and OFF–state step–stress experiments are similar in that the channel is always OFF and there is negligible drain current and negligible self heating taking place in the device. This condition helps to isolate the effects of current and temperature from that of electric field, as the field is found to be the main cause of degradation in GaN HEMTs [4–5].

## III. Results

Figs. 1 and 2 show the results of typical $V_{DS} = 0$ V step–stress experiments in a GaN–on–Si HEMT and a GaN–on–SiC HEMT, respectively. The graphs show the maximum current, $I_{DMAX}$ (defined at $V_{DS} = 5$ V and $V_{GS} = 2$ V); source resistance, $R_S$ and drain resistance, $R_D$ on the left axis (all normalized to their initial values) and the OFF–state gate current, $I_{GOFF}$ (defined at $V_{DS} = 0.1$ V and $V_{GS} = -5$ V) on the right axis as a function of $|V_{GS}|=|V_{GD}|$. These experiments stop at –40 V.

In both devices, at a certain voltage, there is a sharp rise in $I_{GOFF}$ that is irreversible. This voltage is what we term the critical voltage, $V_{CRIT}$. The increase in $I_{GOFF}$ is attributed to the creation of defects in the AlGaN barrier layer by excessive mechanical stress introduced by the inverse piezoelectric effect [4–5]. In our experiments, we see this pattern of degradation in both types of devices also under OFF–state step–stress conditions although the degradation is somewhat larger in the $V_{DS} = 0$ V condition due to its harsher nature (not shown).

While the distinct critical voltage behavior of the degradation of $I_{GOFF}$ in GaN–on–Si HEMTs is similar to that of GaN–on–SiC devices, there are also marked differences between the patterns of degradation in both devices. For stress voltages below the critical voltage, $I_{GOFF}$ and $I_{DMAX}$ are observed to decrease starting from the beginning of the stress, and $R_D$ and $R_S$ increase in GaN–on–Si HEMTs (Fig. 1). In GaN–on–SiC HEMTs these figures of merit remain largely unchanged below $V_{CRIT}$ (Fig. 2). Along with other evidence [6], this unique behavior of GaN–on–Si HEMTs derives from the prominent electron trapping that these devices suffer from in their virgin state. Another important observation from GaN–on–Si HEMTs that is relevant here is shown in Fig. 3. For these devices, $V_{CRIT}$ varies significantly from device to device even when they are nominally identical and at close proximity on the wafer [6].

In order to investigate the role of trapping on the critical voltage, we performed identical stress experiments, except for UV illumination, on pairs of neighboring identical devices. One of these experiments was performed in the dark whereas in the other, its neighbor was illuminated by 365 nm UV light. The intensity of the UV light source at a distance of 4 cm from the device was measured to be 1.56 mW/cm$^2$, which corresponds to 2.9x10$^{15}$ photons/cm$^2$–s. Separately we verified that 365 nm UV light greatly enhances electron detrapping [6, 14]. Fig. 4 shows a typical result in GaN–on–Si HEMTs under $V_{DS} = 0$ V

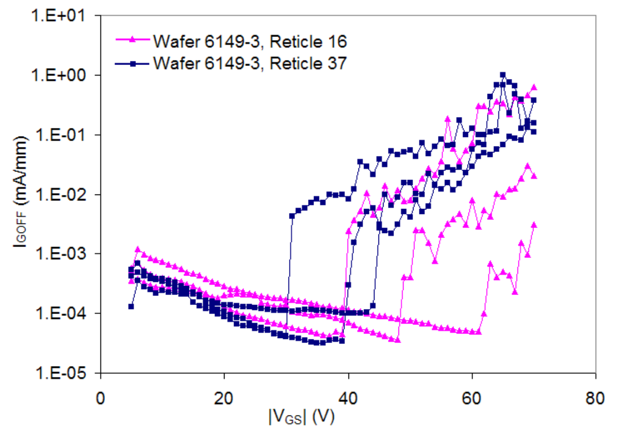


**Fig. 3**. $I_{GOFF}$ vs. stress $|V_{GS}|$ for six GaN–on–Si devices in typical $V_{DS} = 0$ V step–stress experiments. The distribution of $V_{CRIT}$ is very broad even for devices in close proximity. Very high $V_{CRIT}$ values are also observed.

This work was funded by DARPA (WBGS program through ARL) and Office of Naval Research (MURI)

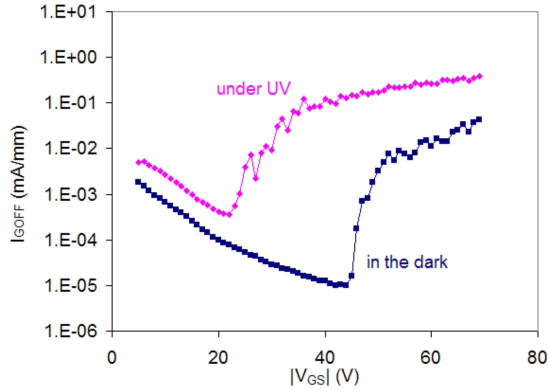


**Fig. 4.** Evolution of $I_{GOFF}$ in $V_{DS} = 0$ V step–stress experiments on two neighboring GaN–on–Si devices, where one of them was stressed under UV illumination (365 nm) and the other in the dark. Under UV illumination $V_{CRIT}$ is significantly smaller than in the dark.

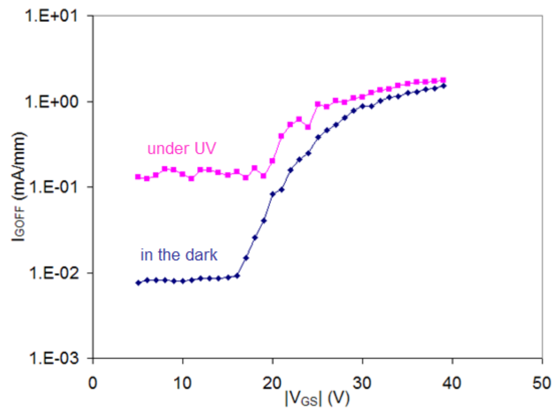


**Fig. 5.** Evolution of $I_{GOFF}$ in $V_{DS} = 0$ V step–stress experiments on two neighboring GaN–on–SiC devices, where one of them was stressed under UV illumination (365 nm) and the other in the dark. No significant effect of UV on $V_{CRIT}$ is observed.

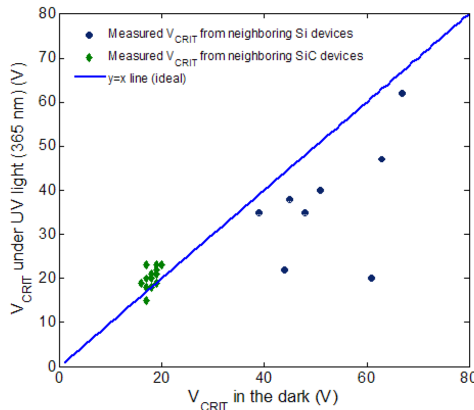


**Fig. 6.** Comparison of $V_{CRIT}$ in $V_{DS} = 0$ V step–stress experiments for closest–neighbor pairs of devices. One device from each pair is stressed under UV and the other in the dark. UV illumination generally results in a lower value of $V_{CRIT}$ for GaN–on–Si devices (8 pairs shown). $V_{CRIT}$ values in the dark and under illumination are negligibly different for GaN–on–SiC devices (15 pairs shown).

step–stress conditions. Under illumination, $V_{CRIT}$ is significantly smaller than in the dark. In contrast with this observation, in a similar experiment, $V_{CRIT}$ in typical GaN–on–SiC HEMTs did not change (Fig. 5). UV light also produces an increase in $I_{DMAX}$ and a reduction in $R_D$ and $R_S$ relative to the dark, which proves that UV light reaches close to the intrinsic device and successfully enhances detrapping of electrons during stress.

Fig. 6 shows the results obtained on several such pairs of $V_{DS} = 0$ V step–stress experiments. Each point in the figure corresponds to a pair of neighboring identical devices. The abscissa is the critical voltage when a device was stressed in the dark and the ordinate is the critical voltage when its neighbor was stressed under UV illumination. On average, $V_{CRIT}$ in GaN–on–Si HEMTs is 29% smaller under UV illumination while it is about the same as in the dark in GaN HEMTs on SiC. The spread in $V_{CRIT}$ values in the dark and under light for GaN on Si HEMTs in Fig. 6 is rather broad reflecting the relatively wide distribution of $V_{CRIT}$ values that was shown in Fig. 3 even among devices spaced by short distances.

In order to further explore this shift in $V_{CRIT}$ under UV illumination in GaN–on–Si HEMTs, similar experiments were performed under different stress bias conditions and with different wavelengths. Fig. 7 shows OFF–state step–stress experiments performed on two neighboring devices on Si in the dark and under UV light illumination. In this stress condition, a high electric field appears on the drain side of the gate, which is not covered by a field plate and is ensured to be exposed to UV illumination. An average reduction of $V_{CRIT}$ of 17% was observed as a result of UV illumination (Fig. 8).

The effects of 254 nm UV as well as visible microscope light were also investigated although results are not shown here. The intensity at 4 cm from the devices was measured to be 1.62 mW/cm$^2$ for 254 nm UV light, which corresponds to 2.1x10$^{15}$ photons/cm$^2$–s. We found that 254 nm UV light was less effective in detrapping electrons due to the different absorption rate by the AlGaN barrier and/or less number of incident photons, hence it had a smaller effect on $V_{CRIT}$ (only 11% decrease in $V_{CRIT}$ under $V_{DS} = 0$ V step–stress). Visible microscope light resulted in no shift in the average $V_{CRIT}$, which is consistent with the observation that it induces negligible detrapping.

## IV. Discussion

Our experiments suggest that native traps (those that exist in the virgin device) play a role in determining the critical voltage for high–voltage gate current degradation of GaN HEMTs. We know from earlier experiments that the application of high voltage results in electron trapping in GaN HEMTs [15]. This trapping reduces the sheet carrier concentration in the high field region of the channel and, in consequence, the peak electric field at the gate edge. This manifests itself, among other ways, in a reduction in the gate current as the voltage increases in electrical stress experiments as can be seen in Figs. 1 and 4. A similar reduction in gate leakage current has also been observed by other authors on GaN–capped devices on SiC substrates after ON and OFF state

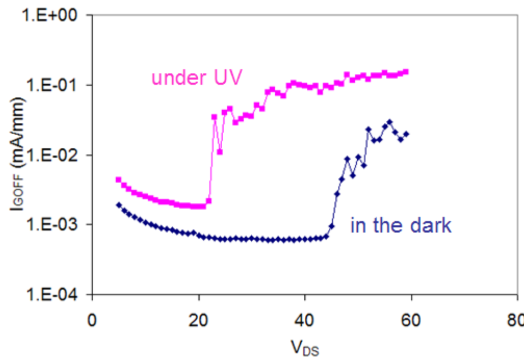


**Fig. 7.** OFF state step–stress experiments on two neighboring GaN–on–Si devices, where one of them was stressed under UV illumination (365 nm) and the other in the dark. Similar to $V_{DS}$ = 0 V step–stress, $V_{CRIT}$ is significantly smaller under UV illumination than in the dark.

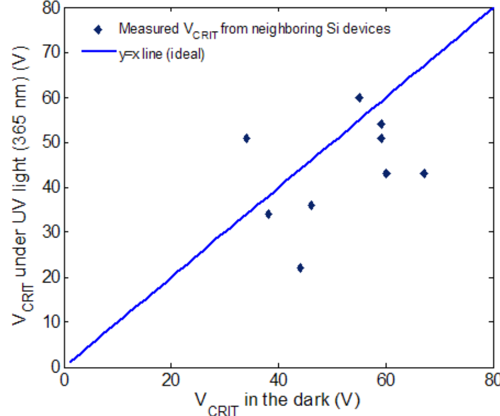


**Fig. 8.** Comparison of $V_{CRIT}$ under OFF–state step–stress experiments for closest–neighbor pairs of devices on Si when one device from each pair is stressed under UV and the other in the dark. UV illumination in OFF–state stress generally results in a lower reduction in value of $V_{CRIT}$ than $V_{DS}$ = 0 V stress for GaN–on–Si devices (9 pairs shown).

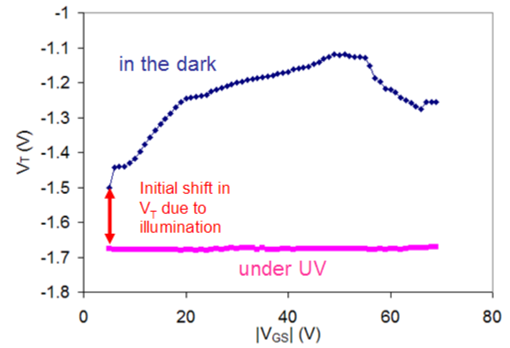


**Fig. 8.** Evolution of $V_T$ in the $V_{DS}$ = 0 V step–stress experiments shown in Fig. 4. Under UV illumination, $V_T$ stays rather constant as opposed to shifting in the positive direction due to trapping in the dark. The initial shift in $V_T$ observed for the neighboring device in the dark can be considered as a relative measure of UV–induced detrapping from the native traps in the fresh device.

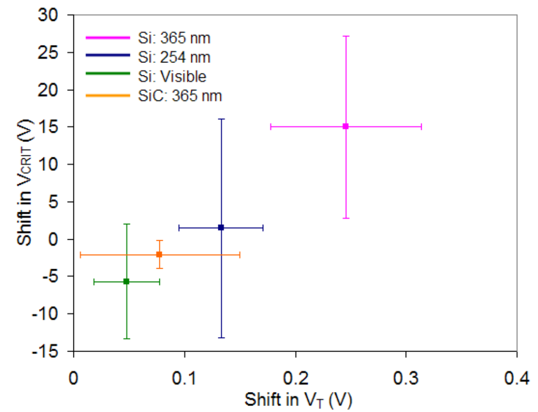


**Fig. 7.** Correlation between the average initial shift in $V_T$ under several illumination schemes and the resulting shift in $V_{CRIT}$ obtained from $V_{DS}$ = 0 V step–stress experiments on pairs of neighboring devices. The error bars represent one standard deviation on each side around the mean value. Under conditions in which $V_T$ shifts in a substantial way as a result of light illumination, $V_{CRIT}$ is also seen to be reduced.

stress experiments [16]. The application of UV illumination causes electron detrapping and increases the electric field. This is seen in the increase in the gate leakage current observed at the beginning of the experiments in Figs. 4 and 7, which is not of a photovoltaic nature [17]. Through the inverse piezoelectric effect, the increase in the electric field should result in an increase in the elastic energy density stored in the AlGaN barrier, which will therefore reach the critical value for defect formation at a lower critical voltage [18].

A correlation between trap density in the virgin device and the shift in $V_{CRIT}$ can be obtained by examining the shift in the threshold voltage induced by UV light. In our hypothesis, UV illumination results in electron detrapping. This should produce a negative shift in $V_T$. The larger the shift, the higher the concentration of traps in the device. Fig. 9 shows the evolution of $V_T$ for the $V_{DS}$ = 0 V step–stress experiments illustrated in Fig. 4. In the dark, $V_T$ shifts positive as traps get filled with electrons. Under UV, electron trapping is largely suppressed and $V_T$ remains unchanged throughout the experiment. The amount of $V_T$ change at the beginning of the experiment can be considered as a qualitative measure of the number of traps in the virgin device. Hence, the correlation between trapping and change in $V_{CRIT}$ can be verified by comparing the initial shift in $V_T$ as a result of illumination and the corresponding decrease in $V_{CRIT}$. Fig. 10 displays the average initial shift in $V_T$ on the horizontal axis and the corresponding average shift in $V_{CRIT}$ on the vertical axis with error bars. This figure shows that they both correlate and that the correlation for different types of illumination follows a general trend that is also consistent. The shift in $V_{CRIT}$ and $V_T$ are both minor in GaN–on–SiC HEMTs regardless of the illumination scheme, which is consistent with the fact that they have few native traps.

## V. CONCLUSIONS

In conclusion, we have studied the degradation of GaN–on–Si and GaN–on–SiC HEMTs under UV illumination and in the dark. We have observed a pronounced decrease in $V_{CRIT}$ for GaN–on–Si HEMTs under UV light in both $V_{DS}$ = 0 V and OFF–state step–stress experiments. We have proposed a mechanism where UV–induced electron detrapping from native traps increases the sheet carrier concentration in the channel, which results in an increase in the peak electric field and in the elastic energy stored in the AlGaN barrier of the HEMT through the inverse piezoelectric effect. This decreases the critical voltage for defect formation. A similar shift in $V_{CRIT}$ was not observed in GaN–on–SiC HEMTs where trapping in the virgin devices is minimal. Our work suggests that the existence of an increased number of traps in GaN–on–Si HEMTs might enhance the robustness of the devices to high voltage degradation of the gate current.

## ACKNOWLEDGMENT

This work was funded by the DARPA WBGS program (Mark Rosker, program manager) under ARL contract #W911QX–05–C–0087 (Alfred Hung, COTR) and by the Office of Naval Research Grant #N00014–08–1–0655 (Paul Maki and Harry Dietrich, Program Managers). We also acknowledge collaboration with Nitronex Corporation and TriQuint Semiconductor and discussions with Dr. Jungwoo Joh.

## REFERENCES

[1] P. Rajagopal et al., “Large–area, device quality GaN on Si using a novel transition layer scheme,” Mater. Res. Soc. Sympos. Proc. vol. 743, L1. 2 (2002).

[2] J. C. Roberts, J. W. Cook, Jr., P. Rajagopal, E. L. Piner, and K. Linthicum, “AlGaN transition layers on Si (111) substrates – observations of microstructure and impact on material quality,” Mater. Res. Soc. Sympos. Proc. vol. 1068, C06–03 (2008).

[3] R. Quay, *Gallium Nitride Electronics*, illustrated ed. Berlin: Springer, 2008.

[4] J. Joh and J. A. del Alamo, "Critical voltage for electrical degradation of GaN high–electron mobility transistors," IEEE Electron Device Lett., vol. 29, no.4, pp. 287–289 (2008).

[5] J.A. del Alamo and J. Joh, “GaN HEMT reliability,” Microelectronics Reliability, vol. 49, Issues 9–11, 20th Europ. Sympos. Reliab. Electron Devices, Fail. Phys. and Analysis, pp. 1200–1206 (2009).

[6] S. Demirtas and J. A. del Alamo, “Critical voltage for electrical reliability of GaN high electron mobility transistors on Si substrate,” Reliab. of Compound Semicond. Workshop, pp. 53–56 (2009).

[7] A. W. Hanson et al., “Development of GaN transistor process for linear power applications,” Comp. Sem. MANTECH, pp. 107–110 (2004).

[8] J. W. Johnson et al., “Material, process and device development of GaN–based HFETs on silicon substrates,” Electrochem. Soc. Proc., vol. 2004–06, pp. 405–419 (2004).

[9] E.L. Piner et al., “Device degradation phenomena in GaN HFET technology: status, mechanisms, and opportunities,” Internat. Electron Devices Mtg., pp.1–4 (2006).

[10] S. Singhal., et al., “Reliability of large periphery GaN–on–Si HFETs,” Reliab. of Compound Semicond. Workshop, pp. 135–149 (2005).

[11] S. Singhal et al., “Qualification and reliability of a GaN process platform,” Comp. Sem. MANTECH, pp. 83–86 (2007).

[12] U. Chowdhury et al., “TEM observation of crack– and pit–shaped defects in electrically degraded GaN HEMTs,” IEEE Electron Device Lett., vol. 29, pp. 1098–1100 (2008).

[13] D. Fanning et al., “High voltage GaAs pHEMT technology for S–band high power amplifiers,” Comp. Sem. MANTECH, pp. 173–176 (2007).

[14] G. Koley, V. Tilak, L. F. Eastman and M. G. Spencer, "Slow transients observed in AlGaN/GaN HFETs: Effects of $SiN_x$ passivation and UV illumination," IEEE Trans. Electron Devices, vol. 50, no.4, pp. 886–893 (2003).

[15] J. Joh and J. A. del Alamo, “Impact of electrical degradation on trapping characteristics of GaN high electron mobility transistors,” Internat. Electron Devices Mtg., pp.1–4 (2008).

[16] G. Meneghesso, F. Rampazzo, P. Kordos, G. Verzellesi and E. Zanoni, “Current collapse and high–electric–field reliability of unpassivated GaN/AlGaN/GaN HEMTs,” IEEE Trans. Electron Devices, vol. 53, no. 12, pp. 2932–2941 (2006).

[17] J. Joh, L. Xia and J. A. del Alamo, “Gate current degradation mechanisms of GaN high electron mobility transistors,” Internat. Electron Devices Mtg., pp. 385–388 (2007).

[18] J. Joh and J. A. del Alamo, “A model for the critical voltage for electrical degradation of GaN high electron mobility transistors,” Reliab. of Compound Semicond. Workshop, pp. 3–6 (2009).